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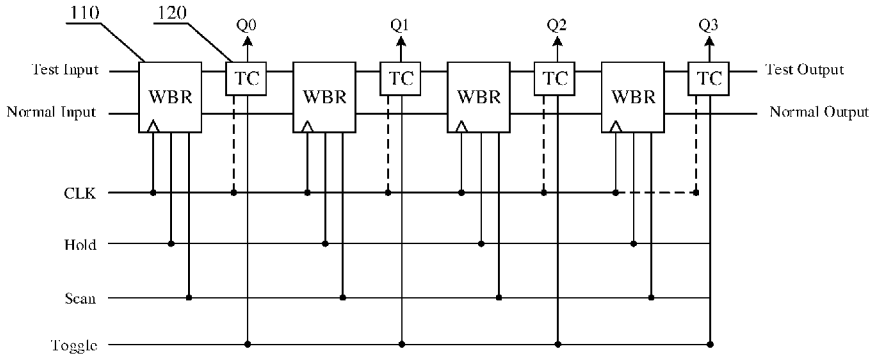


FIG. 1

(57) **Abstract:** Boundary test circuit, memory and boundary test method are provided. The boundary test circuit may include a plurality of serially-connected wrapper boundary registers (WBRs) (110) and a plurality of toggle circuits (TCs) (120). Each WBR (110) may include a first I/O for receiving an initial test signal and a second I/O for transmitting the initial test signal to the WBR (110) at a succeeding stage. Each TC (120) may include an input for receiving the initial test signal stored in a corresponding WBR, a control I/O for receiving a toggle signal, and an output for transmitting a real-time test signal to the integrated circuit. The toggle signal may be configured to control phase switching of the real-time test signal, and, depending on the toggle signal, the real-time test signal may have a phase identical or inverse to a phase of the initial test signal. This method improves the efficiency and flexibility of the boundary test.

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BOUNDARY TEST CIRCUIT, MEMORY AND BOUNDARY TEST METHOD

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority of the Chinese Patent Application No. 201810986092.3, filed on August 28, 2018 and entitled "BOUNDARY TEST CIRCUIT, MEMORY AND BOUNDARY TEST METHOD." The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This invention relates generally to the technical field of electronics, and more specifically, to a boundary test circuit, memory and boundary test method.

BACKGROUND

[0003] In modern electronic system, with the technology advancements in large-scale integrated circuit and manufacturing technologies, printed circuit boards are increasingly becoming smaller, denser and thinner. With the number and the density of pins on a device continuously increasing, conventional "probe" test methods that test a chip using a multimeter and an oscilloscope are unable to meet the demand.

[0004] Boundary scan test is an emerging test method. A boundary scan test may be implemented by adding a boundary scan cell (BSC) on each I/O pin of a chip along with some additional test control logics. Each of the BSCs may be composed of registers, and each I/O pin of the chip may correspond to a BSC. Each BSC may include two data channels, one of which is a test data channel for test data input (TDI) and test data output (TDO), and the other is a normal data channel for normal data input (NDI) and normal data output (NDO).

[0005] In an existing boundary test circuit, in a test mode, the test data is sequentially transmitted at each clock cycle, and the data of each BSC is output to a to-be-tested integrated circuit via the I/O pins. Different test vectors may first need to be input to all BSCs before they can be output to the to-be-tested integrated circuit. As a result, conventional boundary test circuits have low efficiency and poor flexibility. Therefore, a boundary test circuit and related method that can address at least some of the aforementioned limitations are desired.

[0006] The information disclosed in the Background section is for facilitating the understanding on the background of the invention and therefore may include information that does not constitute prior art already known to a person of ordinary skills in the art.

SUMMARY

[0007] To address the limitations of conventional technologies described above, this disclosure provides a boundary test circuit, a memory and a boundary test method.

[0008] One aspect of this disclosure is directed to a boundary test circuit for testing an integrated circuit. The boundary test circuit may include a plurality of serially-connected wrapper boundary registers (WBRs) and a plurality of toggle circuits (TCs). Each WBR may include a first I/O for receiving an initial test signal, and a second I/O for transmitting the initial test signal to the WBR at a succeeding stage. Each TC may include an input for receiving the initial test signal stored in a corresponding WBR, a control I/O for receiving a toggle signal, and an output for transmitting a real-time test signal to the integrated circuit. A phase of the real-time test signal may be either identical or inverse to a phase of the initial test signal.

[0009] In some embodiments, in the aforementioned circuit, the toggle signal may be configured to control phase switching of the real-time test signal.

[0010] In some embodiments, in the aforementioned circuit, each TC may include a NOT gate and a first data selector. The NOT gate may include an input for receiving the initial test signal stored in a WBR, and the first data selector may include a first input for receiving the initial test signal, a second input connected to an output of the NOT gate, a control I/O for receiving the toggle signal, and an output for transmitting the real-time test signal.

[0011] In some embodiments, in the aforementioned circuit, each TC comprises a first register, an OR gate, an XOR gate, and a second data selector. The first register may include an input for receiving the initial test signal stored in a WBR. The OR gate may include a first input connected to an output of the first register, and a second input for receiving the toggle signal. The XOR gate may include a first input connected to the output of the first register, and a second input for receiving the toggle signal. The second data selector may include a first input connected to an output of the OR gate, a second input connected to an output of the XOR gate, a control I/O for receiving the toggle signal, and an output for transmitting the real-time test signal.

[0012] In some embodiments, in the aforementioned circuit, each TC may be configured to transmit the real-time test signal under the control of a CLK signal.

[0013] In some embodiments, in the aforementioned circuit, each WBR may include a third data selector, a second register, and a fourth data selector. The third data selector may include a first input

for receiving the initial test signal, and a control I/O for receiving a Hold signal. The second register may include an input connected to an output of the third data selector, and an output for outputting the initial test signal stored in the second register. The fourth data selector may include a first input for receiving a Normal input, a second input connected to the output of the second register, a control I/O for receiving a Scan signal, and an output for transmitting the Normal output. The output of the fourth data selector may be connected to a second input of the third data selector.

[0014] In some embodiments, in the aforementioned circuit, each WBR may be configured to transmit the initial test signal under the control of a CLK signal.

[0015] In some embodiments, the integrated circuit may be a memory.

[0016] This inventive concept further provides a memory having a boundary test circuit. The boundary test circuit may be configured to test the memory.

[0017] This inventive concept further provides a boundary test method for testing an integrated circuit. The test method may include receiving, by each wrapper boundary register (WBR) in a plurality of serially-connected WBRs, an initial test signal, and receiving, by each toggle circuit (TC) in a plurality of TCs, the initial test signal stored in a corresponding WBR. Each WBR may transmit the initial test signal to the WBR at a succeeding stage, and the TC may transmit a real-time test signal to the integrated circuit according to a toggle signal. A phase of the real-time test signal may be either identical or inverse to a phase of the initial test signal.

[0018] In some embodiments, in the aforementioned test method, the toggle signal may be configured to control phase switching of the real-time test signal.

[0019] In some embodiments, the aforementioned test method may further comprise receiving, by each TC in the plurality of TCs, a CLK signal, and each TC may transmit the real-time test signal under the control of the CLK signal.

[0020] In some embodiments, the aforementioned test method may further comprise receiving, by each WBR in the plurality of WBRs, a CLK signal, and each WBR may transmit the initial test signal under the control of the CLK signal.

[0021] In the boundary test circuits in according to the embodiments of this inventive concept, TCs added to the boundary test circuits may control phase switching of the read-time test signal output by each WBR. Thus each WBR may provide either an original signal or an inversed signal to the to-be-tested integrated circuit at different clock cycles. Therefore, the boundary test circuit can provide improved test efficiency and test flexibility.

[0022] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not necessarily restrictive to the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are incorporated in and constitute a part of the description, illustrate embodiments in accordance with this disclosure and, together with the description, serve to explain the disclosed inventive concept. It is apparent that these drawings present only some embodiments of the inventive concept and persons of ordinary skill in the art may obtain drawings of other embodiments from them without creative effort.

[0024] FIG. 1 is a schematic diagram of a boundary test circuit in accordance with one embodiment of this inventive concept.

[0025] FIG. 2 is a schematic diagram of a part of a boundary test circuit in accordance with one embodiment of this inventive concept.

[0026] FIG. 3 is a schematic diagram of a part of a boundary test circuit in accordance with one embodiment of this inventive concept.

[0027] FIG. 4 is a flowchart of a boundary test method in accordance with one embodiment of this inventive concept.

[0028] Numerals in the drawings:

[0029] 110-wrapper boundary register (WBR);

[0030] 120-toggle circuit (TC);

[0031] 210-NOT gate;

[0032] 220-first data selector;

[0033] 230-third data selector;

[0034] 240-second register;

[0035] 250-fourth data selector;

[0036] 310-first register;

[0037] 320-OR gate;

[0038] 330-exclusive-OR gate;

[0039] 340-second data selector.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0040] The embodiments will be described thoroughly and completely with reference to the accompanying drawings. However, the embodiments can be implemented in various forms, and should not be understood as being limited to the embodiments described herein. Instead, these embodiments are provided to make the present invention thorough and complete, and to fully convey

the concepts of the embodiments to those skilled in the art. Identical numerals in the drawings represent an identical or similar structure and thus the detailed descriptions thereof are omitted.

[0041] Although relative terms are used in the specification, for example, "on" and "under" are used to describe a relative relationship of one numeral component to another component, these terms used in the specification are merely for the convenience, for instance, according to an exemplary direction in the drawings. It is to be understood that if a numeral apparatus is inversed to turn upside down, a component described to be "on" will become a component to be "under". When a structure is "on" other structure, it may be indicated that the structure is integrally formed on the other structure, or indicated that the structure is "directly" disposed on the other structure, or indicated that the structure is "indirectly" disposed on the other structure via another structure.

[0042] Terms "a", "an", "one", "the", "said" and "at least one" are used to represent one or more elements/compositional portions etc. Terms "include", "including", "comprise", "comprising" , "has" and "having" are used to represent a meaning of open inclusion and refer to that another elements/compositional portions etc. may further be present besides the listed elements/compositional portions etc. The terms "first", "second", "third" etc. are merely used as numerals rather than limits to the number of objects thereof.

[0043] In an embodiment of this inventive concept, a boundary test circuit, configured to test an integrated circuit, is provided. The to-be-tested integrated circuit may be an independent chip that is encapsulated, and may also be a partial circuit unit that is not encapsulated into a chip. More specifically, in some embodiments, the integrated circuit may be a memory. When the to-be-tested integrated circuit is an independent chip, the boundary test circuit may be connected to I/O pins of the chip and perform data transmission. When the to-be-tested integrated circuit is an unencapsulated circuit unit, the boundary test circuit may be connected to a data channel of the circuit unit or a node for transmitting data, and perform data transmission. The detail composition and configuration of the to-be-tested integrated circuit is not specially limited in this inventive concept.

[0044] FIG. 1 is a schematic diagram of a boundary test circuit in accordance with one embodiment of this inventive concept. Referring to FIG. 1, the boundary test circuit may include a plurality of wrapper boundary registers (WBRs) 110 and a plurality of toggle circuits (TCs) 120. Each WBR 110 may be composed of registers, and each TC 120 may be configured to control of a state of a test signal.

[0045] In some embodiments, the WBRs 110 and the TCs 120 may be arranged sequentially and alternately, and may be serially connected stage by stage to form a complete test circuit. The number of the WBRs 110 may be the same as the number of the TCs 120, and each WBR 110 and each TC120 may form into a one-to-one corresponding connection relationship. In some embodiments, any other connection modes may be adopted by each WBR 110 and each TC 120. In addition, the

number of the WBRs 110 may also be different with the number of TCs 120. The connection relationship and numerical relationship of the WBRs 110 and the TCs 120 may be set according to the characteristics of the to-be-tested integrated circuit and actual test requirements, which are not specially limited in this disclosure.

[0046] Each WBR 110 may include a first I/O (Test Input) and a second I/O (Test Output). The first I/O (Test Input) may be configured to receive an initial test signal, and the second I/O (Test Output) may be configured to transmit the received initial test signal to a WBR 110 at a succeeding stage. The first I/O (Test Input) of a first-stage WBR 110 may be located at an initial end of the boundary test circuit and may be connected to a test instrument that sends the initial test signal. The second I/O (Test Output) of a last-stage WBR 110 may be located at a last end of the boundary test circuit and may also be connected to the test instrument that sends the initial test signal, thus forming a complete test loop. When a current stage WBR 110 transmits the initial test signal to a next stage WBR 110, the test signal may be directly transmitted to the next stage WBR 110 via a data channel between these two WBRs 110. Alternatively, the test signal may go through a TC between these two WBRs and be indirectly transmitted to the next stage WBR 110. The manner of test signal transmission between two WBRs 110 is not specially limited in this disclosure.

[0047] Referring to FIG. 1, each TC 120 may include an input for receiving the initial test signal stored in a corresponding WBR 110, a control I/O for receiving a toggle signal, and an output (e.g., Q0, Q1, Q2, Q3 shown in FIG. 1) for transmitting a real-time test signal to the to-be-tested integrated circuit. A phase of the real-time test signal may be identical to a phase of the initial test signal, and may also be an inverse of the phase of the initial test signal. The real-time test signal may, under the control of the received toggle signal, go through phase switching to obtain one of two states: one having a phase same as the phase of the initial test signal while the other having a phase inverse to the phase of the initial test signal. Additionally, the real-time test signal transmitted by each TC 120 may also go through the phase switching under the control of a CLK signal or any other trigger signal, which is not specially limited in this disclosure.

[0048] In the boundary test circuit of this embodiment, a plurality of TCs are added to the boundary test circuit. Each of the TCs may perform state switching (phase switching) on a real-time test signal output by each WBR, and, under the control of a relevant control signal, either an original test signal or an inversed test signal (a signal that has an inversed phase with the original test signal) can be output to the to-be-tested integrated circuit at different clock cycles. Therefore, the boundary test circuit can provide improved test efficiency and test flexibility.

[0049] The compositional components and test principles of the WBR 110 and the TC 120 will be described below with reference to FIGS. 2 and 3.

[0050] Referring to FIG. 2, in some embodiments, a TC 120 may include a NOT gate 210 and a first data selector 220. An input of the NOT gate 210 may be configured to receive the initial test signal stored in a corresponding WBR 110.

[0051] The first data selector 220 may include a first input, a second input, a control I/O and an output. A first input of the first data selector 220 may be connected to a same node as the input of the NOT gate 210, and may also be configured to receive the initial test signal stored in a corresponding WBR 110, a second input of the first data selector 220 may be connected to an output of the NOT gate 210, and may be configured to receive an output signal of the NOT gate 210. The control I/O of the first data selector 220 may be configured to receive a toggle signal, which may control a state selection of the first data selector 220. The output of the first data selector 220 may be configured to transmit a real-time test signal, which may be selected, based on the toggle signal received from the control I/O, from one of the two inputs of the first data selector 220.

[0052] For example, when the toggle signal is a first signal (e.g., a high level), the first data selector 220 may select the signal at the second input, thus the real-time test signal at the output of the first data selector 220 may have a phase that is inverse to the phase of the initial test signal. When the toggle signal is a second signal (e.g., a low level), the first data selector 220 may select the signal at the first input, thus the real-time test signal at the output of the first data selector 220 may have a phase that is identical to the phase of the initial test signal.

[0053] It is to be noted that the compositional components of a TC 120 disclosed in this embodiment is only exemplary, and other circuits may also be adopted to form a TC 120 to achieve the same effect as that described above.

[0054] Referring to FIG. 2, a WBR 110 may include: a third data selector 230, a second register 240 and a fourth data selector 250.

[0055] The third data selector 230 may include a first input configured to receive the initial test signal. The initial test signal may be transmitted directly from an external test instrument (when the WBR 110 is the first stage WBR located at the initial end of the boundary test circuit), and may also be transmitted directly from a previous stage WBR via a data transmission channel. In addition, the initial test signal may also be transmitted indirectly from the previous stage WBR via a TC located between the current WBR and the previous stage WBR. The third data selector 230 may include a control I/O configured to receive a Hold signal. The Hold signal may be configured to control the WBR 110 to enter or exit a Hold mode, thereby selecting an input signal from different inputs of the third data selector 230.

[0056] The second register 240 may have an input connected to an output of the third data selector 230, and configured to receive an output signal from the third data selector 230 after the third data selector 230 selects an input for receiving an input signal. The second register 240 may

further include an output configured to output the initial test signal stored thereon. The initial test signal may be output to a TC 120, as shown in FIG. 2, and may also be directly transmitted to a WBR at a succeeding stage through a data transmission channel. Additionally, the second register 240 may receive a CLK signal, under the control of which the initial test signal may be output.

[0057] The fourth data selector 250 may include a first input configured to receive a normal input signal (Normal Input), and a second input connected to the output of the second register 240 and configured to receive a signal output by the second register 240. The fourth data selector 250 may further include a control I/O configured to receive a Scan signal, which may be configured to control a WBR 110 to enter or exit a Scan mode, thereby selecting an input signal from different inputs of the fourth data selector 250. The fourth data selector 250 may further include an output configured to transmit a normal output signal (Normal Output). The output of the fourth data selector 250 may be further connected to the second input of the third data selector 230, so that the Normal Output signal may be transmitted to the third data selector 230 and be selected by the third data selector 230.

[0058] It is to be noted that the compositional components of a WBR 110 provided by this embodiment is exemplary only, and other circuits may also be adopted to form a WBR 110 to achieve the same effect as that described above.

[0059] FIG. 3 is a schematic diagram of a part of a boundary test circuit in accordance with one embodiment of this inventive concept. Referring to FIG. 3, in some embodiments, a TC 120 may include a first register 310, an OR gate 320, an XOR gate 330 and a second data selector 340.

[0060] The first register 310 may include an input configured to receive the initial test signal stored in a corresponding WBR 110. Additionally, the first register 310 may receive a CLK signal, under the control of which the initial test signal may be output.

[0061] In some embodiments, the TC 120 and the WBR 110 may share the same CLK, as shown FIG. 1 (in a dotted line connecting the CLK signal and the TC 120). In some embodiments, the TC 120 and the WBR 110 may have different CLK signals. Detail implementation is not specially limited in this disclosure.

[0062] The OR gate 320 may include a first input connected to an output of the first register 310, and configured to receive the initial test signal stored in the first register 310. The OR gate 320 may further include a second input configured to receive a toggle signal.

[0063] The XOR gate 330 may include a first input connected to the output of the first register 310, and configured to receive the initial test signal stored in the first register 310. The XOR gate 330 may further include a second input configured to receive the toggle signal.

[0064] The second data selector 340 may include a first input connected to an output of the OR gate 320 and configured to receive a signal output by the OR gate 320. The second data selector 340

may further include a second input connected to an output of the XOR gate 330 and configured to receive a signal output from the XOR gate 330. The second data selector 340 may further include a control I/O configured to receive the toggle signal, which may control a state selection of the second data selector 340. The second data selector 340 may further include an output configured to transmit a real-time test signal, which may be selected, based on the toggle signal received from the control I/O, from one of the two inputs of the second data selector 340.

[0065] For example, when the toggle signal is a first signal (e.g., a high level), the second data selector 340 may select the signal at the second input, thus the real-time test signal output at the output of the second data selector 340 may have a phase that is inverse to the phase of the initial test signal. When the toggle signal is a second signal (e.g., a low level), the second data selector 340 may select the signal at the first input, thus the real-time test signal output at the output of the second data selector 340 may have a phase that is identical to the phase of the initial test signal.

[0066] In this embodiment, the compositional components of a WBR 110 may be the same as those described in details in the WBRs 110 in the aforementioned embodiments, and thus will not be repeated herein. The compositional components of a TC 120 in this embodiment may be exemplary only, and other circuits may also be adopted to form the TCs 120 to achieve the same effect as those described above.

[0067] This inventive concept further provides a memory having a boundary test circuit. The boundary test circuit may be the boundary test circuit in any of the aforementioned embodiments, and may be configured to test the memory. Relevant composition and test principles of the boundary test circuit in this embodiment may be the same as those described in details in the aforementioned embodiments, and thus will not be repeated herein.

[0068] This inventive concept further provides a boundary test method based on the boundary test circuit or the memory in the aforementioned embodiments. The method may be configured for testing an integrated circuit.

[0069] FIG. 4 is a flowchart of a boundary test method in accordance with one embodiment of this inventive concept. Referring to FIG. 4, the method may include the following steps S410 and S420.

[0070] In step S410, each WBR may receive an initial test signal, and transmit the initial test signal to a WBR at a succeeding stage.

[0071] In this step, a boundary test circuit may first be set to be in a Scan mode using a Scan signal. Controlled by a plurality of control signals described in the aforementioned embodiments, the initial test signal may be transmitted to each WBR stage by stage. Then, the boundary test circuit may be set in a Hold mode using a Hold signal.

[0072] In step S420, each TC may receive the initial test signal stored in a corresponding WBR, and transmit a real-time test signal to a to-be-tested integrated circuit based on a toggle signal. The real-time test signal may have a phase that is either identical or inverse to a phase of the initial test signal.

[0073] In this step, under the control of the toggle signal, each TC may transmit the real-time test signal to the to-be-tested integrated circuit. The real-time test signal may have a phase that is either identical or inverse to the phase of the initial test signal. In other words, each TC may send an original signal or an inverse signal to the to-be-tested integrated circuit at different clock cycles. For example, when the toggle signal is a first signal (e.g., a high level), a signal having a phase identical to a phase of the initial test signal may be sent to the to-be-tested integrated circuit. When the toggle signal is a second signal (e.g., a low level), a signal having a phase inversed to the phase of the initial test signal may be sent to the to-be-tested integrated circuit.

[0074] In the boundary test method provided by the embodiments of this inventive concept, under the control of the toggle signal, the state switching (phase switching) can be performed by each TC on a real-time test signal output from each WBR. Under the control of related control signals, either an original test signal or a test signal with inversed phase may be output to the to-be-tested integrated circuit at different clock cycles. Therefore, the boundary test circuit can provide improved test efficiency and test flexibility.

[0075] Other embodiments of this inventive concept will be apparent to those skilled in the art based on the specification and practice of the embodiments disclosed here. This disclosure is intended to cover any variations, uses, or adaptations of this inventive concept following the general principles thereof and including such departures from this inventive concept as come within known or customary practice in the art. It is intended that the specification and embodiments be considered as exemplary only, with a true scope and spirit of this inventive concept being indicated by the appended claims.

CLAIMS

1. A boundary test circuit for testing an integrated circuit, comprising:

a plurality of serially-connected wrapper boundary registers (WBRs), each WBR comprising a first I/O for receiving an initial test signal, and a second I/O for transmitting the initial test signal to the WBR at a succeeding stage; and

a plurality of toggle circuits (TCs), each TC comprising an input for receiving the initial test signal stored in a corresponding WBR, a control I/O for receiving a toggle signal, and an output for transmitting a real-time test signal to the integrated circuit,

wherein a phase of the real-time test signal is either identical or inverse to a phase of the initial test signal.

2. The circuit of claim 1, wherein the toggle signal is configured to switching the phase of the real-time test signal.

3. The circuit of claim 1, wherein each TC comprises:

a NOT gate, comprising an input for receiving the initial test signal stored in a WBR; and

a first data selector, comprising a first input for receiving the initial test signal, a second input connected to an output of the NOT gate, a control I/O for receiving the toggle signal, and an output for transmitting the real-time test signal.

4. The circuit of claim 1, wherein each TC comprises:

a first register, comprising an input for receiving the initial test signal stored in a WBR;

an OR gate, comprising a first input connected to an output of the first register, and a second input for receiving the toggle signal;

an XOR gate, comprising a first input connected to the output of the first register, and a second input for receiving the toggle signal; and

a second data selector, comprising a first input connected to an output of the OR gate, a second input connected to an output of the XOR gate, a control I/O for receiving the toggle signal, and an output for transmitting the real-time test signal.

5. The circuit of claim 1, wherein each TC is configured to transmit the real-time test signal under the control of a CLK signal.

6. The circuit of claim 1, wherein each WBR comprises:

a third data selector, comprising a first input for receiving the initial test signal, and a control I/O for receiving a Hold signal;

a second register, comprising an input connected to an output of the third data selector, and an output for outputting the initial test signal stored in the second register; and

a fourth data selector, comprising a first input for receiving a Normal input, a second input connected to the output of the second register, a control I/O for receiving a Scan signal, and an output for transmitting the Normal output, and the output of the fourth data selector being connected to a second input of the third data selector.

7. The circuit of claim 6, wherein each WBR is configured to transmit the initial test signal under the control of a CLK signal.

8. The circuit of claim 1, wherein the integrated circuit is a memory.

9. A boundary test method for testing an integrated circuit, comprising:

receiving, by each wrapper boundary register (WBR) in a plurality of serially-connected WBRs, an initial test signal, wherein each WBR transmits the initial test signal to the WBR at a succeeding stage; and

receiving, by each toggle circuit (TC) in a plurality of TCs, the initial test signal stored in a corresponding WBR, wherein the TC transmits a real-time test signal to the integrated circuit according to a toggle signal,

wherein a phase of the real-time test signal is either identical or inverse to a phase of the initial test signal.

10. The method of claim 9, wherein the toggle signal is configured to switching the phase of the real-time test signal.

11. The method of claim 9, further comprising:

receiving, by each TC in the plurality of TCs, a CLK signal, wherein each TC transmits the real-time test signal under the control of the CLK signal.

12. The method of claim 9, further comprising:

receiving, by each WBR in the plurality of WBRs, a CLK signal, wherein each WBR transmits the initial test signal under the control of the CLK signal.

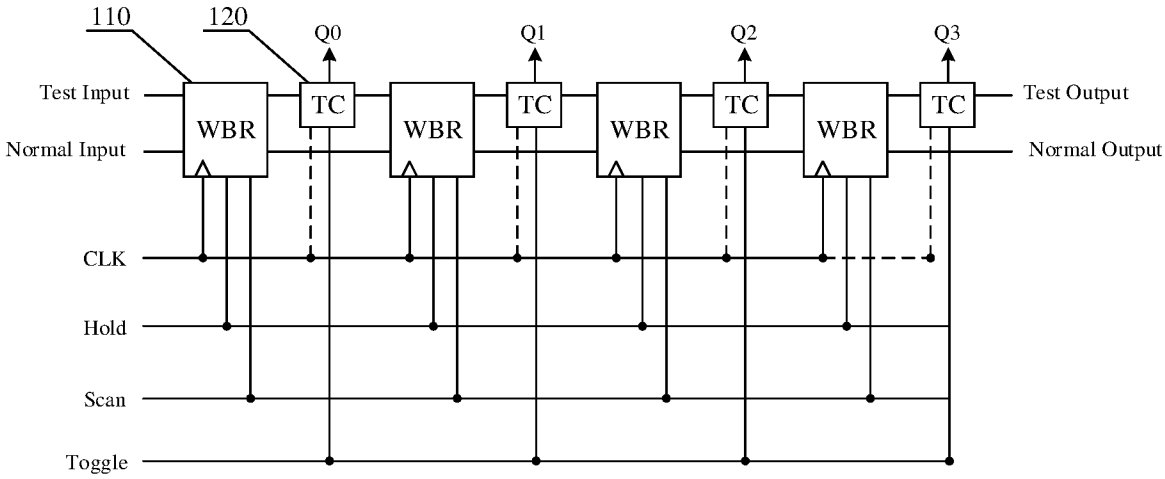

110
120
Q0
Q1
Q2
Q3
Test Input
Normal Input
WBR
TC
Test Output
Normal Output
CLK
Hold
Scan
Toggle

FIG. 1

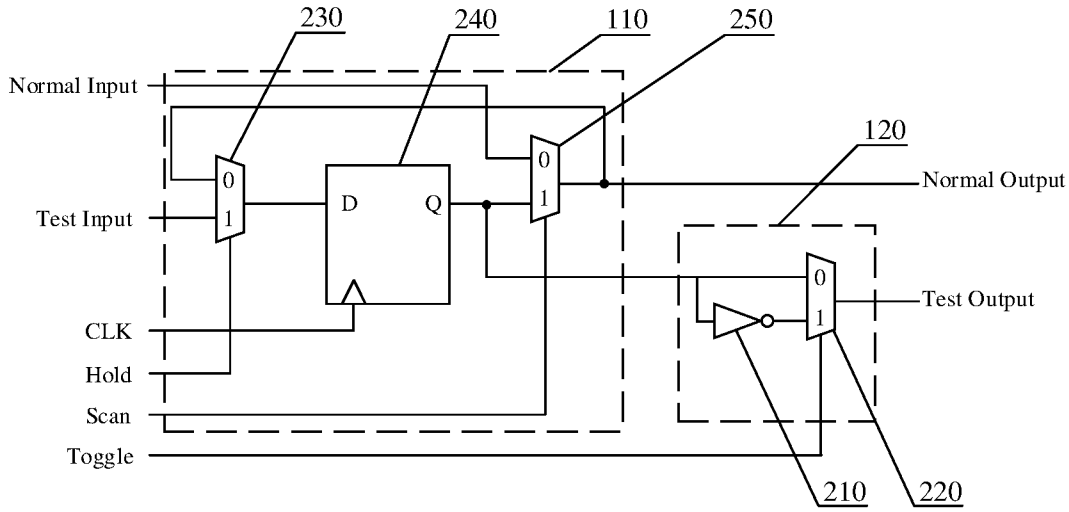

230
240
110
250
120
Normal Input
Test Input
CLK
Hold
Scan
Toggle
0
1
D
Q
Normal Output
Test Output
210
220

FIG. 2

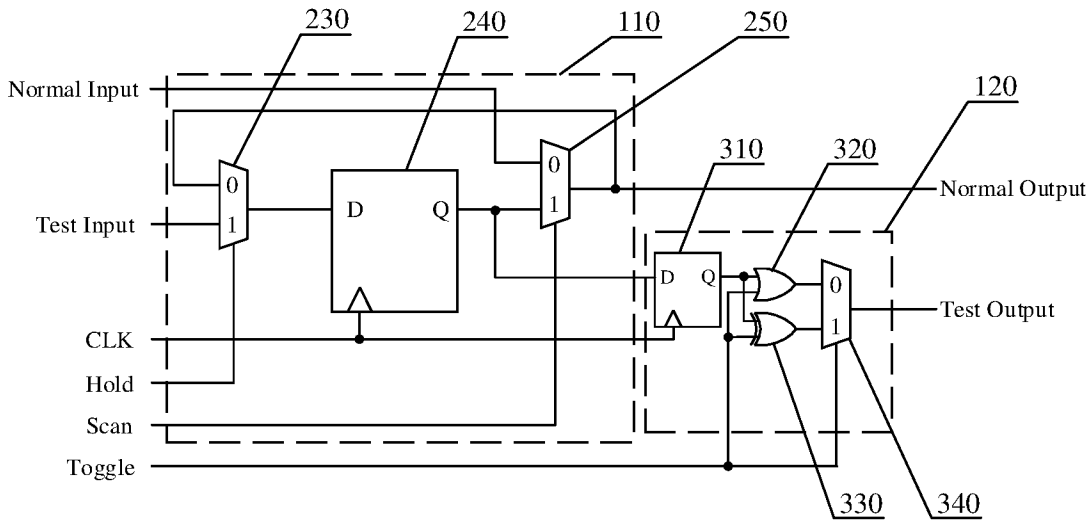

230
240
110
250
120
Normal Input
Test Input
CLK
Hold
Scan
Toggle
0
1
D
Q
310
320
Normal Output
Test Output
330
340

FIG. 3

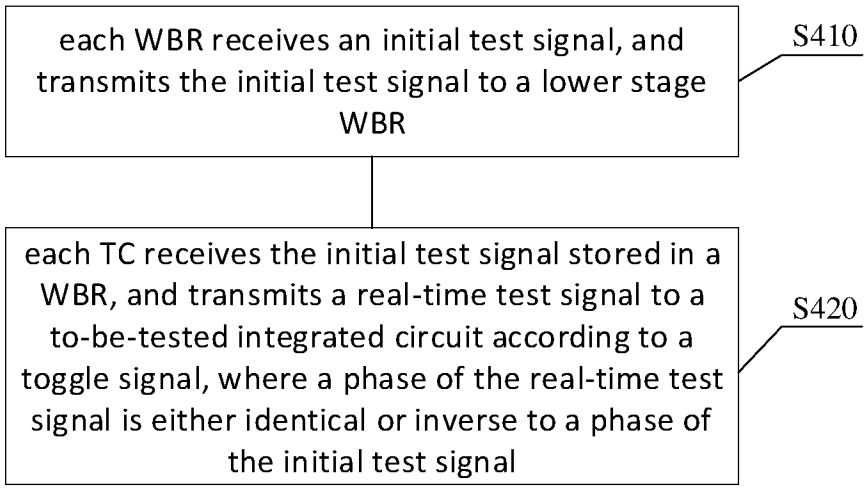

each WBR receives an initial test signal, and transmits the initial test signal to a lower stage WBR
S410
each TC receives the initial test signal stored in a WBR, and transmits a real-time test signal to a to-be-tested integrated circuit according to a toggle signal, where a phase of the real-time test signal is either identical or inverse to a phase of the initial test signal
S420

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/102123

A. CLASSIFICATION OF SUBJECT MATTER

G11C 29/56(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT;WPI;EPODOC;BAIDU;CNKI;ISI: boundary, test, register, toggle, control, signal, inverse, NOT gate, XOR gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 109192240 A (CHANGXIN MEMORY TECHNOLOGIES, INC.) 11 January 2019 (2019-01-11) claims 1-10, description, paragraphs [0062]-[0075], figures 2 and 3	1-12
PX	CN 208596549 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 12 March 2019 (2019-03-12) claims 1-8, description, paragraphs [0062]-[0075], figures 2 and 3	1-12
A	US 5648973 A (AST RESEARCH INC.) 15 July 1997 (1997-07-15) description, column 3, line 2 to column 4, line 4 and figure 2	1-12
A	CN 107340467 A (BEIJING ZHAOXIN ELECTRONICS TECHNOLOGY CO., LTD.) 10 November 2017 (2017-11-10) the whole document	1-12
A	US 2008244343 A1 (GREALISH JAMES ET AL.) 02 October 2008 (2008-10-02) the whole document	1-12
A	CN 102419415 A (BEIJING MXTRONICS CO., LTD. ET AL.) 18 April 2012 (2012-04-18) the whole document	1-12

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 October 2019	**07 November 2019**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088** **China**	**ZHANG,Linlin**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961404**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/102123

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				EP	0880708	A1	02 December 1998
				RU	2163023	C2	10 February 2001
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				KR	19990072031	A	27 September 1999
				IL	124556	A	14 June 2001
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CN	102419415	A	18 April 2012	CN	102419415	B	02 July 2014