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(54) **Title:** FABRICATION TECHNIQUES AND STRUCTURES FOR GETTERING MATERIALS IN ULTRASONIC TRANSDUCER CAVITIES

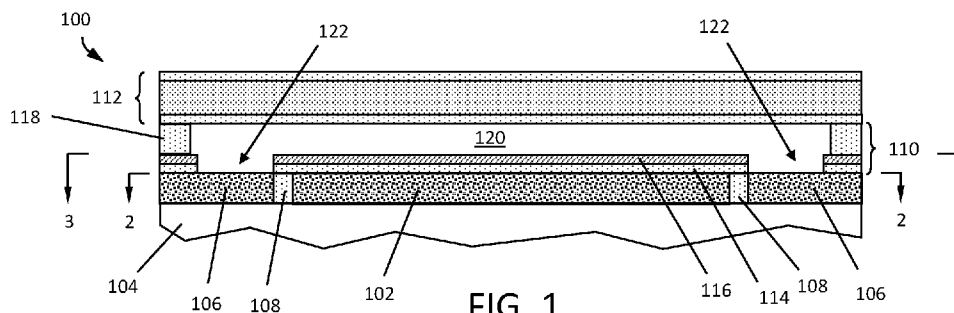


FIG. 1

(57) **Abstract:** A method of forming an ultrasound transducer device includes bonding a membrane to a substrate so as to form a sealed cavity between the membrane and the substrate. An exposed surface located within the sealed cavity includes a getter material that is electrically isolated from a bottom electrode of the cavity.



**FABRICATION TECHNIQUES AND STRUCTURES FOR GETTERING
MATERIALS IN ULTRASONIC TRANSDUCER CAVITIES**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit under 35 U.S.C. § 119(e) of U.S. Patent Application Serial No. 62/738,502, filed September 28, 2018 under Attorney Docket No. B1348.70103US00, and entitled “FABRICATION TECHNIQUES AND STRUCTURES FOR GETTERING MATERIALS IN ULTRASONIC TRANSDUCER CAVITIES,” which is hereby incorporated herein by reference in its entirety.

FIELD

[0002] The present disclosure relates generally to micromachined ultrasound transducers and, more specifically, to fabrication techniques and associated structures for gettering materials present in ultrasound transducer cavities during manufacture.

BACKGROUND

[0003] Ultrasound devices may be used to perform diagnostic imaging and/or treatment, using sound waves with frequencies that are higher with respect to those audible to humans. Ultrasound imaging may be used to see internal soft tissue body structures, for example to find a source of disease or to exclude any pathology. When pulses of ultrasound are transmitted into tissue (e.g., by using a probe), sound waves are reflected off the tissue with different tissues reflecting varying degrees of sound. These reflected sound waves may then be recorded and displayed as an ultrasound image to the operator. The strength (amplitude) of the sound signal and the time it takes for the wave to travel through the body provide information used to produce the ultrasound images.

[0004] Some ultrasound imaging devices may be fabricated using micromachined ultrasound transducers, including a flexible membrane suspended above a substrate. A cavity is located between part of the substrate and the membrane, such that the combination of the substrate, cavity and membrane form a variable capacitor. When actuated by an appropriate electrical signal, the membrane generates an ultrasound signal by vibration. In response to

receiving an ultrasound signal, the membrane is caused to vibrate and, as a result, an output electrical signal can be generated.

SUMMARY

[0005] In one aspect, a method of forming an ultrasound transducer device includes bonding a membrane to a substrate so as to form a sealed cavity therebetween, wherein an exposed surface located within the sealed cavity comprises a getter material, the getter material being electrically isolated from a bottom electrode of the cavity.

[0006] In another aspect, an ultrasound transducer device includes a membrane bonded to a substrate with a sealed cavity therebetween. An exposed surface located within the sealed cavity includes a getter material, the getter material being electrically isolated from a bottom electrode of the cavity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0008] FIG. 1 is a cross-sectional view of a micromachined ultrasound transducer having a cavity getter material, in accordance with an embodiment.

[0009] FIG. 2 is a top view of the ultrasound transducer of FIG. 1, taken along the arrows 2-2.

[0010] FIG. 3 is a top view of the ultrasound transducer of FIG. 1, taken along the arrows 3-3.

[0011] FIG. 4 is a cross-sectional view of a micromachined ultrasound transducer having a cavity getter material, in accordance with another embodiment.

[0012] FIG. 5 is a top view of the ultrasound transducer of FIG. 4, taken along the arrows 5-5.

[0013] FIG. 6 is a top view of the ultrasound transducer of FIG. 4, taken along the arrows 6-6.

[0014] FIG. 7 is a cross-sectional view of a micromachined ultrasound transducer having a cavity getter material, in accordance with another embodiment.

[0015] FIG. 8 is a top view of the ultrasound transducer of FIG. 7, taken along the arrows 8-8.

[0016] FIG. 9 is a top view of the ultrasound transducer of FIG. 7, taken along the arrows 9-9.

[0017] FIGS. 10-19 illustrate a process flow sequence for forming the ultrasound transducer embodiments of FIGS. 1-9, in which:

[0018] FIG. 10 illustrates the formation of an electrode layer over a CMOS substrate.

[0019] FIG. 11-1 illustrates patterning of the electrode layer of FIG. 10 according to the embodiment of FIG. 1.

[0020] FIG. 11-2 illustrates patterning of the electrode layer of FIG. 10 according to the embodiment of FIG. 4.

[0021] FIG. 11-3 illustrates patterning of the electrode layer of FIG. 10 according to the embodiment of FIG. 7.

[0022] FIG. 12-1 illustrates forming an insulation layer over the structure of FIG. 11-1.

[0023] FIG. 12-2 illustrates forming an insulation layer over the structure of FIG. 11-2.

[0024] FIG. 12-3 illustrates forming an insulation layer over the structure of FIG. 11-3.

[0025] FIG. 13-1 illustrates planarizing the insulation layer of the structure of FIG. 12-1.

[0026] FIG. 13-2 illustrates planarizing the insulation layer of the structure of FIG. 12-2.

[0027] FIG. 13-3 illustrates planarizing the insulation layer of the structure of FIG. 12-3.

- [0028] FIG. 14 illustrates forming an insulation stack over the structure of FIG. 13-1.
- [0029] FIG. 15 illustrates forming a cavity in the insulation stack.
- [0030] FIG. 16 illustrates removing a portion of the lower insulation layers of the insulation stack to expose adjacent electrode material that serves as a getter material.
- [0031] FIG. 17 illustrates a silicon-on-insulator (SOI) wafer to be bonded to the structure of FIG. 16.
- [0032] FIG. 18 illustrates the SOI wafer bonded to the structure of FIG. 16.
- [0033] FIG. 19 illustrates removing a portion of the SOI wafer to define a membrane of a micromachined ultrasound transducer.
- [0034] FIG. 20 illustrates a top view of an example ultrasound transducer device formed using any of the process flow sequences described herein.

DETAILED DESCRIPTION

[0035] One type of transducer suitable for use in ultrasound imaging devices is a micromachined ultrasound transducer (MUT), which can be fabricated from, for example, silicon and configured to transmit and receive ultrasound energy. MUTs may include capacitive micromachined ultrasound transducers (CMUTs) and piezoelectric micromachined ultrasound transducers (PMUTs), which can offer several advantages over more conventional ultrasound transducer designs such as, for example, lower manufacturing costs and fabrication times and/or increased frequency bandwidth. With respect to the CMUT device, the basic structure is a parallel plate capacitor with a rigid bottom electrode and a top electrode residing on or within a flexible membrane. Thus, a cavity is defined between the bottom and top electrodes. In some designs (such as those produced by the assignee of the present application for example), the CMUT transducer may be directly integrated on an integrated circuit that controls the operation of the transducer. One way of manufacturing a CMUT ultrasound device is to bond a membrane substrate to an integrated circuit substrate, such as a complementary metal oxide semiconductor (CMOS) substrate. This may be

performed at temperatures sufficiently low to prevent damage to the devices of the integrated circuit.

[0036] However, during bonding of the membrane substrate to the CMOS substrate, there may be a difference in cavity pressures across the die and wafer due to the water vapor and other gaseous byproducts and the propagation of the bond. This in turn may result in undesired variability of certain CMUT-based operating parameters such as for example, collapse voltage, as well as transmit/receive pressure sensitivity. Accordingly, it is desirable to be able to control cavity pressure within such a transducer device during the manufacturing process, as well as over the lifetime of the device.

[0037] Referring now to FIG. 1, there is shown a cross-sectional view of a micromachined ultrasound transducer 100 having a cavity getter material, in accordance with an embodiment. As is shown, the ultrasound transducer 100 includes a lower electrode 102 formed over a substrate 104 (e.g., a CMOS substrate, such as silicon). The CMOS substrate 104 may include, but is not necessarily limited to, CMOS circuits, wiring layers, redistribution layers, and insulation/passivation layers. In an exemplary embodiment, suitable materials for the lower electrode 102 include one or more of titanium (Ti), zirconium (Zr), vanadium (V), cobalt (Co), nickel (Ni), as well as alloys thereof.

[0038] As further shown in FIG. 1, the lower electrode 102 is electrically isolated from adjacent metal regions 106 that are also formed on the substrate 104. Exposed portions of the adjacent metal regions 106 may thus serve as a getter material during cavity formation. The adjacent metal regions 106 may be formed from a same metal material as the lower electrode 102, and are electrically isolated from the lower electrode 102 by an insulator material 108 (e.g., silicon oxide). By way of further illustration, FIG. 2 is a top down view of the lower electrode, adjacent metal regions 106 and insulator material 108, taken along the arrows 2-2 in FIG. 1. It should be appreciated that although the exemplary geometric structure of this portion of the ultrasound transducer 100 is generally circular in shape, other configurations are also contemplated such as for example, rectangular, hexagonal, octagonal, and other multi-sided shapes, etc.

[0039] Referring again to FIG. 1, an insulator layer (e.g., one or more individual insulator layers, such as an insulator stack 110) is formed over the lower electrode 102 and portions of adjacent metal regions 106. Portions of the stack 110 provide support for a moveable membrane 112 (e.g., an SOI wafer having a doped silicon device layer with an oxidized surface) bonded to the stack 110. In the illustrated embodiment, the insulator stack 110 includes a first oxide layer 114 (e.g., chemical vapor deposition (CVD) silicon oxide), a second oxide layer 116 (e.g., atomic layer deposition (ALD) aluminum oxide) and a third oxide layer 118 (e.g., sputter deposited silicon oxide). By suitable lithographic patterning and etching of the third oxide layer 118, a cavity 120 may be defined for the ultrasound transducer 100. Further, in embodiments where the second oxide layer 116 is chosen from a material having an etch selectivity with respect to the third oxide layer 118, the second oxide layer 116 may serve as an etch stop for removing portions of the third oxide layer 118 in order to define the cavity 120.

[0040] In addition to the etch of the third oxide layer that defines the cavity 120, another etch is used to define openings 122 through the second oxide layer 116 and first oxide layer 114, thereby exposing a top surface of a portion of metal regions 106. A top down view of the cavity 120, illustrating remaining portions of the second oxide layer 116 and the exposed portions of metal regions is illustrated in FIG. 3, taken along the arrows 3-3 in FIG. 1. The exposed portions of metal regions 106 may advantageously serve as a getter material of one or more gases present during a bonding operation of the membrane 112 to seal the cavity 120. Additional exemplary processing operations used in forming the ultrasound transducer 100 are discussed hereinafter.

[0041] It will be appreciated that the gettering technique and associated removal of a portion of oxide layers 116 and 114 to expose a portion of metal regions 106 can be implemented in conjunction with any of a number of transducer electrode structures. For example, FIGs. 4-6 illustrate a cross-sectional and top down views of a micromachined ultrasound transducer 400 having a cavity getter material, in accordance with another embodiment. For ease of description, like elements are designated by like reference numerals in the various embodiments. As particularly illustrated in FIG. 4 and in FIG. 5 (taken along the lines 5-5 in FIG. 4) the lower electrode 102 is formed so as to have a “donut” pattern; that

is, a region corresponding to the innermost radius of the electrode structure of the earlier described embodiment is instead formed from an insulating material (e.g., oxide 108) rather than the conductive electrode material. It will be noted that since oxide layers 116 and 114 are only removed from the outer region of the cavity geometry, the top down view of FIG. 6 is substantially similar to that of the embodiment of FIG. 3.

[0042] The electrode geometry of FIG. 4 may be employed in various operating modes, including in conjunction with a collapse mode of operation of the ultrasound transducer 400, where at least a part of the membrane 112 comes into physical contact with a bottom surface of the cavity 120 (for example, second oxide layer 116). In this case, substituting a central portion of the lower electrode material with an insulator material can help to reduce parasitic capacitance of the ultrasound transducer 400 without significantly compromising performance, as the central portion of the electrode in physical contact with the bottom of the ultrasound transducer cavity has a minimum contribution to the production of ultrasonic signals. Still a further benefit to such an electrode structure may be the reduction of charging on the membrane 112 otherwise caused by repeated collapsing. Additional information regarding a donut shaped lower electrode may be found in U.S. Patent Application Serial No. 62/666,643, filed May 3, 2018 and assigned to the assignee of the present application, and in co-pending U.S. Patent Application Serial No. 16/401,630, filed May 2, 2019 and assigned to the assignee of the present application, the contents of both of which are incorporated by reference herein in their entireties.

[0043] Referring now to FIGs. 7-9, there is illustrated a cross-sectional and top down views of a micromachined ultrasound transducer 700 having a cavity getter material, in accordance with still another embodiment. Again, for ease of description, like elements are designated by like reference numerals in the various embodiments. As particularly illustrated in FIG. 7 and in FIG. 8 (taken along the lines 8-8 in FIG. 7) the lower electrode 102 is still formed so as to have a “donut” pattern. However, in contrast to the embodiment of FIGs. 4-6, an additional electrode 702 is formed at the central portion of the cavity region. The electrode 702 is patterned to be electrically isolated from lower electrode 102, such as by being insulated therefrom by oxide 108 for example. As is the case with the other

embodiments, the top down view of FIG. 9 is substantially similar to that of the embodiments of FIG. 3 and FIG. 6.

[0044] An electrode geometry of the type shown in FIG. 7, in addition to the benefits described with respect to the previous embodiment, can also contribute to a bypass capacitance between the membrane 112 and ground, which in turn may contribute to noise reduction on the voltage of the membrane 112. Another benefit of electrode 702 may be to help provide for a lower collapse voltage for the ultrasound transducer 700 by way of the electrode 702 attracting the membrane 112 toward the bottom of the cavity 120. Additional information regarding this electrode design may also be found in the aforementioned co-pending U.S. Patent Applications Serial Nos. 62/666,643 and 16/401,630.

[0045] Referring generally now to FIGs. 10-19, there is shown an exemplary process flow sequence for forming the ultrasound transducer embodiments described above. In FIG. 10, an electrode layer 1000 is formed over CMOS substrate 104, such as a silicon substrate for example. Again, the CMOS substrate 104 may include, but is not necessarily limited to, CMOS circuits, wiring layers, redistribution layers, and insulation/passivation layers. As also mentioned previously, suitable materials for the electrode layer 1000 include one more of titanium (Ti), zirconium (Zr), vanadium (V), cobalt (Co), nickel (Ni), as well as alloys thereof.

[0046] Depending on the specific lower electrode pattern desired, the process may proceed to any of FIGs. 11-1, 11-2 or 11-3. For example, in FIG. 11-1, a photolithographic process is used to pattern and etch openings into the electrode layer 1000 so as to define the electrode pattern of FIG. 1, namely a lower electrode 102 and adjacent metal regions 106. In this particular embodiment, a center region of the lower electrode 102 remains intact. FIG. 11-2 illustrates the patterning of the electrode layer 1000 of the FIG. 4 embodiment (i.e., center portion of electrode removed to define a “donut” pattern), and FIG. 11-3 illustrates the patterning of the electrode layer 1000 of the FIG. 7 embodiment (i.e., formation of the additional electrode 702 at the center portion of the donut pattern).

[0047] Once the electrode pattern is defined, the process may then proceed to an insulation fill operation as illustrated in FIGs. 12-1, 12-2 and 12-3. As shown, an insulation

layer 1200 (e.g., silicon oxide) is formed over the patterned electrode material. The insulation layer 1200 is then planarized as respectively shown in FIGs. 13-1, 13-2 and 13-3 to form the insulator material 108 described above. From this point, processing for each of the illustrated electrode design embodiments is substantially the same. Accordingly, the remaining figures are illustrated in the context of the first embodiment only (i.e., from FIG. 13-1) for conciseness, although it should be understood that the subsequent processes are equally applicable to the other embodiments.

[0048] Referring now to FIG. 14, an insulator stack 110 as described above is formed over the lower electrode layer, such as the lower electrode 102 and adjacent metal regions 106 illustrated in FIG. 13-1. In the illustrated embodiment, the insulator stack 110 includes a first oxide layer 114 (e.g., CVD silicon oxide having a thickness of about 1-100 nm) formed over the lower electrode 102 and adjacent metal regions 106, a second oxide layer 116 (e.g., ALD aluminum oxide having a thickness of about 5-100 nm) formed over the first oxide layer 114, and a third oxide layer 118 (e.g., sputter deposited silicon oxide having a thickness of about 1-300 nm) formed over the second oxide layer 116.

[0049] In FIG. 15, a first lithographic patterning and etch process is performed to define the cavity 120 by removing a portion of the third oxide layer 118, using the second oxide layer 116 as an etch stop. As an added benefit, aluminum oxide material of the second oxide layer 116 present at the bottom of the cavity 1500 may also help to reduce charging of a (subsequently formed) top membrane in the event the top membrane comes into contact with the second oxide layer 116 during device operation (e.g., such as during a collapse mode of transducer operation). Optionally, a thin layer of aluminum oxide (not shown) and also a thin self-assembled monolayer (SAM) with a heptadecafluoro tetrahydrodecyl trichlorosilane or dodecyltrichlorosilane precursor (not shown) may be formed on the second oxide layer 116 after patterning and before photoresist removal. A SAM formed at the bottom of the cavity 120 may help to reduce any stiction of the top membrane to the bottom of the cavity 120 in the aforementioned collapse mode of operation or other mode where the top membrane comes in physical contact with the bottom of the cavity 120. It should further be appreciated at this point that although the illustrated embodiments depict a single cavity, any suitable

number of cavities and corresponding electrode structures may be formed (e.g., hundreds, thousands, tens of thousands, etc.)

[0050] Referring now to FIG. 16, a second lithographic patterning and etch process is performed to expose the adjacent metal regions 106 at the outer perimeter of the cavity 120. The second etch removes a portion of the second oxide layer 116 and first oxide layer 114, stopping on the adjacent metal regions 106, which will serve as a getter material. At this point, the device as depicted in FIG. 16 is prepared for membrane bonding. A particular size or size range of the opening(s) formed through the second oxide layer 116 and first oxide layer 114 (and thus the resulting amount of adjacent metal region material to be exposed) may be chosen based on one or more calculations on how much gas needs to be consumed/gettered during the bonding process. In addition, a determination of how much getter material area to be formed in each cavity may depend on factors such as for example, how much gas is released during the bonding process, the device lifetime, and the desirable cavity pressure after the getter is activated. Final pressure may be adjusted by getter activation, which in turn may be accomplished by annealing at elevated temperatures. In embodiments, it is generally preferable to have more exposed getter material than a targeted amount, rather than less exposed getter material than the target amount, since the annealing time could be shortened with the extra getter material. By way of example only, for a transducer cavity having a cross sectional area of about 0.030 cm^2 , an example range of getter material area within this cavity for effective gettering maybe about $1 \times 10^{-4} \text{ cm}^2$ to about $2.5 \times 10^{-4} \text{ cm}^2$. In embodiments, it may be desirable to build in a further margin for getter material exposure to allow for process variations and calculated getter efficiency. Thus, for this specific example shown in FIG. 16, an inner radius r_1 of the getter material (metal regions 106) is about 83 microns (μm), an outer radius r_2 of the getter material is about 96 microns μm , and a transducer cavity radius r_3 is about 98 μm . With a circular cavity configuration, the resulting getter area is about $7.3 \times 10^{-3} \text{ cm}^2$, which is roughly an order of magnitude more than an exemplary calculated range needed for a desired gettering capability. Again, it should be appreciated that these values are exemplary only and the disclosure is not limited to such values and ranges.

[0051] As shown in FIG. 17, a substrate 1700 (e.g., a silicon-on-insulator (SOI) substrate) includes a handle layer 1702 (e.g., a silicon layer), a buried oxide (BOX) layer 1704, and a silicon device layer 1706. An oxide layer 1708 may optionally be provided on a backside of the handle layer 1702. The silicon device layer 1706 may be formed from single crystal silicon and may be doped in some embodiments. Such doping may be highly doped P-type or, alternatively N-type, and may be uniform through the silicon device layer 1706 or patterned by implantation in certain regions. In addition, an oxide layer 1710 (e.g., a thermal silicon oxide) is formed on the silicon device layer 1706.

[0052] As shown in FIG. 18, the substrate 1700 is bonded to the substrate 104 and the aforementioned structures formed on the substrate 104. In the embodiment depicted, the oxide material of layer 1710 is bonded to the oxide material 118 by low temperature oxide bonding methods (e.g., below 450°C), which may prevent damage to circuitry of the substrate 104. As stated above, there may be a difference in cavity pressures across the die and wafer due to H₂O based byproducts and the propagation of the bond. Because the metal surface of the adjacent metal regions 106 is exposed during bonding of the substrate 1700, the metal is able to consume gases such as oxygen, nitrogen, argon, water vapor, etc., resulting in a more uniform pressure across the various cavities 120 of the ultrasound device.

[0053] After bonding, the oxide layer 1708 and the handle layer 1702 are removed by a suitable technique (e.g., etching, grinding, etc.), thereby defining the membrane 112 discussed above and as illustrated in FIG. 19. Optionally, the BOX layer 1704 may also be removed prior to additional processing, which may include suitable steps to complete final wiring, interconnect and/or packaging steps used to produce an ultrasound device.

[0054] FIG. 20 illustrates a top view of an example ultrasound transducer device 2000 formed using any of the process flow sequences described herein. As illustrated, the transducer device includes an array of individual transducers 100, such as those described above. The specific number of transducers 100 shown in FIG. 20 should not be construed in any limiting sense, and may include any number suitable for a desired imaging application, which may be for example on the order of tens, hundreds, thousands, tens of thousands or more. It will be appreciated the above described gettering techniques are particularly beneficial with an increasing larger array, given the ability to provide a uniform cavity

pressure across a wafer or die. FIG. 20 further illustrates an example location of metal 2002 that may distribute an electrical signal to the membranes (upper electrodes) of the transducers 100.

[0055] It should be appreciated that although the exemplary embodiments illustrate and describe a same bottom electrode metal material used as a getter material during membrane bonding, other non-metallic or non-metallic alloy getter materials may also be used in a similar manner. For example, graphite, phosphorous and/or certain salts may serve as a cavity getter material. Moreover, with respect to the specific placement of a getter material, other locations in addition to a cavity bottom are also contemplated. For example, with additional processing operations, layers may be formed in a manner so as to have getter material disposed on cavity sidewalls and/or the membrane itself (top of sealed cavity) for gettering during membrane bonding. Such additional getter layer(s) may also be formed at a different level than the bottom electrode material.

[0056] The above-described embodiments can be implemented in any of numerous ways. For example, the embodiments may be implemented using hardware, software or a combination thereof. When implemented in software, the software code can be executed on any suitable processor (e.g., a microprocessor) or collection of processors, whether provided in a single computing device or distributed among multiple computing devices. It should be appreciated that any component or collection of components that perform the functions described above can be generically considered as one or more controllers that control the above-discussed functions. The one or more controllers can be implemented in numerous ways, such as with dedicated hardware, or with general purpose hardware (e.g., one or more processors) that is programmed using microcode or software to perform the functions recited above.

[0057] Various aspects of the present application may be used alone, in combination, or in a variety of arrangements not specifically discussed in the embodiments described in the foregoing and is therefore not limited in its application to the details and arrangement of components set forth in the foregoing description or illustrated in the drawings. For example, features described in one embodiment may be combined in any manner with features described in other embodiments.

[0058] Also, certain aspects may be embodied as a method, of which an example has been provided. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0059] Use of ordinal terms such as “first,” “second,” “third,” etc., in the claims to modify a claim element does not by itself connote any priority, precedence, or order of one claim element over another or the temporal order in which acts of a method are performed, but are used merely as labels to distinguish one claim element having a certain name from another element having a same name (but for use of the ordinal term) to distinguish the claim elements.

[0060] The terms “approximately” and “about” may be used to mean within $\pm 20\%$ of a target value in some embodiments, within $\pm 10\%$ of a target value in some embodiments, within $\pm 5\%$ of a target value in some embodiments, and yet within $\pm 2\%$ of a target value in some embodiments. The terms “approximately” and “about” may include the target value.

CLAIMS

What is claimed is:

1. A method of forming an ultrasound transducer device, the method comprising:

bonding a membrane to a substrate so as to form a sealed cavity therebetween;

wherein an exposed surface located within the sealed cavity comprises a getter material, the getter material being electrically isolated from a bottom electrode of the cavity.
2. The method of 1, wherein the exposed surface comprises a top surface of the substrate.
3. The method of claim 1, wherein the getter material comprises a same material as a bottom electrode of the cavity.
4. The method of claim 1, wherein the getter material comprises one or more of: titanium, zirconium, vanadium, cobalt, nickel, and alloys thereof.
5. The method of claim 4, further comprising removing one or more insulating layers from the getter material.
6. The method of claim 5, wherein the getter material is disposed at an outer perimeter of the cavity.
7. The method of claim 5, wherein the cavity is circular shaped and the getter material is disposed at an outer radius of the cavity.
8. The method of claim 1, wherein the getter material is configured to remove one or more of oxygen, nitrogen, argon, or water vapor from the cavity.
9. An ultrasound transducer device, comprising:

a membrane bonded to a substrate with a sealed cavity therebetween;

wherein an exposed surface located within the sealed cavity comprises a getter material, the getter material being electrically isolated from a bottom electrode of the cavity.

10. The device of claim 9, wherein the exposed surface comprises a top surface of the substrate.

11. The device of claim 9, wherein the getter material comprises one or more of: titanium, zirconium, vanadium, cobalt, nickel, and alloys thereof.

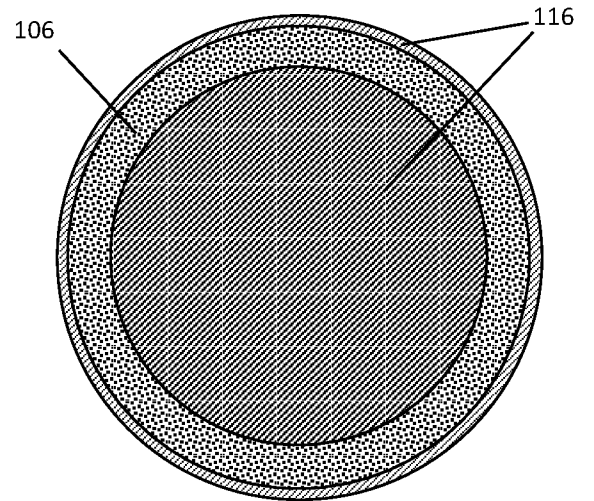
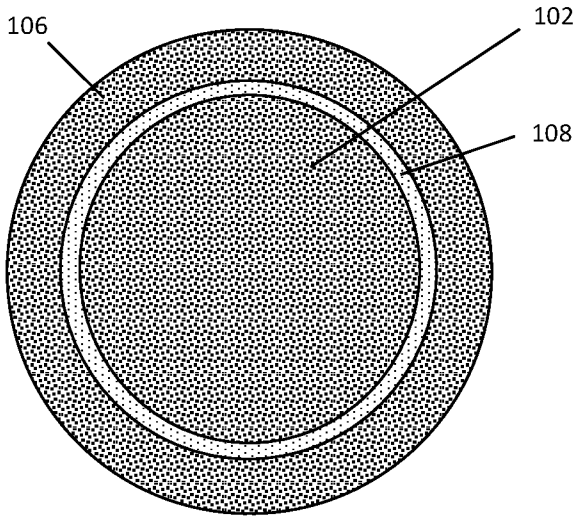
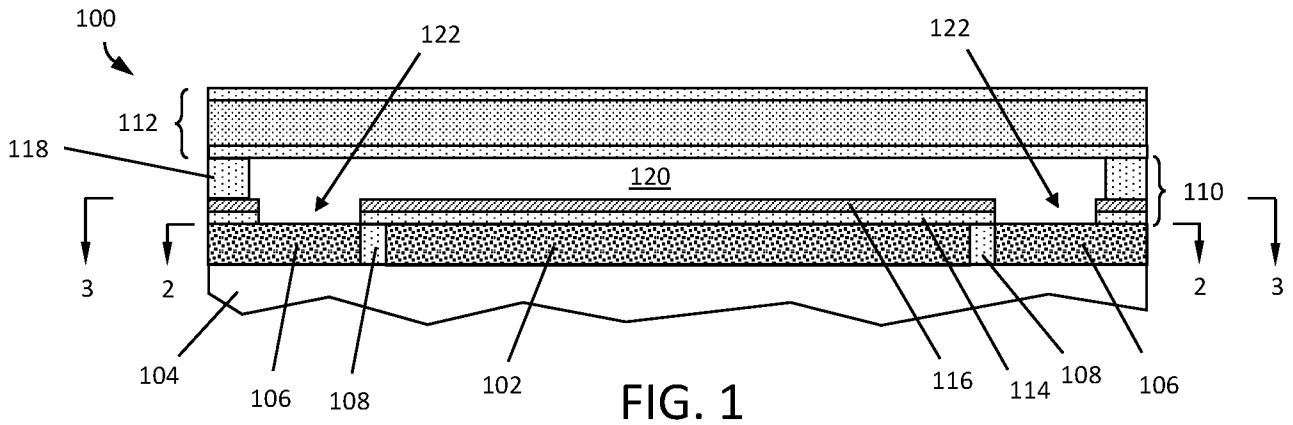
12. The device of claim 11, further comprising one or more insulating layers formed over the bottom electrode but not present over the getter material.

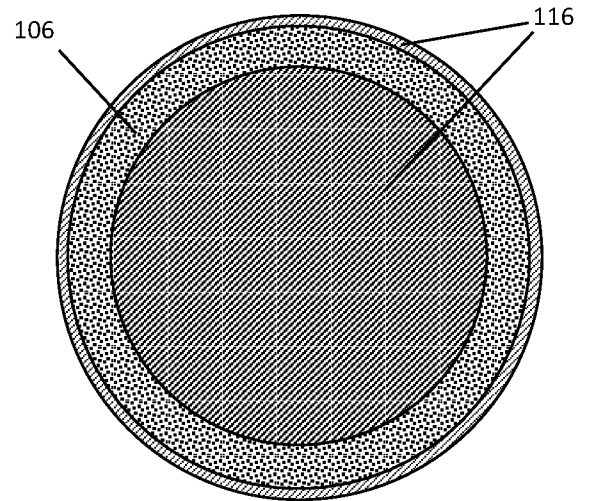
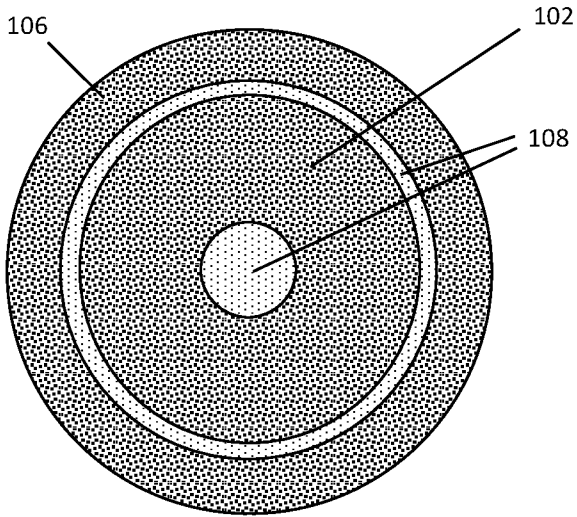
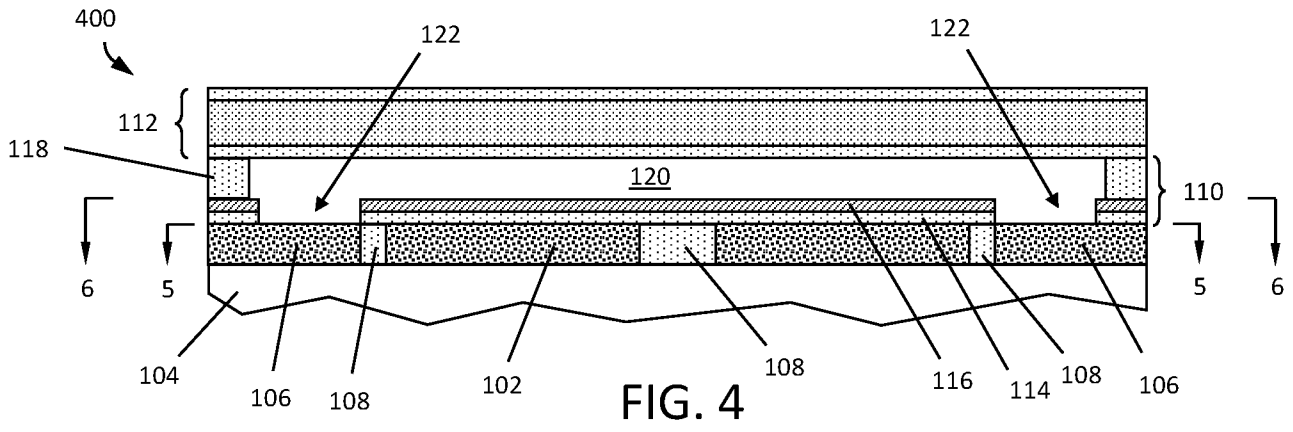
13. The device of claim 12, wherein the getter material is disposed at an outer perimeter of the cavity.

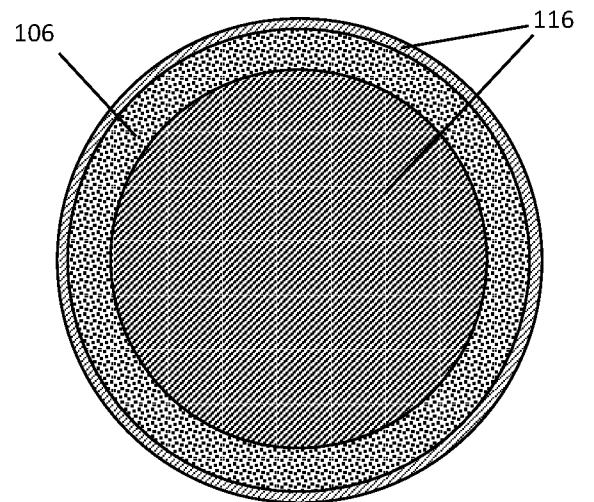
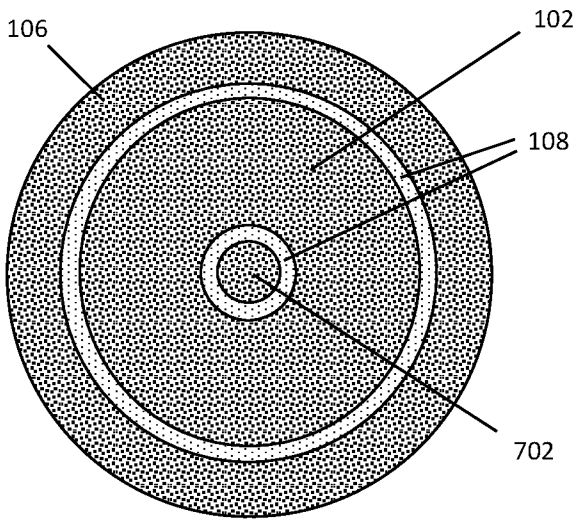
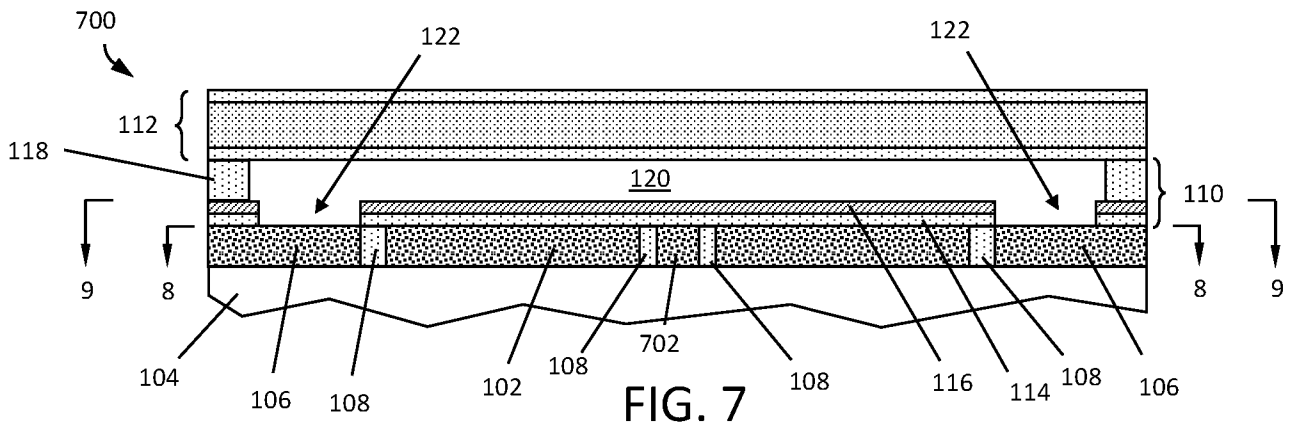
14. The device of claim 12, wherein the cavity is circular shaped and the getter material is disposed at an outer radius of the cavity.

15. The device of claim 9, wherein the getter material is selected to remove one or more gases including one or more of oxygen, nitrogen, argon, or water vapor.

16. The device of claim 9, wherein the getter material comprises a same material as the bottom electrode of the cavity.







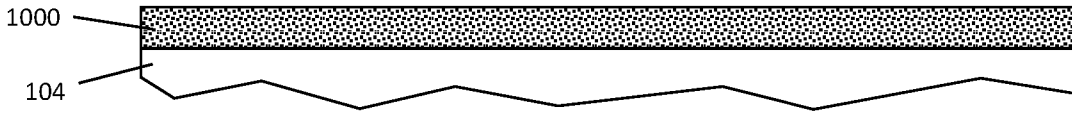


FIG. 10

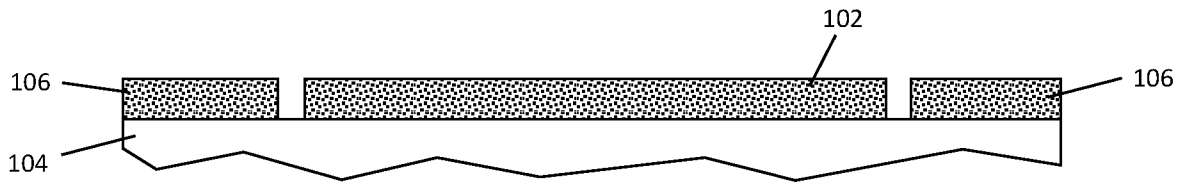


FIG. 11-1

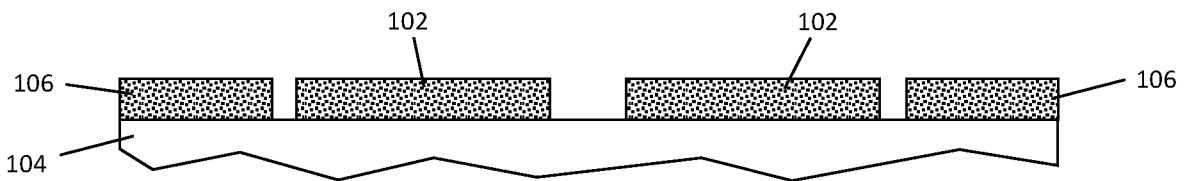


FIG. 11-2

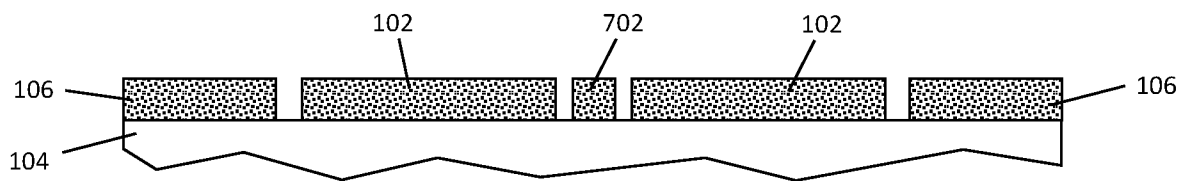


FIG. 11-3

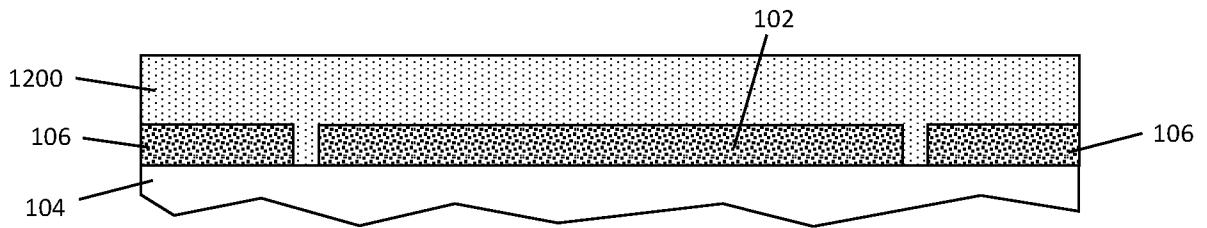


FIG. 12-1

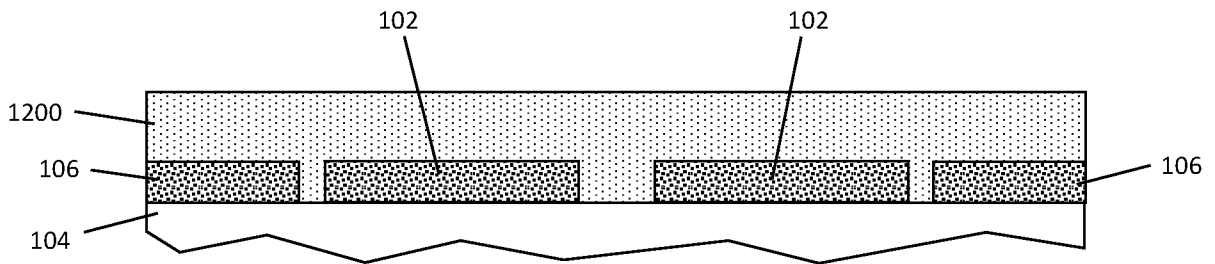


FIG. 12-2

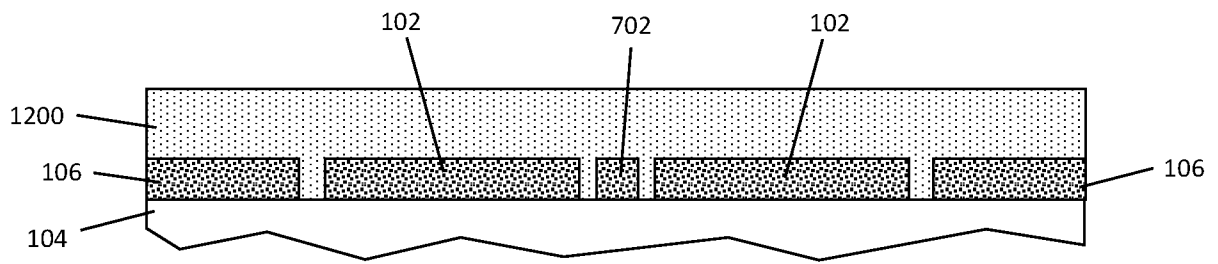


FIG. 12-3

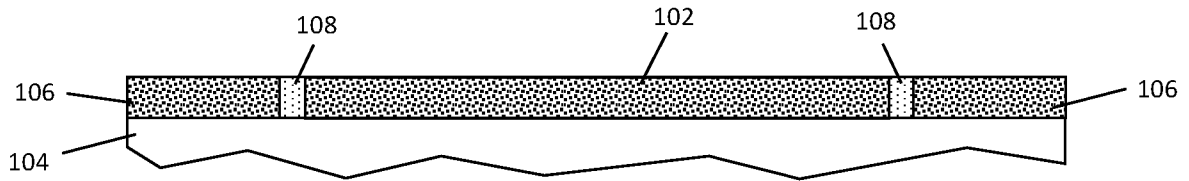


FIG. 13-1

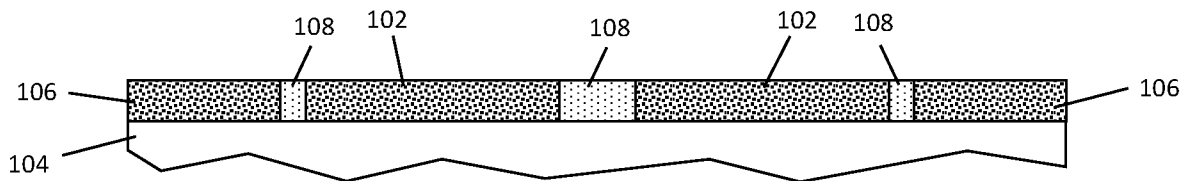


FIG. 13-2

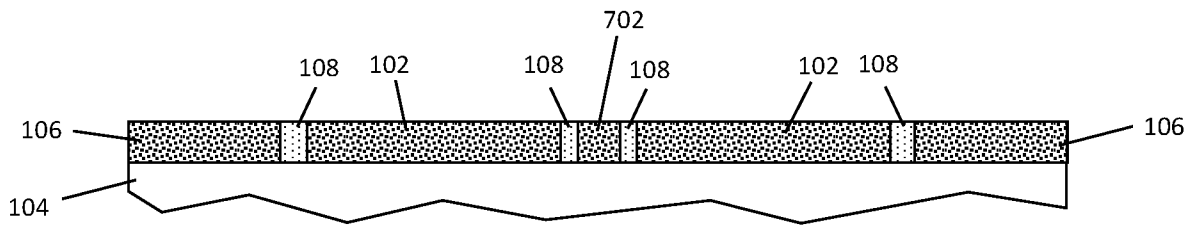
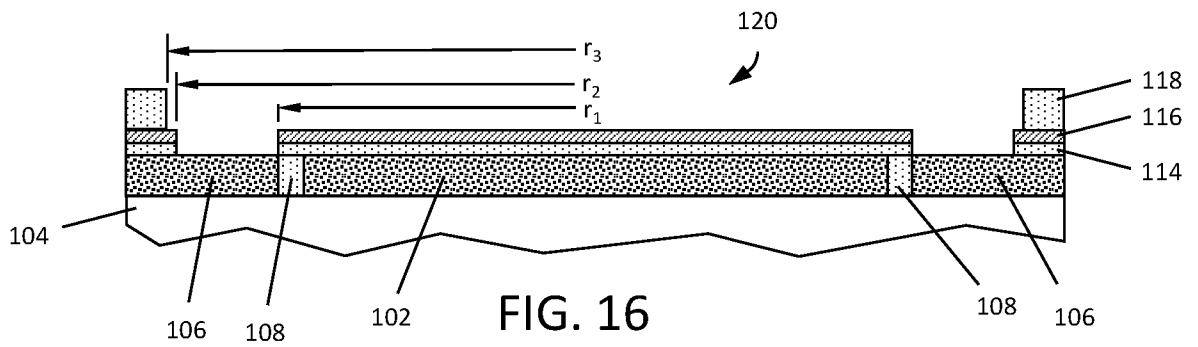
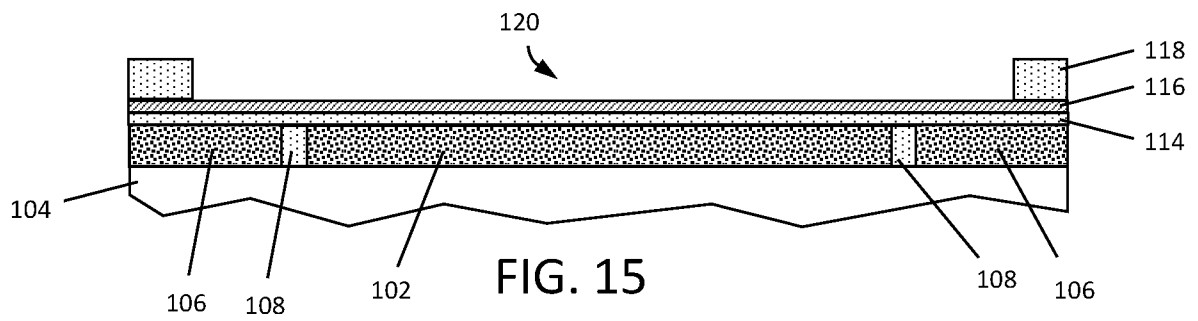
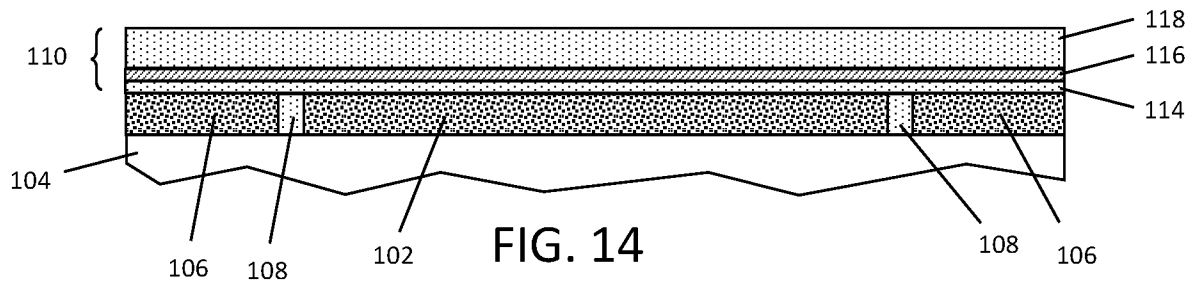
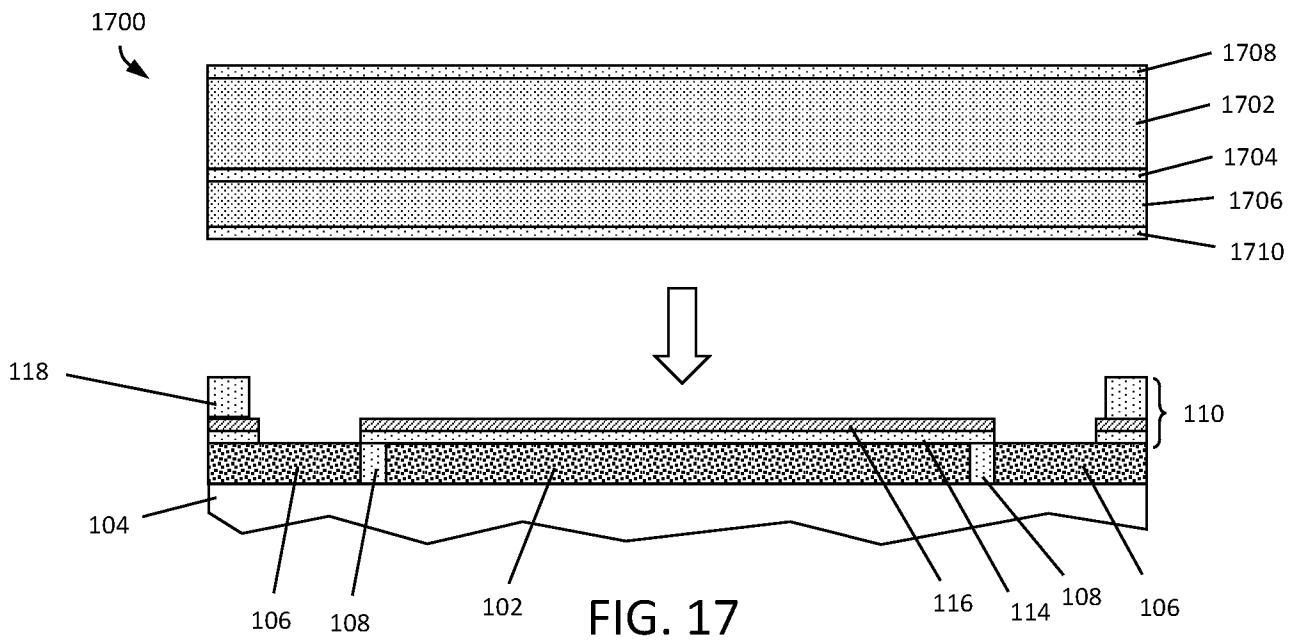


FIG. 13-3





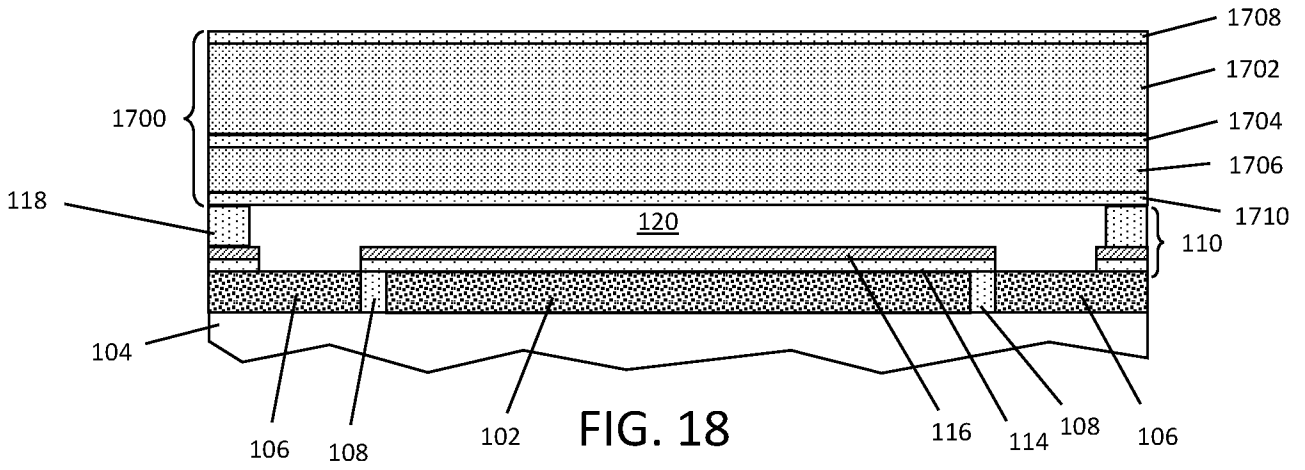


FIG. 18

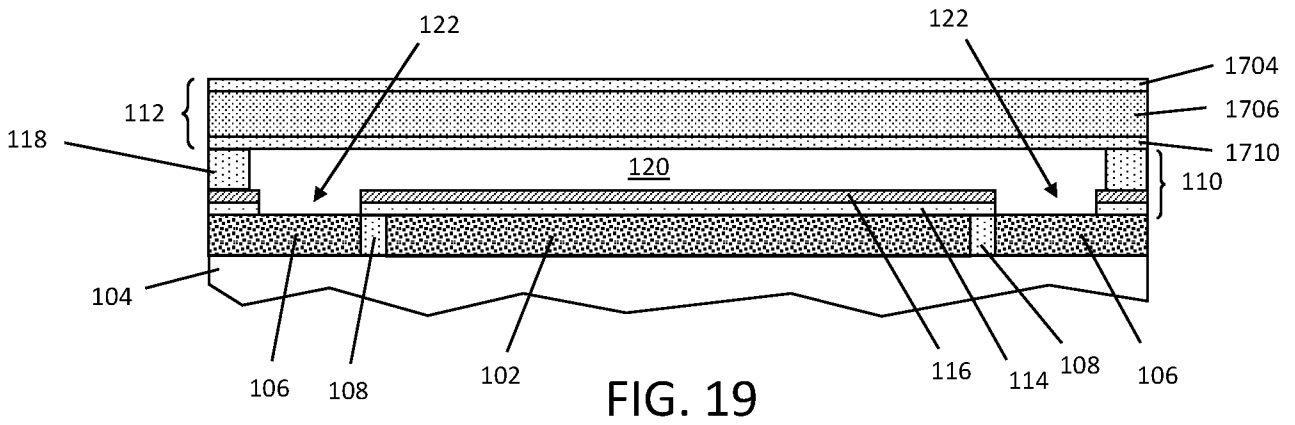


FIG. 19

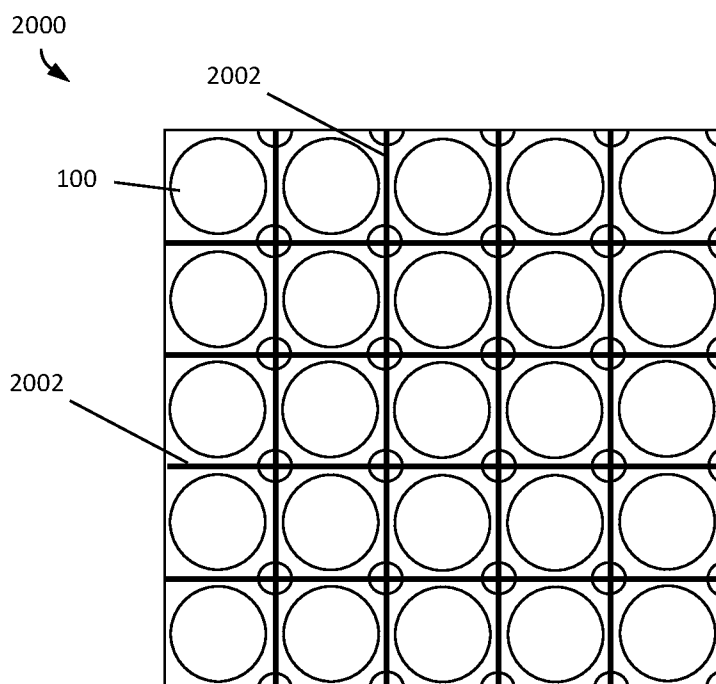


FIG. 20

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US19/53352

A. CLASSIFICATION OF SUBJECT MATTER

IPC - B81B 3/00; B81C 1/00 (2019.01)

CPC - B06B 1/00, 1/02, 1/0292; B81B 3/00, 3/0018, 3/0021; B81C 1/00, 1/00134, 1/00158, 1/00166, 1/00182, 1/00436, 1/00523; H03H 9/00, 9/02007, 9/15, 9/17, 9/171, 9/172, 9/173, 9/174; H01G 5/00, 5/16, 5/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- A	US 2011/0018398 A1 (FUKUDA, J) 27 January 2011; figures 1,3,4; paragraphs [0025], [0066]	1-4, 8-11, 15-16 ----- 5-7
X --- Y	US 2013/0135056 A1 (STMICROELECTRICS S.R.I) 30 May 2013; figures 10b,13; paragraphs [0027], [0047], [0058]	1-2, 4, 8-13, 15 ----- 14
Y	WO 2013/049794 A1 (CLEAN ENERGY LABS, LLC) 04 April 2013; figure 4	14
A	US 2011/0050045 A1 (ARATAKE, K et al.) 03 March 2011; entire document	1-16
A	US 2018/0243792 A1 (BUTTERFLY NETWORK, INC.) 30 August 2018; entire document	1-16
A	US 2017/0232474 A1 (NORTH CAROLINA STATE UNIVERSITY) 17 August 2017; entire document	1-16

 Further documents are listed in the continuation of Box C. See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 November 2019 (20.11.2019)

Date of mailing of the international search report

16 DEC 2019

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