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(54) APPARATUS FOR MASS DIE TESTING

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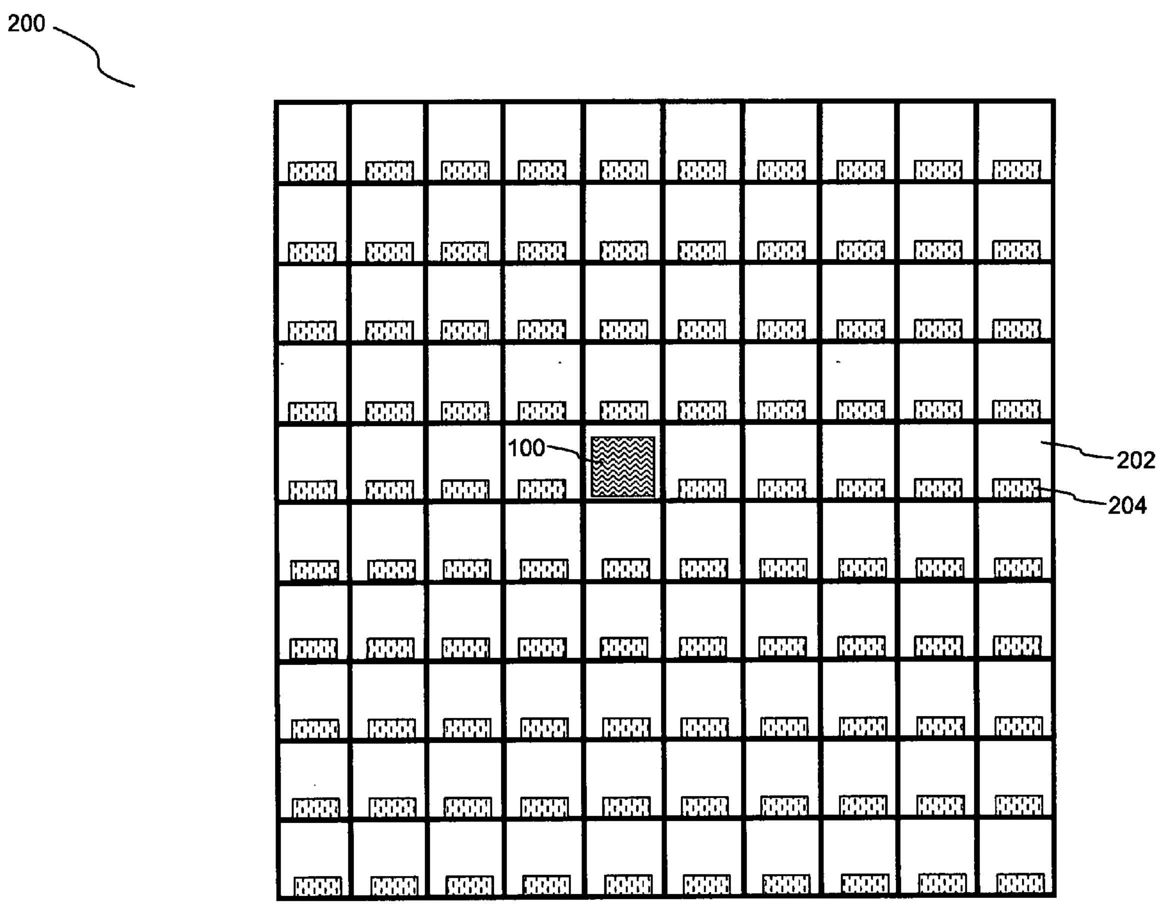
(57) ABSTRACT

A semiconductor wafer includes a set of dice under test connected together by a plurality of signal buses; and at least one test die designed for carrying out tests of the dice under test, having a set of pads to be connected to one or more probes of an external test apparatus, and at least one multiplexer connected with the set of dice under test via the signal buses, such that the test die is capable of receiving signals from the external test apparatus to select any die under test within the set via the multiplexer and the signal buses without repositioning the probes.



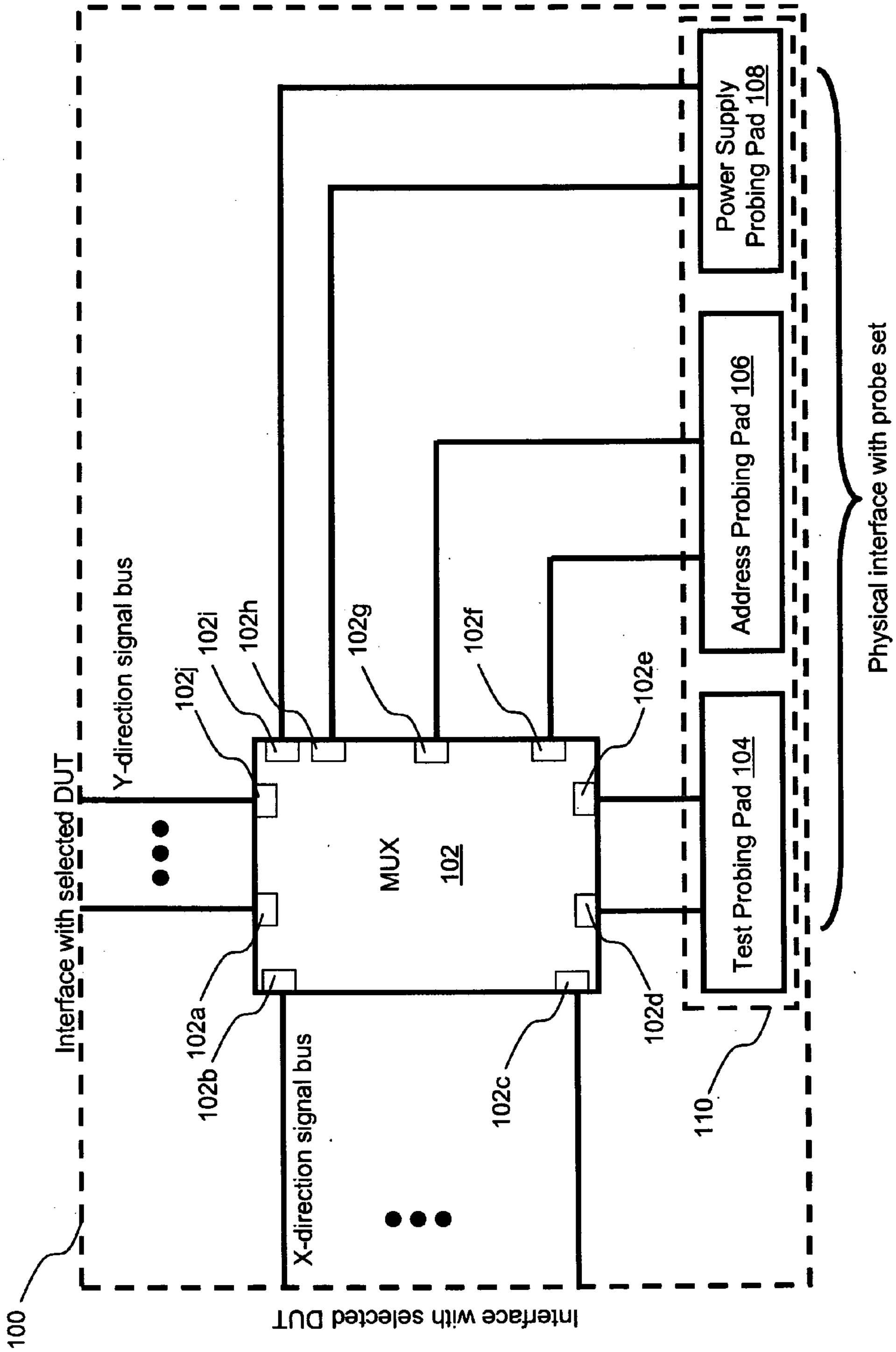

100
Interface with selected DUT
Y-direction signal bus
X-direction signal bus
Interface with selected DUT
MUX
102
102a
102b
102c
102d
102e
102f
102g
102h
102i
102j
Test Probing Pad 104
Address Probing Pad 106
Power Supply Probing Pad 108
110
Physical interface with probe set

FIG. 1

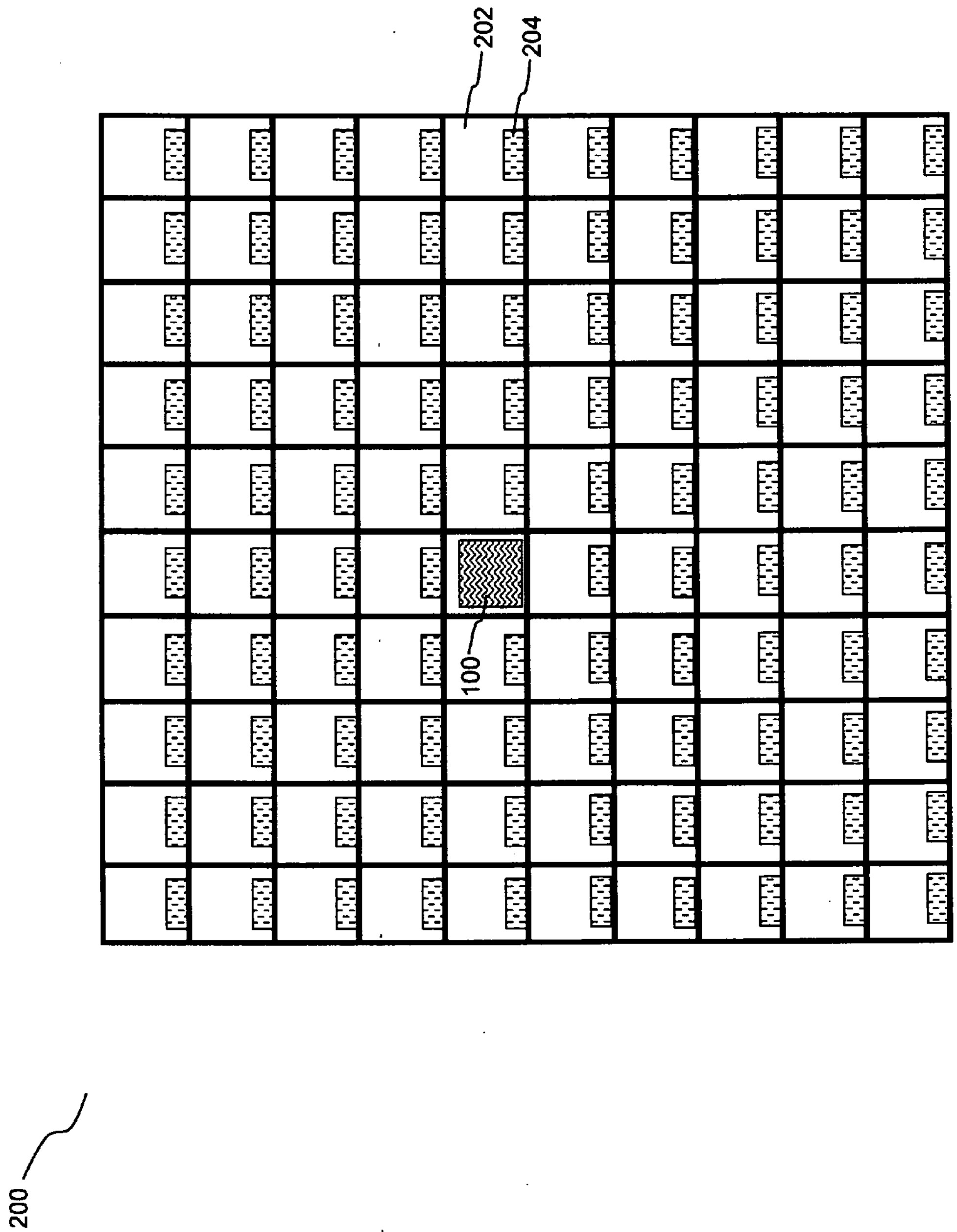


FIG. 2A

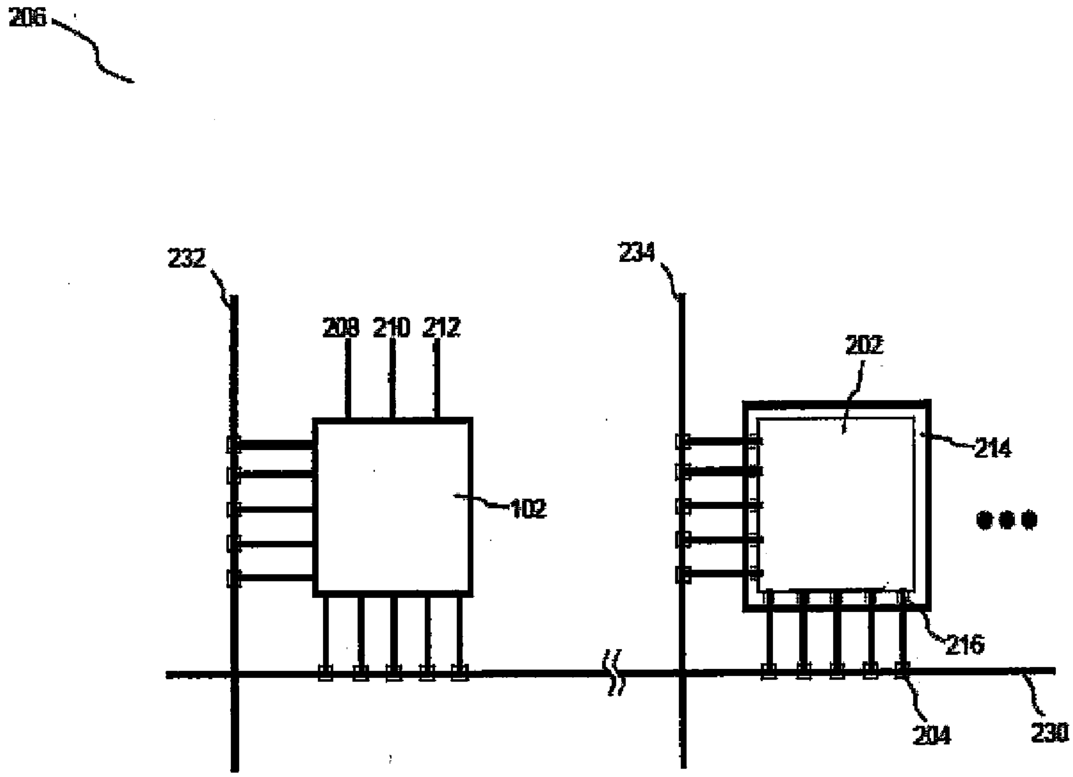


FIG. 2B

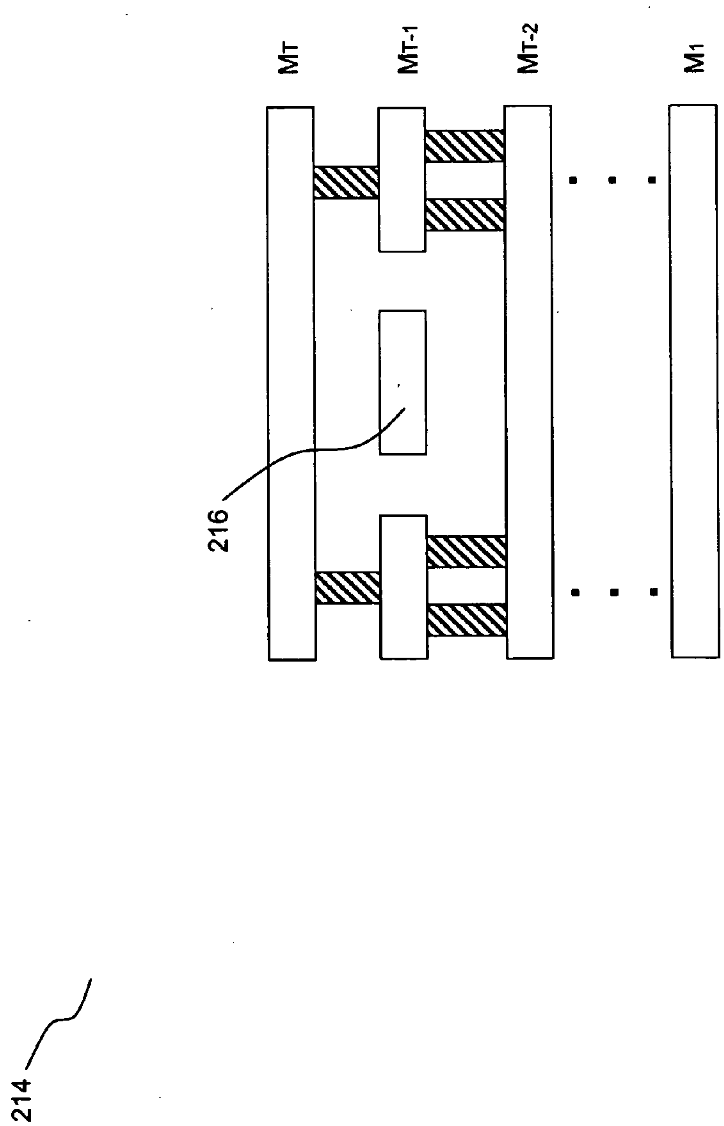


FIG. 2C

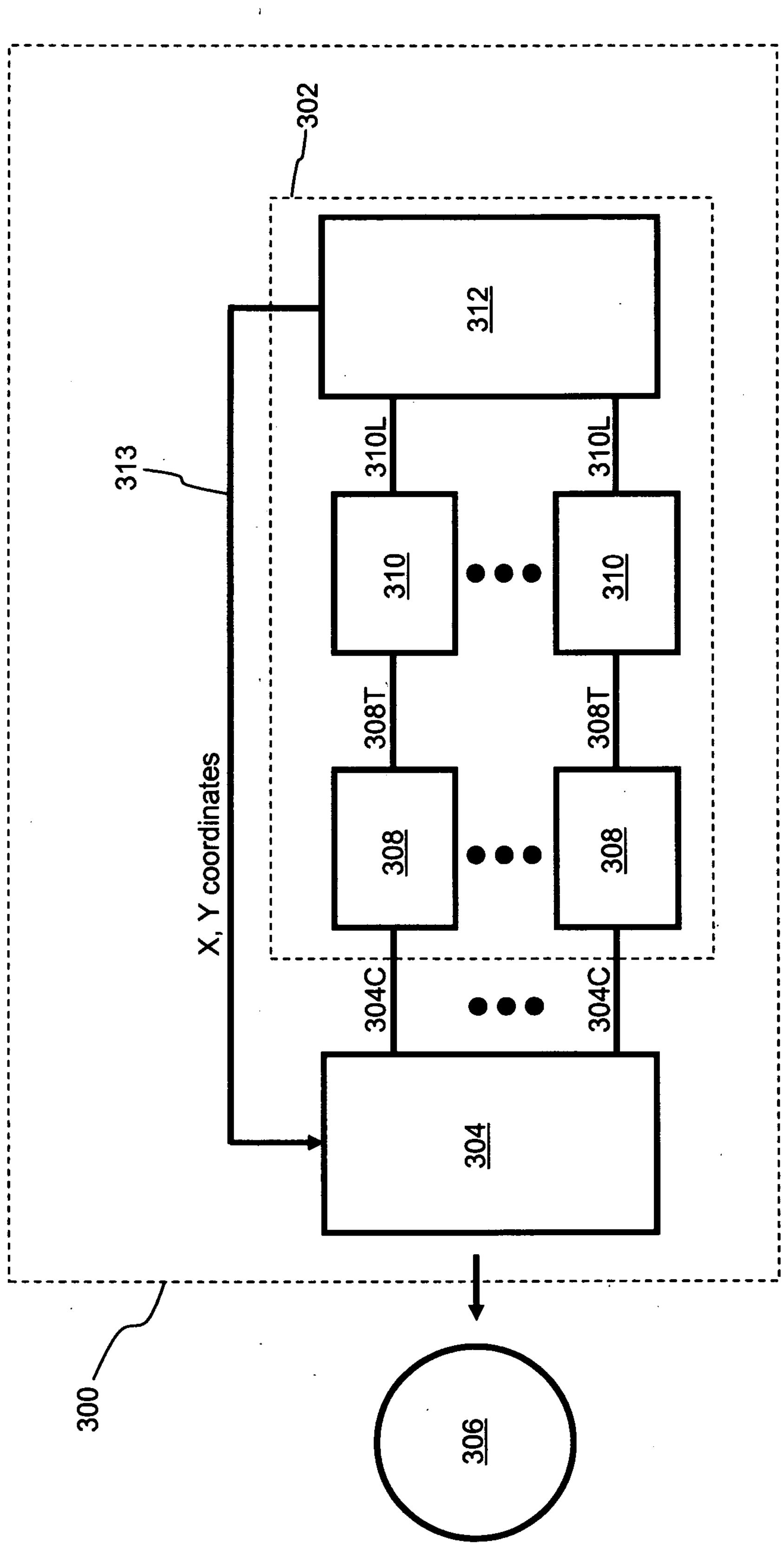

302
312
313
310L
310L
310
310
308T
308T
X, Y coordinates
308
308
304C
304C
304
300
306

FIG. 3A

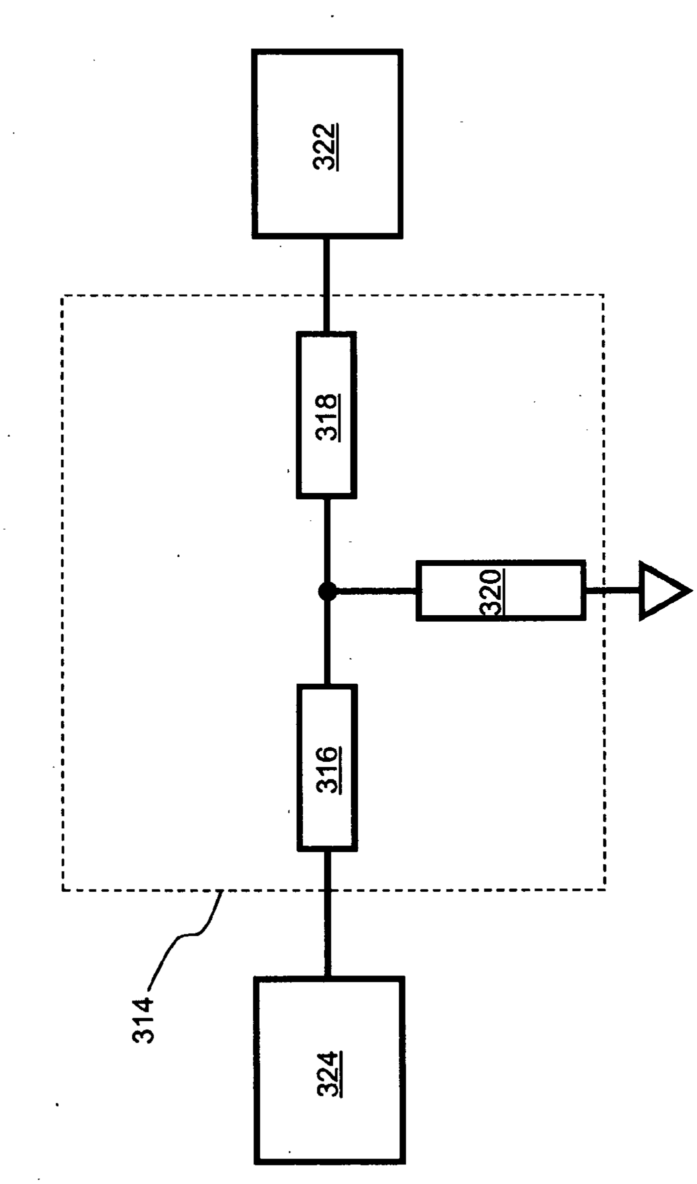


FIG. 3B

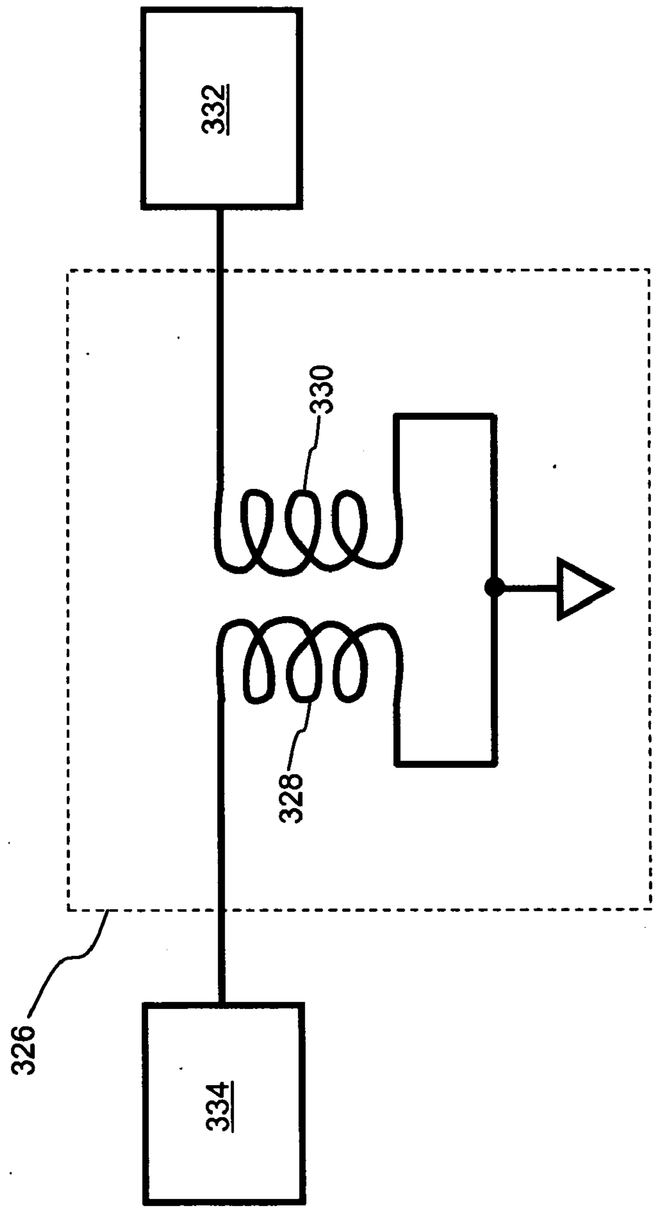


FIG. 3C

APPARATUS FOR MASS DIE TESTING

BACKGROUND

[0001] The present invention relates generally to integrated circuit (IC) designs, and more particularly to an apparatus for testing a large number of dice on a semiconductor wafer without repositioning test probes.

[0002] A semiconductor wafer typically contains a large number of dice constructed on a round-shaped semiconductor substrate. Each die embodies a complex integrated circuit formed by semiconductor processing technology, such as chemical vapor deposition, thermal oxidation, ion implantation, lithography, etching, and metallization, to carry out certain functionalities. These dice need to be tested to determine whether they meet predefined specifications, before they can be separated from the wafer for individual package. Conventionally, each die may include one or more pads that can be used to form electrical contacts with test probes of an external test machine. The test machine sends out test signals and receives resultant signals to and from the die under test (DUT) via the test probes and the pads. The resultant signal contains information with respect to the DUT, and can be further analyzed by the test machine to determine whether the DUT meet those predefined specifications.

[0003] One drawback of the conventional die testing scheme is that it is very time consuming. Every time when the test machine tests a new die, the test probes need to be repositioned from a previous DUT to form electrical contacts with the pads of the new die. Every repositioning of probes may take seconds, and a semiconductor wafer usually contains tens to tens of thousands of dice. As a result, a complete test for a semiconductor wafer usually requires a long time, which often represents a significant portion of the manufacturing cost for each die. As the semiconductor processing technology advances, the number of dice on a semiconductor wafer increases significantly, and therefore the manufacturing cost of die also increases dramatically due to the prolonged die testing procedure.

[0004] For example, conventional probe testing can only be performed on a few unsorted dice, typically less than 20 DUTs, for each time that the probes are positioned. In order to perform tests on a larger number of DUTs, the probes need to be repositioned. Supposing that 80,000 DUTs on a semiconductor wafer need to be tested, a really long period of time will be needed just for repositioning the probes. In the time-conscious of semiconductor industry, the cost incurred by the testing time is often unacceptable.

[0005] As such, desirable in the art of IC designs is an apparatus for testing a large number of dice on a semiconductor wafer without repositioning test probes.

SUMMARY

[0006] The present invention discloses an apparatus for testing a large number of dice on a semiconductor wafer without repositioning test probes. One embodiment of the invention is described herein for explaining the principles of the invention. In the embodiment, the apparatus is embodied as a semiconductor wafer, which includes a set of dice under test connected together by a plurality of signal buses; and at least one test die designed for carrying out tests of the dice under test, having a set of pads to be connected to one or more probes of an external test apparatus, and at least one multiplexer connected with the set of dice under test via the signal buses, such that the test die is capable of receiving signals from the external test apparatus to select any die under test within the set via the multiplexer and the signal buses without repositioning the probes.

[0007] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** illustrates a block diagram of a built-in self test (BIST) die used for multiplexing test signals to a selected DUT on a semiconductor wafer in accordance with one embodiment of the present invention.

[0009] FIG. **2**A illustrates a set of DUTs, among which a BIST die is implemented, in accordance with one embodiment of the present invention.

[0010] FIG. **2**B illustrates a diagram showing a DUT connected to the BIST die via signal buses routed along the scribe lines in accordance with one embodiment of the present invention.

[0011] FIG. **2**C illustrates a cross-sectional view of the seal ring in accordance with one embodiment of the present invention.

[0012] FIG. **3**A illustrates a block diagram of a test system designed for testing a plurality of RF dice in accordance with one embodiment of the present invention.

[0013] FIG. **3**B illustrates an impedance matching circuit that can be implemented in a matching module of the test system shown in FIG. **3**A in accordance with one embodiment of the present invention.

[0014] FIG. **3**C illustrates a transformer circuit that can be implemented in a matching module of the test system shown in FIG. **3**A in accordance with one embodiment of the present invention.

DESCRIPTION

[0015] This invention describes an apparatus for testing a large number of dice on a semiconductor wafer without repositioning test probes. The following merely illustrates various embodiments of the present invention for purposes of explaining the principles thereof. It is understood that those skilled in the art will be able to devise various equivalents that, although not explicitly described herein, embody the principles of this invention.

[0016] FIG. **1** illustrates a block diagram of a BIST die **100** implemented for performing circuit probing test for RF dice on a semiconductor wafer in accordance with one embodiment of the present invention. It is noted that the RF dice are used merely as an example to explain the principles of the invention, which can be applied to other types of dice, and by no means are limited to RF dice.

[0017] The BIST die **100** includes a multiplexer **102**, a set of test probing pads **104**, a set of address probing pads **106**, and a set of power supply probing pads **108**. The probing pads **104**, **106** and **108** can be collectively referred to as a pad array **110**. The multiplexer **102** has a plurality of ports **102***a* through **102***j* connected to a plurality of signal buses, including the buses extended to the pad array **110** and the buses extended to other dice on the semiconductor wafer. During test operation, the probing pads **104**, **106**, and **108** are further coupled to a test apparatus (not shown in this figure), which selects one or more dice on a semiconductor wafer for testing. The multiplexer **102** is also coupled with signal buses **102***b* and **102***a* that are placed on a X-direction scribe line and a Y-direction scribe line, respectively, such that a specific DUT may be selected by the multiplexer **102** with address information received at the address probing pads **106** from the test apparatus. When a particular DUT is selected by the BIST die **100**, it can be powered up quickly using the power received at the power supply probing pads **108** from the test apparatus or using the DC power converted from an RF signal generated by the test apparatus with the DUT or the BIST die. Various tests can be performed on the selected DUT based on the test signals received at the test probing pads **104** from the test apparatus. In this embodiment, the BIST die **100** is embedded among the dice under test on the semiconductor wafer.

[0018] In another embodiment, the multiplexer **102** can be implemented on a probe card, instead of a semiconductor wafer. The multiplexer **102** on the probe card includes a number of ports that allow the multiplexer to couple with a test apparatus for receiving and transmitting test signals, address signals, and power signals there between. The probe card further includes a number of probes for forming electrical contacts with the DUTs on the semiconductor wafer. In this embodiment where the probe card is used to test RF DUTs, the probes at minimum includes two RF probes for passing RF test signals, two power probes for supplying power, and three digital probes for passing address signals. The semiconductor wafer can be implemented with a number of pads that function as accesses to the DUTs through signal buses routed along the scribe lines. The probes can be placed on the pads of the semiconductor wafer to form one or more signal paths among the DUTs and the test apparatus. The test apparatus can select one or more DUTs, sends out RF test signals, and receives resultant signals from the DUTs for further analysis to determine whether they meet certain predefined specifications.

[0019] FIG. **2**A illustrates a set of DUTs **200**, among which a BIST die **100** as shown in FIG. **1** is implemented in accordance with one embodiment of the present invention. The set of DUTs **200**, for example, includes 99 DUTs **202** arranged in a 10×10 array. The multiplexer within the BIST die **100** is connected to each DUT within the set **200** through signal buses routed along the scribe lines, which are shown as the dark lines in this figure. Each DUT **202** includes a set of tacks **204** that are extended from the circuit region of the DUT **202** to its surrounding scribe lines to form electrical connections between the electrical components within the DUT **202** and the signal buses on the scribe lines.

[0020] When a DUT is being tested, a test apparatus (not shown in the figure) generates testing signals, address signals, and power signals to the multiplexer within the BIST die **100** through contacts formed by its probes and the probing pads on the BIST die **100**. The multiplexer utilizes the information carrier by the address signals to select one or more DUTs for testing. Power and test signals are passed onto the selected DUTs via the signal buses. The set of tacks extended from the selected DUT to the scribe line allow the DUT to receive test signals and power from the signal buses. It is noted that although FIG. **2**A only shows 99 DUTs, in real applications, the BIST die **100** may be implemented among a set of DUTs with a much larger number, such that the probes will not need to be repositioned for any DUT selected from the set.

[0021] FIG. **2**B illustrates an enlarged diagram **206** showing the DUT **202** and the multiplexer **102** of the BIST die are connected via signal buses along the scribe lines in accordance with one embodiment of the present invention. The multiplexer **102** is coupled with the signal buses along an X scribe line **230** and a Y scribe line **232**, and it is designed to select a DUT within the array based on the address information provided by address signals received at the address probing pad from an external test apparatus. The multiplexer **102** has a number of ports designed for receiving signals from the probes of the test apparatus that are in contact with its probing pads. In this embodiment, the multiplexer **102** includes a set of RF testing signal ports **208**, a set of address ports **210**, and a set of power input ports **212**. When the DUT **202** is selected using the address information received at the address ports **210**, the multiplexer **102** will provide power and RF test signals received at its power and RF ports to the DUT **202** through the signal buses along the scribe lines. It is noted that in one embodiment, the DUT **202** can convert RF power received from the multiplexer **102** into DC power for operation. In such case, the multiplexer **102** will provide only the RF signals without the power signals.

[0022] The integrated circuits in the DUT **202** is surrounded by a seal ring **214** that is designed to protect the electrical components within the DUT **202** from the outside environment, once it is cut out from the semiconductor wafer. The DUT **202** is coupled with the signal buses along the X scribe line **230** and a Y scribe line **234** via the tacks disposed there between. The tacks, not shown in FIG. **2**B, are metal traces deposited at the edges of the DUT **202**, and extended to the signal buses on the scribe line. These metal traces are designed to deliver signals, such as the RF test signals, from the multiplexer **102** into the DUT **202**, and they are laid on the space of the scribe lines that will eventually be cut off when the dice are separated. In order for the connection to be made between the DUT **202** and the signal buses, a plurality of feed-through paths **216** are constructed through the seal ring **214** for the metal traces to contact with the electrical components within the DUT **202**. The DUT **202** has a number of ports used for receiving signals from the tacks passing though the seal ring **214**.

[0023] FIG. **2**C illustrates a cross-sectional view of the seal ring **214**, across which the feed-through paths **216** are disposed, in accordance with one embodiment of the present invention. The feed-through paths **216** can be formed on any metallization layer. In another embodiment, multiple feed-through paths **216** may be used for complex applications, where the feed-through paths **216** are electrically connected with one another through vias, if required.

[0024] FIG. **3**A illustrates a block diagram of a test system **300** designed for testing a large quantity of RF dice on a semiconductor wafer **306** in accordance with one embodiment of the present invention. The test system **300** includes a test apparatus **302** and a probe array **304**. The test apparatus **302** further includes a plurality of matching modules **308**, a plurality of RF testers **310**, and a control device **312**.

[0025] In this embodiment, the semiconductor wafer **306** contains a large number of RF dice grouped into hundreds of sets of DUTs. Each set of DUTs includes at least one test chip such as the BIST die **100** shown in FIG. **1**. Several thousands of DUTs with the set can be selected and tested for each placement of probes based on the address information provided to the BIST die **100** by the control device **312** via an addressing bus **313** and the probe array **304**. This addressing bus **313** essentially provides X and Y coordinates that are designated by the control device **312** and received by the probe array **304**. The probe array **304** provides physical connections to the BIST die **100** which, based on the X and Y coordinates provided by the addressing bus **313**, selects one or more DUTs for testing. During test operation, RF test input signals are provided to the selected DUTs, and the output test signals from the selected DUTs then travel through the multiplexer within the BIST die and the probe array **304** to reach the matching modules **308** via a set of RF cables **304**C. The matching modules **308** are designed to couple the RF signals between the probe array **304** and the RF testers **310**. Thus, the signals output from the selected DUTs can be sent to the RF tester **310** and control device **312** for further analysis to determine whether they meet certain predetermined specifications.

[0026] FIG. **3**B illustrates an impedance matching circuit **314** that can be implemented in the matching module **308** shown in FIG. **3**A in accordance with one embodiment of the present invention. The impedance matching circuit **314**, which includes inductors **316**, **318** and a capacitor **320**, is implemented between an antenna interface **324** coupled to the probe array **304** shown in FIG. **3**A and an RF tester **322**. The inductors **316** and **318** are serially connected with the capacitor connected there between in parallel in order to couple RF signals between the antenna interface **324** and the RF tester **322**. The matching circuit **314** allows RF signals to be converted into DC signals, thereby allowing the test apparatus **302** to test RF dice on the semiconductor wafer **306**, as shown in FIG. **3**A.

[0027] FIG. **3**C illustrates a transformer circuit **326** that can also be implemented in the matching module **308** shown in FIG. **3**A in accordance with one embodiment of the present invention. The transformer circuit **326** includes two inductors **328** and **330**, and is implemented between an antenna interface **334** coupled to the probe array **304** shown in FIG. **3**A and a RF tester **332**. The transformer circuit **326** allows RF signals to be converted into DC signals, thereby allowing the test apparatus **302** to test RF dice on the semiconductor wafer **306**, as shown in FIG. **3**A.

[0028] One of the advantages of the invention is that the time needed for testing a semiconductor wafer can be reduced significantly due to a reduced number of probe repositioning. For example where a semiconductor wafer has 79,920 dice, the dices can be grouped into 555 sets with each having 114 dice. In this example, the probes only need to be repositioned 555 times to complete the test of the wafer. However, in a conventional test scheme, the probes may need to be repositioned 79,920 times to complete the test. As a result, the proposed test scheme can reduce the test time significantly, thereby reducing the manufacturing costs of the wafer. Another advantage of the invention is that the proposed scheme with the antenna coupling device can be used to test RF dice, which may not be readily tested by conventional test schemes.

[0029] The BIST dice and regular dice can be constructed on a semiconductor wafer by various processes. In one embodiment of the present invention, a mask set is used to form both the BIST dice and regular dice on the semiconductor wafer. During photolithography processes, a layer of photoresist material is coated over the wafer, and then exposed to light for transferring circuit patterns from the mask set to the photoresist layer. The transferred patterns include those for the regular dice and those for the BIST dice. Thus, one mask set would be sufficient. In another embodiment of the present invention, two mask sets are used to form the BIST dice and regular dices on a semiconductor wafer. One of the mask sets includes patterns for making the regular dice and the other mask set includes patterns for making the BIST dice. As such, two separate photolithography processes will be needed to transfer the patterns from the two mask sets to the photoresist layer coated on the semiconductor wafer for forming the two types of dice.

[0030] The above illustration provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

[0031] Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

1. A semiconductor wafer comprising:

a set of dice under test (DUT) connected together by a plurality of signal buses; and

at least one built-in self test (BIST) die including at least one multiplexer designed for multiplexing test signals to a selected DUT on the semiconductor wafer for carrying out tests of the dice under test, the BIST die having a set of pads to be connected to one or more probes of an external test apparatus, and

wherein the at least one multiplexer being connected with the set of dice under test via the signal buses, such that the BIST die is capable of receiving signals from the external test apparatus to select any die under test within the set via the multiplexer and the signal buses without repositioning the probes.

2. The semiconductor wafer of claim **1** wherein the set of pads comprises one or more test probing pads for receiving test signals from the external test apparatus via the probes.

3. The semiconductor wafer of claim **1** wherein the set of pads comprises one or more address probing pads for receiving address signals indicating an address of at least one die under test from the external test apparatus via the probes.

4. The semiconductor wafer of claim **1** wherein the set of pads comprises one or more power supply probing pads for receiving power from the external test apparatus via the probes.

5. The semiconductor wafer of claim **1** wherein the signal buses are routed along scribe lines among the dice under test.

6. The semiconductor wafer of claim **5** wherein each die under test has a seal ring with one or more feed-through paths, through which one or more tacks are disposed to form electrical connections between the signal buses and electrical components within the seal ring.

7. The semiconductor wafer of claim **6** wherein the die under test is a radio frequency (RF) chip.

8. A test system comprising:

a semiconductor wafer having a set of dice under test connected together by a plurality of signal buses, and at least one built-in self test BIST die designed for carrying out tests of the dice under test, wherein the BIST includes at least one multiplexer;

a set of probes connected to one or more pads on the BIST die;

a test apparatus coupled to the probes for sending test signals to one or more selected dice under test, and for receiving output signals from the selected dice under test for analysis through the multiplexer,

wherein the multiplexer is connected to the dice under test via the signal buses, such that the BIST die is capable of receiving signals from the test apparatus to select any die under test within the set without repositioning the probes.

9. The system of claim **8** wherein the pads comprise one or more test probing pads for receiving test signals from the test apparatus via the probes, one or more address probing pads for receiving address signals indicating an address of at least one die under test from the test apparatus via the probes, and one or more power supply probing pads for receiving power from the test apparatus via the probes.

10. The system of claim **8** wherein the signal buses are routed along scribe lines among the dice under test.

11. The system of claim **10** wherein each die under test has a seal ring with one or more feed-through paths, through which one or more tacks are disposed to form electrical connections between the signal buses and electrical components within the seal ring.

12. The system of claim **8** wherein the regular die is a radio frequency (RF) chip.

13. The system of claim **12** wherein the set of probes comprises at least two test signal probes for passing test signals, at least three address probes for passing address signals to select one or more dice under test, and at least two power probes for providing the test die with power.

14. The system of claim **13** wherein the test apparatus comprises a control device coupled to the probes for generating the address signals.

15. The system of claim **14** wherein the test apparatus comprises at least one RF tester coupled between the control device and at least one matching module that couples RF signals between the RF tester and an antenna interface for signals output from the test die.

16. The system of claim **15** wherein the matching module is a transformer or an impedance matching circuit constructed by at least one inductor and at least one capacitor.

17. A probe card for testing a set of dice under test on a semiconductor wafer, comprising:

at least one set of probes to be connected to one or more pads or a built-in self test (BIST) die on the semiconductor wafer for providing accesses to the dice under test via signal buses there among;

at least one multiplexer located within the BIST die and coupled to the probes, having one or more ports for receiving and sending signals from and to an external test apparatus;

wherein when the test probes are in contact with the pads and the ports are connected to the external test apparatus, the external test apparatus can select any die under test within the set without repositioning the probes.

18. The probe card of claim **17** wherein the probes comprises at least one radio frequency (RF) probes for passing RF test signals, at least two power probes for providing power, and at least three digital probes for passing address signals.

19. The probe card of claim **17** wherein the signal buses are routed along scribe lines among the dice under test.

20. The probe card of claim **17** wherein each die under test has a seal ring with one or more feed-through paths, through which one or more tacks are disposed to form electrical connections between the signal buses and electrical components within the seal ring.

* * * * *