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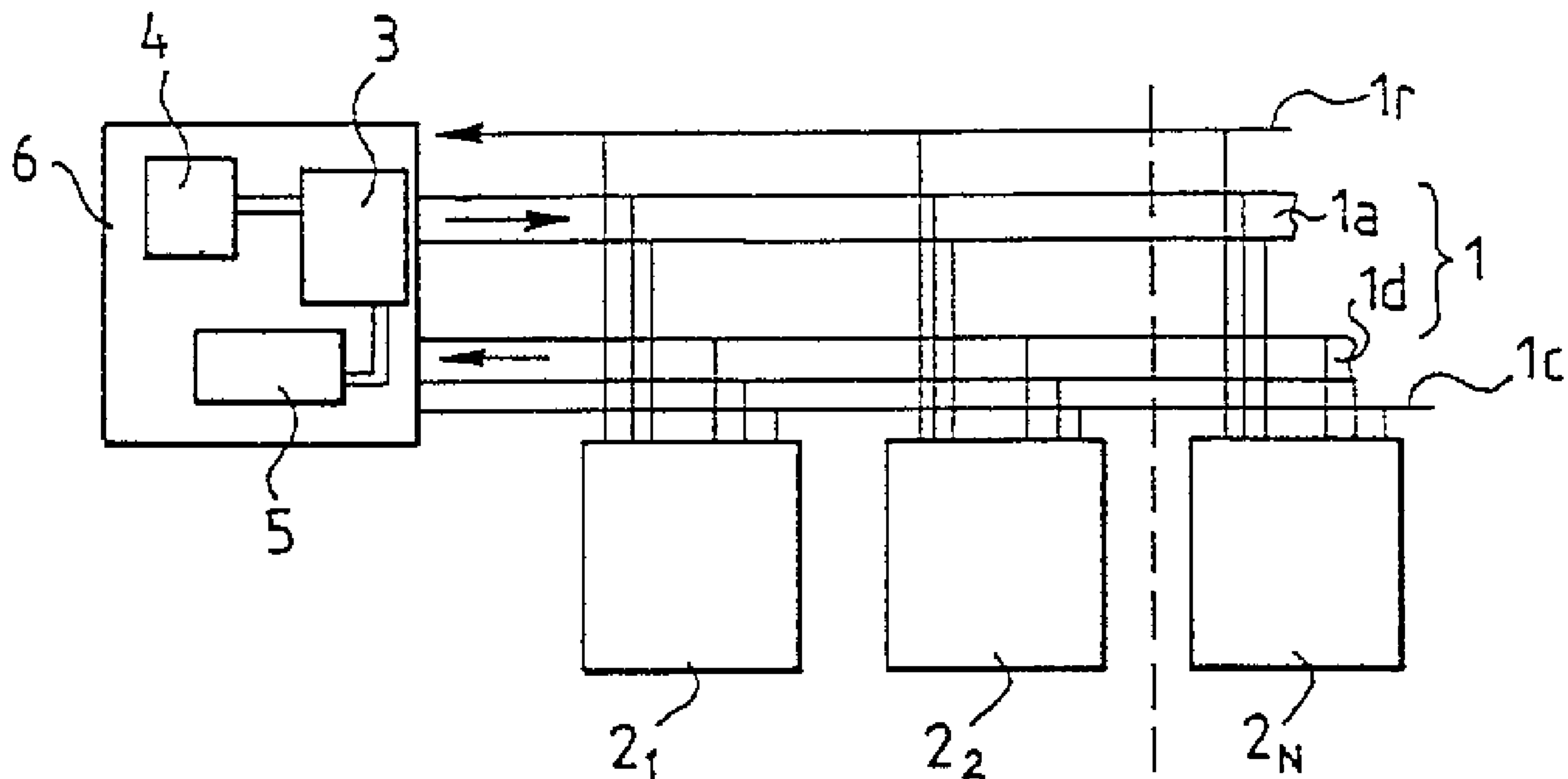
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(54) Title: METHOD AND SYSTEM FOR CONTROLLING STATISTICALLY MULTIPLEXED ATM BUS



(57) **Abrégé/Abstract:**

The invention relates to a method and system for controlling a statistically multiplexed ATM bus (1), to the bus being connected a bus controller (6) and interface units (2_{1-2_N}) for transmission of packets, i.e. cells, over the bus. Having detected, for each cell to be transmitted to an ATM bus, the address of the interface unit participating in the transmission, the bus controller (6) sets the address on an address bus (1a) of the ATM bus (1), thereby activating transmission of the cell from the bus controller to the interface unit or vice versa over a data bus (1d) of the ATM bus. During the transmission of the cell, the bus controller (6) fetches the next interface unit address for transmission of the next cell from or to the interface unit concerned.



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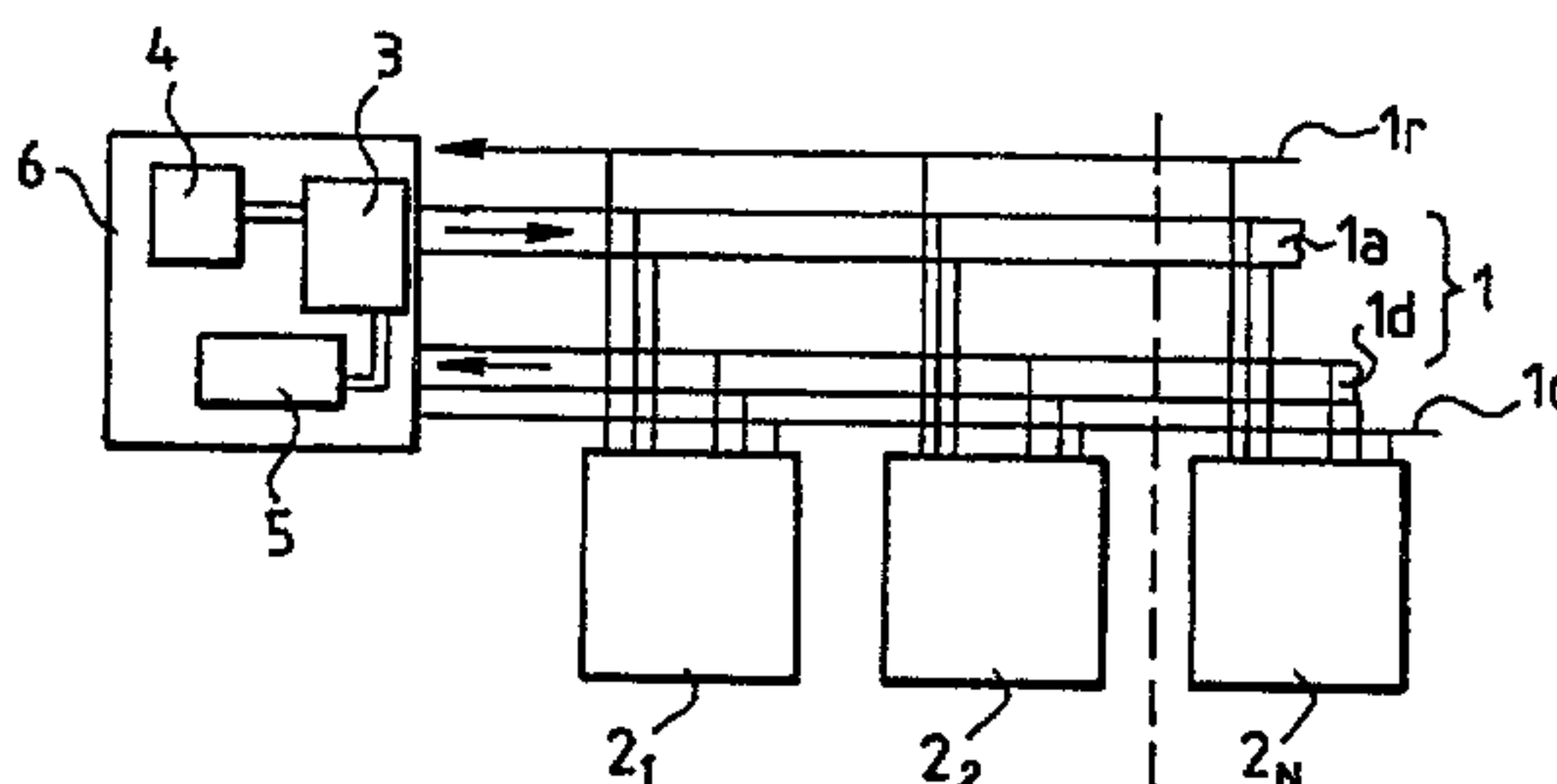
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(54) Title: METHOD AND SYSTEM FOR CONTROLLING STATISTICALLY MULTIPLEXED ATM BUS



(57) Abstract

The invention relates to a method and system for controlling a statistically multiplexed ATM bus (1), to the bus being connected a bus controller (6) and interface units (2₁-2_N) for transmission of packets, i.e. cells, over the bus. Having detected, for each cell to be transmitted to an ATM bus, the address of the interface unit participating in the transmission, the bus controller (6) sets the address on an address bus (1a) of the ATM bus (1), thereby activating transmission of the cell from the bus controller to the interface unit or vice versa over a data bus (1d) of the ATM bus. During the transmission of the cell, the bus controller (6) fetches the next interface unit address for transmission of the next cell from or to the interface unit concerned.

Method and system for controlling statistically multiplexed ATM bus

5 The invention relates to a method and system
for controlling a statistically multiplexed ATM bus, to
the bus being connected a bus controller and interface
units for transmission of packets, i.e. cells, over the
bus. The invention thus relates to a bus solution
10 applicable to statistical multiplexing and demulti-
plexing of ATM cells from several interface cards. The
interface rates are typically between 0 and 155 Mbit/s.

 In an ATM (Asynchronous Transfer Mode), data
is transmitted in packets, i.e. cells, of 53 octets. One
basic ATM rate at which these cells are transmitted and
15 switched is 155 Mbit/s. When interfaces with a lower
transmission rate are connected to an ATM switch that
switches 155 Mbit/s cell streams, the ATM cells
generated by the interfaces must be multiplexed to this
rate. Correspondingly, it must be possible to demulti-
20 plex a 155 Mbit/s cell stream to a lower rate.

 Previously used bus solutions, such as the SDH
multiplexers of product family SYNFO NET and the PCM
buses of Nokia DX200, are based on time-shared operation
of the bus, in which each interface is allocated a
25 separate time slot. This is a waste of bus capacity and
is not suitable to statistical multiplexing since bus
capacity is assigned irrespective of transmission need.
Because of this, concentration, i.e. serving of inter-
faces having a greater than nominal cell transmission
30 rate, is impossible.

 The object of the present invention is to pro-
vide a method and system by which the above restrictions
can be eliminated. The method of the invention is char-
acterized in that after detecting, for each cell to be
35 transmitted to an ATM bus, the address of the interface

unit participating in the transmission, the bus controller sets the address on an address bus of the ATM bus, thereby activating the transmission of the cell from the bus controller to the interface unit or vice versa over a data bus of the ATM bus; and that during the transmission of the cell, the bus controller fetches the next interface unit address for transmission of the next cell from or to the interface unit concerned.

The bus allocation in accordance with the invention enables the use of transmission capacity by only those interfaces that have an actual transmission need. The allocation method allows prioritization of interfaces and makes concentration possible by furnishing it with interface units having a transmission capacity of above e.g. 155 Mbit/s.

Transmission capacity of a bus controlled as described in the invention is thus used in both uplink and downlink directions such that in both directions e.g. a single unit can take the whole transmission capacity if the other units do not have anything to transmit.

The advantageous embodiments of the method according to the invention and the system according to the invention are characterized by what is stated in the claims below.

In the following the invention will be described by means of an example with reference to the attached drawing, wherein

Fig. 1 illustrates the principle of the invention in the multiplexing direction, and

Fig. 2 illustrates the principle of the invention in the demultiplexing direction.

The principle of the system shown in Fig. 1 and operating in accordance with the invention is the following.

The ATM bus of the invention is a 'point-to-multipoint' type bus with a transmission capacity of e.g. about 155 Mbit/s. Data is transmitted in cells of 53 octets. The start of a cell is indicated by a cell sync pulse, which occurs at 2.72 μ s intervals. The bus divides into a multiplexing ('uplink') and demultiplexing ('downlink') element, the multiplexing element being shown in Fig. 1 and the demultiplexing in Fig. 2. A multiplexing element 1 of the bus has its own data bus 1d and address bus 1a.

Part 1c of the bus is for timing on the cell and bit level. The operation of the bus is controlled by a bus controller 6, multiplexer, provided with a microprocessor 5 and connected to an ATM switch by a 155 Mbit/s line. To the bus is also connected a number of interface units 2_1-2_N , which generate and/or receive ATM cells in accordance with their own transmission need and rate.

In the multiplexing direction, the bus controller 6 allocates transmission periods to the interface units 2_1-2_N by setting interface unit addresses from a RAM 3 of the controller on the address bus 1a. The controller scans the entire address space within the duration of one cell, which in this example (155 Mbit/s bus) is the above-mentioned 2.72 μ s.

An interface unit 2_x , i.e. any one of units 2_1-2_N , that has an ATM cell to transmit, sends a request-to-send signal 1r to the bus controller 6, which stops a counter 4 that increments addresses in the RAM 3 at the corresponding memory location X, maintaining the address of the interface unit 2_x that sent the request-to-send signal on the address bus 1a. The interface unit that requested transmission receives permission to transmit its cell at the rising edge of the next cell sync pulse (bus signal 1c). The bus controller

simultaneously continues the interrupted incrementing of addresses at the next memory location $X+1$. Those interface units which do not have anything to transmit do not react in any way to the contents of the address bus in the multiplexing direction. The next possible transmitter is looked for simultaneously as the cell of the interface unit 2_x that has been authorized to transmit is being transmitted.

In the multiplexing direction, the interface units thus continuously 'listen' to the address bus 1a, but only an interface unit 2_x with a cell ready for transmission sends a request-to-send signal to the bus controller 6 when it detects its own address on the address bus.

By suitably initializing interface unit addresses in the memory locations of the RAM 3, different interface units 2_1-2_N can advantageously be given a different position in the allocation of the bus 1. If addresses of interface units are initialized in the memory in proportion to their transmission capacity, bus capacity can be allocated in a congestion in proportion to the transmission rate of the interface, i.e. the number of memory locations per interface unit in the memory of the bus controller is in proportion to the rate of each interface unit. For example, an 8 Mbit/s interface thus has 4 times as many addresses as a 2 Mbit/s interface.

It is also possible to assign more addresses to desired interface units than they are actually entitled to in view of their transmission rate, whereby interfaces are prioritized, i.e. the number of memory locations per interface unit in the memory of the bus controller is in proportion to the priority level of the interface unit.

Here addresses of interface units stored in the memory 3 and located on the address bus may mean either addresses in a tabular memory or addresses stored in memory locations according to a rule. In the first case, the address is in a register that is scanned address-by-address, one address at a time; in the second case, the address is fetched from a memory location. Even in the latter case, one memory location is scanned at a time, but not necessarily in the physical order; addresses can thus be prioritized without repeating the same addresses, e.g. by means of prioritization tests varying with the situation.

The bus control according to the invention allows concentration of interface units, whereby the bus controller serves a larger number of interface units than the transmission capacity of the bus would allow if the interface units were used at full capacity.

In the demultiplexing direction, as shown in Fig. 2, the bus controller 6 selects the address of the ATM cell to be transmitted to the receiver 2_1-2_N on the basis of the cell header, the whole or part of the contents of the VPI/VCI field in the cell being used for indicating the memory location of the memory 3 where the bus address of the desired interface unit is located. The address thus obtained is taken to the address bus 1a' of the demultiplexing bus 1', and the original cell is taken to the data bus 1d'. The multiplexing (Fig. 1) and demultiplexing transmission directions thus have their own address and data buses.

The width and detailed timing of the bus (address and data buses 1a, 1d; 1a', 1d') are dependent on the technology available. The bus may either operate as a backplane bus for one multiplexer, or it may extend from one multiplexer to another. When a twisted twin cable is used for extending the bus from one multiplexer

to another, the clock of the bus should be less than 20 MHz (e.g. 19.4 MHz), which leads to 8-bit wide data buses. The width of the address bus depends on the number of units to be multiplexed, but the address space of the bus controller, the memory access rate, and the cell transmission frequency of the bus must be proportioned to one another so that the entire address space can be scanned between two cell sync pulses, i.e. in this example in less than 2.72 μ s, by conducting a poll that covers the addresses of the interface units.

It is obvious to one skilled in the art that the different embodiments of the invention are not limited by the above-described example but that they may vary within the scope of the attached claims.

Claims

1. A method for controlling a statistically multiplexed ATM bus (1; 1'), to the bus being connected a bus controller (6) and interface units (2₁-2_N) for transmission of ATM cells, over the bus, each interface unit having an address selected from an address space, characterized by the following steps carried out by the bus controller (6):

detecting, for each ATM cell to be transmitted to the ATM bus, the address of one of the plurality of the interface units which participates in the transmission,

setting the address on an address bus (1a; 1a') of the ATM bus (1; 1'), thereby activating the transmission of the ATM cell from the bus controller to the interface unit or vice versa over a data bus (1d; 1d') of the ATM bus; and

fetching, during the transmission of the ATM cell, the address of the interface unit from or to which the next ATM cell is to be transmitted.

2. The method according to claim 1, characterized in that in a direction in which multiplexing takes place, the bus controller (6) increments addresses of interface units (2₁-2_N) from the memory (3) onto the address bus (1a), whereby an interface unit having an ATM cell ready for transmission sends a request-to-send signal to the bus controller (6) when the interface unit detects its own address on the address bus.

3. The method according to claim 1 or 2, characterized in that in a direction in which demultiplexing takes place, the bus controller (6) reads an identifier of the current interface unit from the address field of multiplexed ATM cells to be transmitted to the interface units (2₁-2_N).

4. The method according to claim 1, 2 or 3, characterized in that the address space of the bus controller (6), the memory access rate, and the cell transmission frequency of the bus are proportioned to one another so that the entire address space can be scanned between two cell sync pulses of the bus (1; 1') by conducting a poll that covers the addresses of the interface units (2₁-2_N).

5. The method according to any one of claims 1 to 4, characterized by providing the bus controller (6) with a memory (3) having a number of memory locations per interface unit which is in proportion to the transmission capacity of each of the plurality of interface units (2_1 - 2_N).

6. The method according to any one of claims 1 to 4, characterized by providing the bus controller (6) with a memory (3) having a number of memory locations per interface unit which is in proportion to a priority level of each of the plurality of interface units (2_1 - 2_N).

7. The method according to any one of claims 1 to 6, characterized in that the bus controller (6) offers a concentrated service for a larger number of interface units (2_1 - 2_N) than the transmission capacity of the bus would allow if the interface units were used at full capacity.

8. A system for controlling a statistically multiplexed ATM bus, the system comprising a bus controller (6) transmitting ATM cells, over the bus (1; 1'), and interface units (2_1 - 2_N) connected to the controller by means of the bus, characterized in that the bus controller (6) is provided with a memory (3) for storing addresses of the interface units (2_1 - 2_N) and for each ATM cell to be transmitted to an ATM bus, the address of the interface unit participating in the transmission is read from the memory (3) and set on an address bus (1a; 1a') of the ATM bus (1; 1'); and that the bus controller (6) is arranged to:

transmit the ATM cell over a data bus (1d; 1d') of the ATM bus (1; 1') from the bus controller to the interface unit or vice versa,

during the transmission of the ATM cell, fetch the address of the interface unit which is to transmit the next ATM cell to the bus.

9. The system according to claim 8, characterized in that the bus controller (6) is arranged to scan the address space of the bus controller (6) between two ATM cell sync pulses by conducting a poll that covers the addresses of the interface units (2_1 - 2_N).

10. The system according to claim 8 or 9, characterized in that to the ATM bus (1; 1') are connected a larger number of interface units (2_1 - 2_N) than the transmission capacity of the ATM bus would allow if the interface units were transmitting or receiving at full capacity.

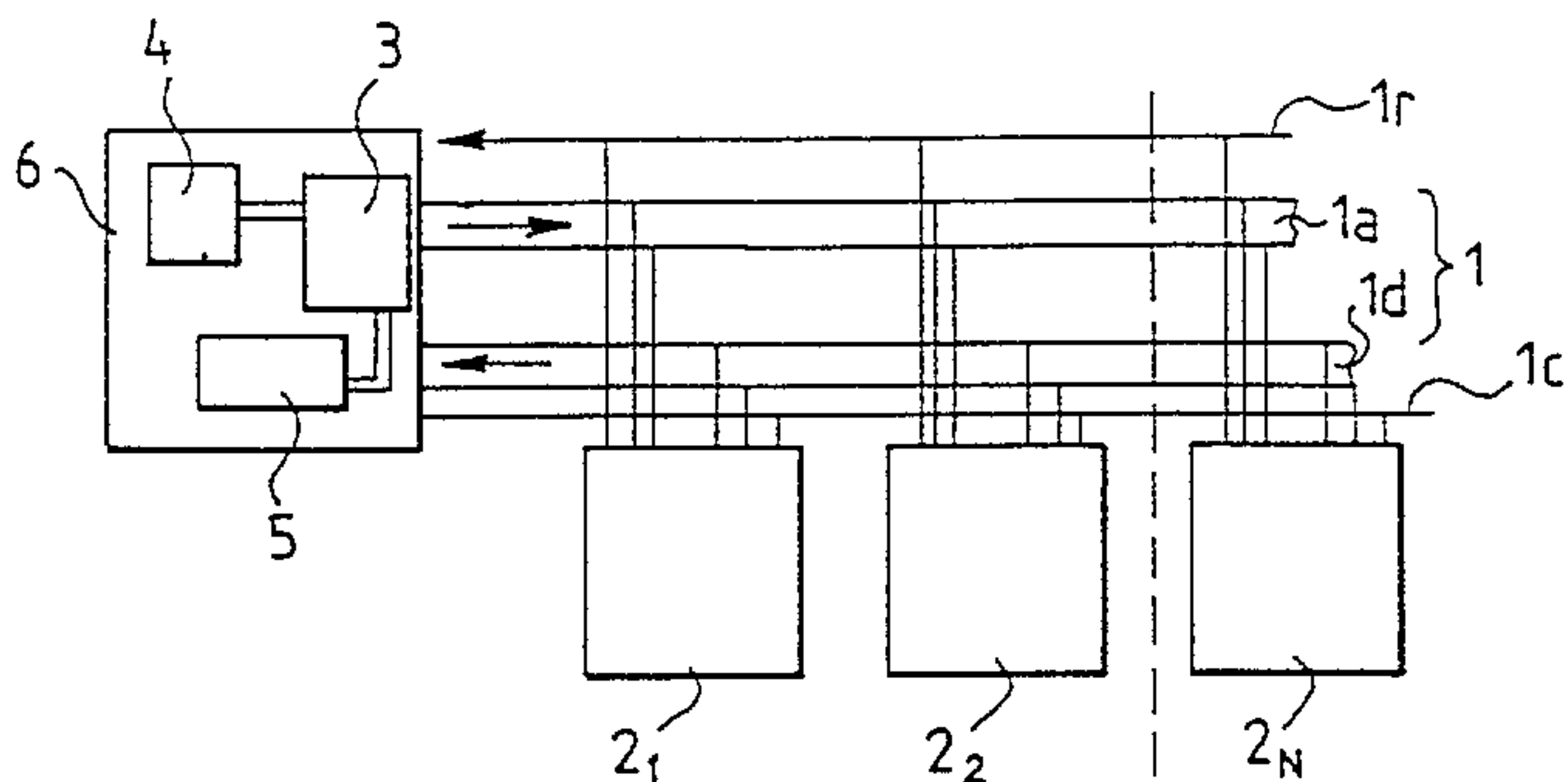


FIG. 1

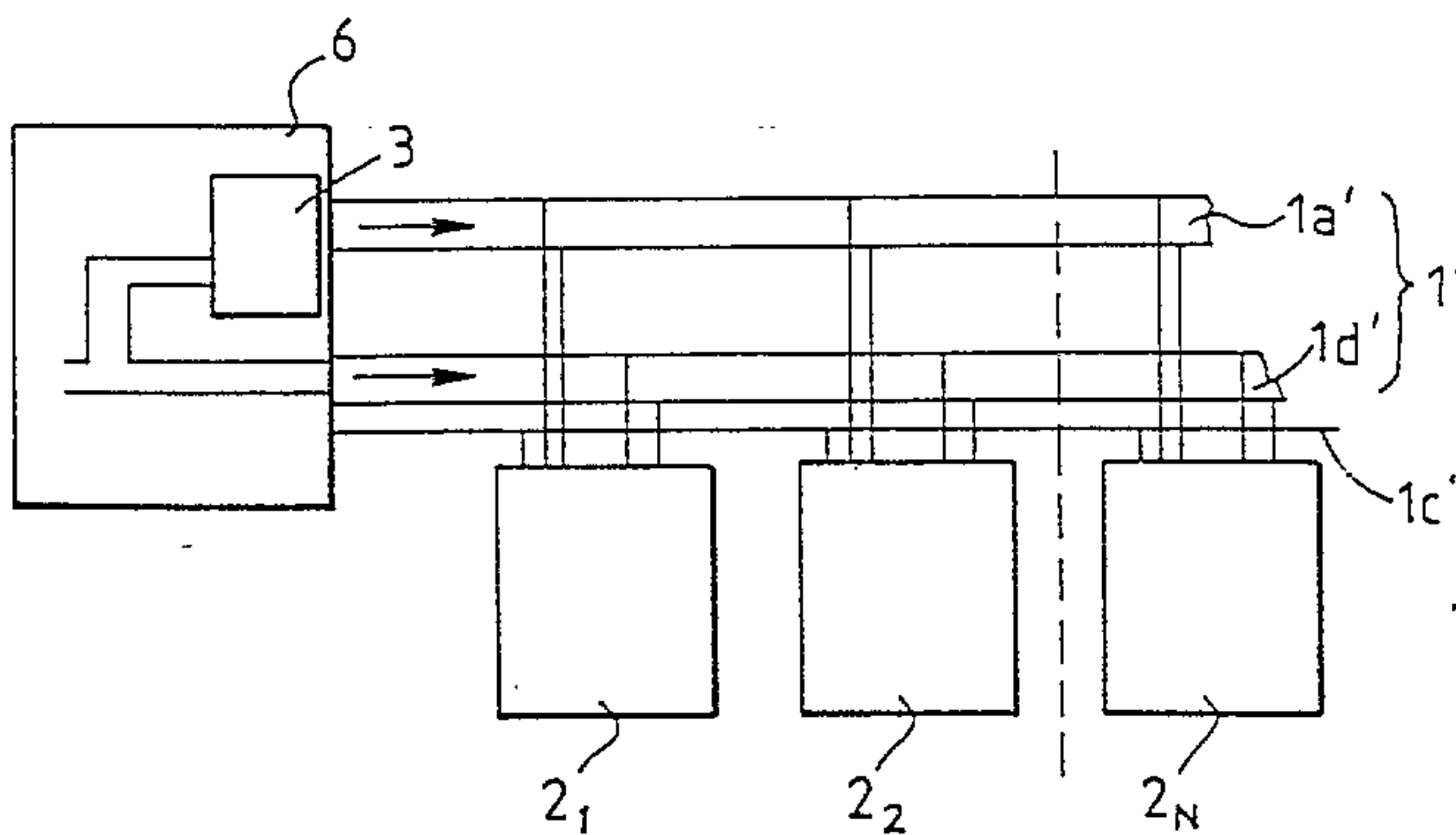


FIG. 2

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