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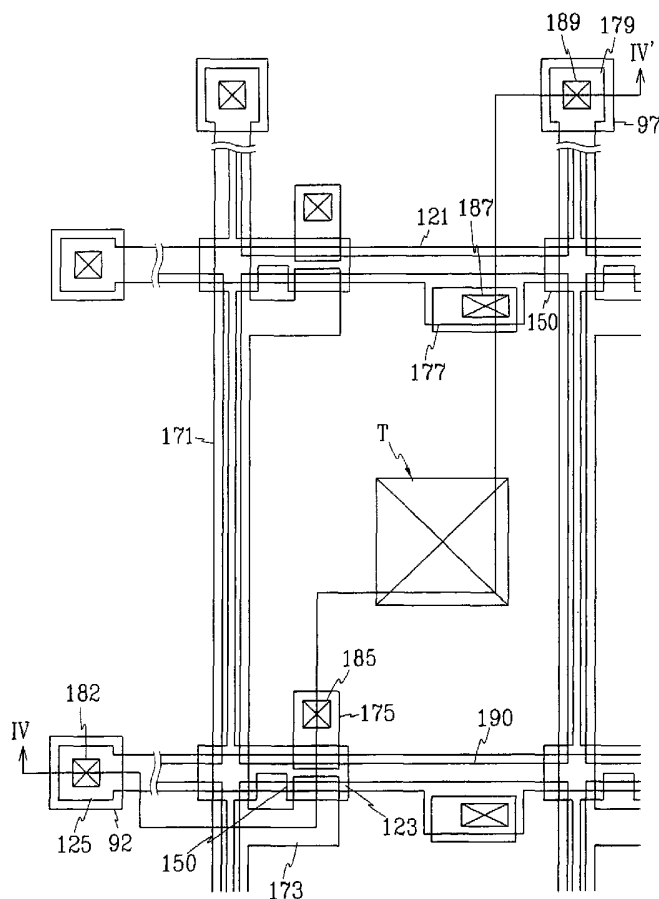
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(54) Title: LIQUID CRYSTAL DISPLAY



(57) Abstract: A liquid crystal display according to an embodiment of the present invention is divided into a display area seen as screen to a user and a peripheral area surrounding the display area. A plurality of pixel areas defined by intersections of a plurality of signal lines are provided on the display area, while a plurality of dummy pixel areas are provided on a portion of the peripheral area. The pixel areas are defined by intersections of a plurality of gate lines extending in a transverse direction and a plurality of data lines extending in a longitudinal direction, while the pixel areas in the peripheral area are defined by intersections of the gate lines and plurality of dummy data lines. Pixel electrodes include transparent films and reflective films. The reflective film in each dummy pixel area has a larger area than the reflective film in each pixel area such that it blocks light from a light source through the dummy pixel area. It is preferred that the reflective film in the peripheral area preferably has no hole exposing the transparent film and covers entire area of the dummy pixel area.



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LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

(a) Field of the Invention

5 The present invention relates to a liquid crystal display.

(b) Description of the Related Art

A typical liquid crystal display ("LCD") includes an upper panel having a common electrode and an array of color filters, and a lower panel having a plurality of pixel electrodes and thin film transistors ("TFT"s). A pair of aligning
10 films are coated on the upper and the lower panels, and a liquid crystal layer is interposed between the aligning films of the upper and the lower panels. The orientations of molecules of the liquid crystal layer are changed by adjusting an electric field generated by the potential difference between the pixel electrodes and the common electrode, which are applied with appropriate voltages. The
15 change of the orientations of the liquid crystal molecules causes the transmittance of light passing through the LCD to be varied, thereby obtaining desired images.

During the fabricating process of such a conventional LCD, impurity ions are often generated and remained on the surface of the aligning films. After
20 the fabricated LCD operates for a time, these impurity ions travel along an alignment direction formed by rubbing the aligning films, to gather at one corner of the liquid crystal display. As a result, this causes a defect that one corner of a display area is bright when displaying dark images.

SUMMARY OF THE INVENTION

25 An object of the present invention is to provide liquid crystal displays having structures with improved image qualities.

The present invention for accomplishing the object locates at least one pixel electrode in a peripheral area external to a display area, and the pixel electrode in the peripheral area includes a reflective film having an area larger
30 than an area of a reflective film of the pixel electrode in the display area.

In detail, a liquid crystal display includes a first insulating substrate including a display area represented as a screen and including a plurality of pixel areas and a peripheral area located outside the display area and a dummy pixel area and a plurality of signal lines provided on the first substrate.

5 The liquid crystal display further includes a plurality of pixel electrodes electrically connected to the signal lines and located in the pixel areas and the dummy pixel area, each pixel electrode including a transparent film made of transparent conductive material and a reflective film made of reflective conductive material. The reflective film of the pixel electrode in the dummy
10 pixel area has an area larger than the reflective films in the pixel areas.

Preferably, the liquid crystal display further includes a second insulating substrate disposed opposite the first substrate and a black matrix provided on the second substrate, the black matrix screening the second pixel electrodes.

15 It is preferable that the liquid crystal display further includes a common electrode provided on the second substrate and disposed opposite the pixel electrodes, and the pixel electrodes and the common electrode are supplied with signals having periodically inverting polarity.

The pixel electrodes are arranged in a matrix, the signal lines include a
20 plurality of gate lines extending substantially parallel to each other in a row direction and a plurality of data lines extending substantially parallel to each other in a column direction, and the liquid crystal display further includes a plurality of switching elements transmitting first signals from the data lines to the pixel electrodes in response to second signals from the gate lines.

25 The reflective film of the pixel electrode in the dummy pixel area preferably covers substantially entire area of the dummy pixel area, and the reflective film of the pixel electrode in the pixel area preferably has a hole exposing a portion of the transparent film.

The present invention will be described hereinafter with reference to the
30 accompanying drawings, in which preferred embodiments of the invention are

shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, substrate or panel is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic plan view of an LCD according to an embodiment of the present invention;

FIG. 2 is a sectional view taken along the line II-II' shown in FIG. 1;

FIG. 3 is an exemplary enlarged layout view of a pixel area in a display area and a pad area shown in FIG. 1;

FIG. 4 is a sectional view taken along the line IV-IV' shown in FIG. 3;

FIG. 5 is an exemplary enlarged layout view of a pixel area in a peripheral area shown in FIG. 1; and

FIG. 6 is a sectional view taken along the line VI-VI' shown in FIG. 5.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Then, TFT array panels for liquid crystal displays and liquid crystal displays including the same according to embodiments of the present invention will be described with reference to the drawings.

First, a schematic structure of an LCD according to an embodiment of the present invention is described with reference to FIGs. 1 to 6.

FIG. 1 is a schematic plan view of an LCD according to an embodiment of the present invention; FIG. 2 is a sectional view taken along the line II-II' shown in FIG. 1; FIG. 3 is an exemplary enlarged layout view of a pixel area in a display area and a pad area shown in FIG. 1; FIG. 4 is a sectional view taken along the line IV-IV' shown in FIG. 3; FIG. 5 is an exemplary enlarged layout

view of a pixel area in a peripheral area shown in FIG. 1; and FIG. 6 is a sectional view taken along the line VI-VI' shown in FIG. 5.

As shown in FIG. 1, an LCD according to an embodiment of the present invention includes a liquid crystal panel assembly 100, a gate printed circuit board ("PCB") 200, a data PCB 300, a plurality of gate tape carrier packages ("TCP"s) 400, a plurality of data TCPs 500, and two flexible printed circuit ("FPC") films 600. The gate TCPs 400 are attached to the panel assembly 100 and the gate PCB 200, and the data TCPs 500 are attached to the panel assembly 100 and the data PCB 300. The FPC films 600 connect the panel assembly 100 to the gate PCB 200 and connect the gate PCB 200 to the data PCB 300. The gate PCB 200 and the data PCB 300 are disposed external to the left and the right edges of the panel assembly 100, respectively.

As shown in FIGs. 1 and 2, the panel assembly 100 includes a thin film transistor (TFT) array panel 1 and a color filter panel 2, opposite each other. The panel assembly 100 further includes a liquid crystal layer 3 of liquid crystal material disposed in a gap between the two panels 1 and 2, and a sealant 4 supporting the two panels 1 and 2 and sealing the liquid crystal material.

The TFT array panel 1 is divided into a display area 5 seen as a screen to a user of an LCD and a peripheral area 6 surrounding the display area 5. A plurality of pixel areas AP defined by intersections of a plurality of signal lines 121 and 171 are provided on the display area 5, while a plurality of dummy pixel areas DP are provided on a portion of the peripheral area 6. The pixel areas AP are defined by intersections of a plurality of gate lines 121 extending in a transverse direction and a plurality of data lines 171 extending in a longitudinal direction, while the pixel areas DP in the peripheral area 6 are defined by intersections of the gate lines 121 and a plurality of dummy data lines 172. The peripheral area 6 includes a plurality of gate pad areas 250 and a plurality of data pad areas 790, where the gate pads and the data pads connected to one ends of the gate lines 121 and the data lines 171 are crowded. A plurality of pixel electrodes 190 electrically connected to the gate lines 121 and the data lines 171 via TFTs are provided on the pixel areas AP, while a plurality of dummy pixel

electrodes 109 connected to the gate lines 121 and the dummy data lines 172 via TFTs are provided on the dummy pixel areas DP.

The LCD according to this embodiment is a transfective LCD operating in a transmissive mode and a reflective mode, and thus the pixel electrodes 190 and 109 include transparent films and reflective films having holes in the pixel areas. The reflective film in each dummy pixel area DP has a larger area than the reflective film in each pixel area AP such that it blocks light from a light source through the dummy pixel area DP. It is apparent that the reflective film in the peripheral area preferably has no hole exposing the transparent film.

A TFT array panel having an above-described pixel structure according to an embodiment of the present invention is described more in detail with reference to FIGs. 1-6.

A gate wire transmitting scanning signals or gate signals is formed on an insulating substrate 110 preferably made of transparent glass. The gate wire includes a plurality of gate lines 121 extending in a row direction, a plurality of gate electrodes 123 connected thereto, and a plurality of gate pads 125 connected to one ends of the gate lines 121.

The gate wire 121, 123 and 125 is covered with a gate insulating film 140, and a semiconductor layer 150 preferably made of amorphous silicon or polysilicon is formed on the gate insulating film 140 opposite the gate electrode 123. An ohmic contact layer including two separated portions 163 and 165 is formed on the semiconductor layer 150. The ohmic contact layer 163 and 165 is preferably made of amorphous silicon doped with high concentration N-type impurity such as phosphorous.

A data wire transmitting image signals or data signals is formed on the gate insulating film 140 and the ohmic contact layer 163 and 165. The data wire includes a plurality of data lines 171 extending in a column direction, a plurality of source electrodes 173 connected thereto, a plurality of drain electrodes 175 separated from the data lines 171 and the source electrodes 173, and a plurality of data pads 179 connected to one ends of the data lines 171.

One gate electrode 123, one source electrode 173 and one drain electrode 175 serve as three terminals of a TFT, and a portion of the semiconductor layer 150 interposed between the source electrode 173 and the drain electrode 175 acts as a channel layer of the TFT.

5 As described above, adjacent two gate lines 121 and adjacent two data lines 171 or adjacent two dummy data lines 172 define a pixel area AP or a pixel area DP as shown in FIGs. 1, 3 and 5.

The data wire 171, 173, 175 and 179, and exposed portions of the semiconductor layer 150 and the gate insulating film 140 are covered with a passivation layer 180, which has contact holes 185 exposing the drain electrodes 175. The passivation layer 180 and the gate insulating layer 140 has a plurality of contact holes 182 and 189 exposing the gate pads 125 and the data pads 189. The passivation layer 180 has unevenness on its surface for increasing the reflective efficiency of reflective films which will be formed later.

15 A plurality of pixel electrodes 190 and a plurality of dummy pixel electrodes 109 are formed on the passivation layer 180. Each pixel electrode 190 or 109 includes a transparent film 191 preferably made of a transparent conductive material such as indium zinc oxide (IZO) and indium tin oxide (ITO) and a reflective film 192 preferably made of highly-reflective opaque conductive material such as Ag and Al. The pixel electrodes 190 and 109 are connected to the drain electrodes 175 through the contact holes 185 so that the TFTs provide the image signals from the data lines 171 and 172 to the pixel electrodes 190 and 109 in response to the scanning signals from the gate lines 121. As shown in FIGs. 3 and 4, the reflective film 192 of the pixel area AP has a hole T exposing the transparent film 191 and located at the center of the pixel area AP, while the reflective film 192 in the dummy pixel area DP covers entire area of the dummy pixel area DP as shown in FIGs. 5 and 6.

25 An aligning film 290 forms an uppermost layer of the TFT array panel 1 as shown in FIG. 2, and the aligning film 290 is rubbed in a direction indicated by arrows shown in FIG. 1, i.e., in the direction from the upper left to the lower right.

Next, the color filter panel 2 will be described with reference to FIGs. 1 and 2.

A black matrix 220 preferably made of an organic material is formed on an insulating substrate 210 preferably made of transparent glass. The black matrix 220 surrounds and defines the display area 5. The black matrix 220 overlaps the dummy pixel electrodes 109 in the dummy pixel areas DP. Although it is not shown, the black matrix 220 screens the borders between the regular pixel electrodes 190 to define the pixel areas AP and to prevent light leakage between the pixel areas AP. Red, green and blue color filters (not shown) are formed in respective pixel areas AP of the display area 5. A common electrode 230 preferably made of transparent conducting material is formed on the color filters and the black matrix 220 and covers the entire area of the substrate 210. An aligning film 292 forms an uppermost layer of the color filter panel 2, and the rubbing direction thereof is the same as that of the aligning film 290 of the TFT array panel 1.

As can be seen in FIGs. 1 and 2, since the TFT array panel 1 is larger than the color filter panel 2, the pad areas 250 and 790, where the gate pads 125 and the data pads 179 are disposed, are located outside the color filter panel 2. The sealant 4 is located external to the display area 5 and interposed between the two panels 1 and 2. The sealant 4 partly overlaps the black matrix 220.

The gate PCB 200 and the data PCB 300 are electrically connected via the FPC film 600 therebetween for signal transmission. Signal paths 610 and 310 preferably made of conducting wires for transmitting signals are provided on the PCBs 200 and 300 and the FPC film 600 therebetween. An LCD controller 700 is provided on the data PCB 300 but it may be provided on the gate PCB 200. A driving voltage generator (not shown) is also provided on the gate PCB 200. The driving voltage generator 900 generates a gate-on voltage, a gate-off voltage and a common voltage. A gray voltage generator (not shown) generating a plurality of gray voltages is provided on the data PCB 300. At least one of the gate PCB 200 and the data PCB 300 may be omitted, and then the associated circuits and signal paths may be formed in the TFT array panel 1.

A plurality of gate driving integrated circuits (ICs) 410 and the data driving ICs 510, preferably made in chips, are mounted on the gate TCPs 400 and the data TCPs 500, respectively. A plurality of leads (not shown) connected between the gate driving ICs 410 and the signal path 610 and between the gate driving ICs and the gate lines 121 are formed on the gate TCPs 410. Another plurality of leads (not shown) connected between the data driving ICs 510 and the signal path 310 and between the data driving ICs 510 and the data lines 171 are formed on the data TCPs 500.

The gate TCPs 400 and the data TCPs 500 are respectively attached to the gate PCB 200 and the data PCB 300 to be electrically connected thereto, and are attached to the panel assembly 100 to be electrically connected to the gate lines 121 and the data lines 171, respectively. Alternatively, the gate driving ICs 410 and/or the data driving ICs 510 are mounted on the TFT array panel 1, which is called a COG (chip on glass) type. Alternatively, the gate driving ICs 410 and/or the data driving ICs 510 are substituted with driving circuits formed in the TFT array panel 1, which are made of the same layers as the gate lines 121, the data lines 171 and the TFTs.

The LCD controller 700 provides a plurality of red, green and blue image signals for the data driving ICs 510 and a plurality of control signals for the driving ICs 410 and 510 via the signal paths 610 and 310 on the PCBs 200 and 300 and the FPC film 600 to control the driving ICs 410 and 510. The gate driving ICs 410 generate the scanning signals based on the gate-on voltage and the gate-off voltage from the driving voltage generator 900 to apply to the gate lines 121 via the gate pads 125 thereof in synchronization with the control signals from the LCD controller 700. The data driving ICs 510 select the gray voltages from the gray voltage generator based on the image signals from the LCD controller 700 to apply as the data signals to the appropriate data lines 171 via the data pads 179 thereof in synchronization with the control signals from the LCD controller 700.

In this LCD, the impurity ions on the surface of the aligning films 290 and 292 travel along the rubbing direction, and gather at in the rightmost

columns, in particular, at the dummy pixel areas DP near the lower right corner. As described above, since the dummy pixel electrodes 109 in the rightmost columns overlap the black matrix 220, the area with defect image caused by such ions is screened by the black matrix 220. Furthermore, the dummy pixel electrodes 109, which cover entire area of the dummy pixel areas DP, block the light from a light source. Accordingly, the LCD according to this embodiment compensates the defects in the dummy pixel areas DP.

The dummy pixel areas DP may be elongated portions of the rightmost pixel areas AP in the display area 5.

In order to supply signals to the dummy pixel electrodes 109, a plurality of dummy signal lines such as a plurality of dummy data lines 172 and dummy pads connected thereto are provided. Preferably, the dummy signal lines have the same shapes and are formed by the same method as the gate lines 121, the data lines 171 and their pads 125 and 179.

As shown in FIG. 1, an additional signal path or signal paths such as 320 for electrically connecting the dummy signal lines 172 to an LCD controller 700 are provided on the data PCB 300 and/or the gate PCB 200 and/or the FPC film 600.

Although preferred embodiments of the present invention have been described in detail hereinabove, it shall be clearly understood that many embodiments having variations and/or modifications of the basic inventive concepts herein taught are possible, which may appear to those of ordinary skill in the pertinent art based on the teachings herein. Such embodiments will fall within the spirit and scope of the present invention, as defined in the appended claims.

As described above, the transfective LCD according to an embodiment of the present invention overlaps the dummy pixel areas with the black matrix and makes reflective films of the dummy pixel areas cover the entire surface, thereby preventing the defect that one corner of a display area is bright.

WHAT IS CLAIMED IS:

1. A liquid crystal display comprising:
a first insulating substrate including a display area represented as a
5 screen and including a plurality of pixel areas and a peripheral area located
outside the display area and a dummy pixel area;
a plurality of signal lines provided on the first substrate; and
a plurality of pixel electrodes electrically connected to the signal lines
and located in the pixel areas and the dummy pixel area, each pixel electrode
10 including a transparent film made of transparent conductive material and a
reflective film made of reflective conductive material,
wherein the reflective film of the pixel electrode in the dummy pixel
area has an area larger than the reflective films in the pixel areas.
2. The liquid crystal display of claim 1, further comprising:
15 a second insulating substrate disposed opposite the first substrate; and
a black matrix provided on the second substrate, the black matrix
screening the second pixel electrodes.
3. The liquid crystal display of claim 2, further comprising a
common electrode provided on the second substrate and disposed opposite the
20 pixel electrodes, wherein the pixel electrodes and the common electrode are
supplied with signals having periodically inverting polarity.
4. The liquid crystal display of claim 1, wherein the pixel
electrodes are arranged in a matrix, the signal lines include a plurality of gate
lines extending substantially parallel to each other in a row direction and a
25 plurality of data lines extending substantially parallel to each other in a column
direction, and the liquid crystal display further comprises a plurality of
switching elements transmitting first signals from the data lines to the pixel
electrodes in response to second signals from the gate lines.
5. The liquid crystal display of claim 1, wherein the reflective film
30 of the pixel electrode in the dummy pixel area covers substantially entire area of
the dummy pixel area.

6. The liquid crystal display of claim 2, wherein the reflective film of the pixel electrode in the pixel area has a hole exposing a portion of the transparent film.

1/6

FIG.1

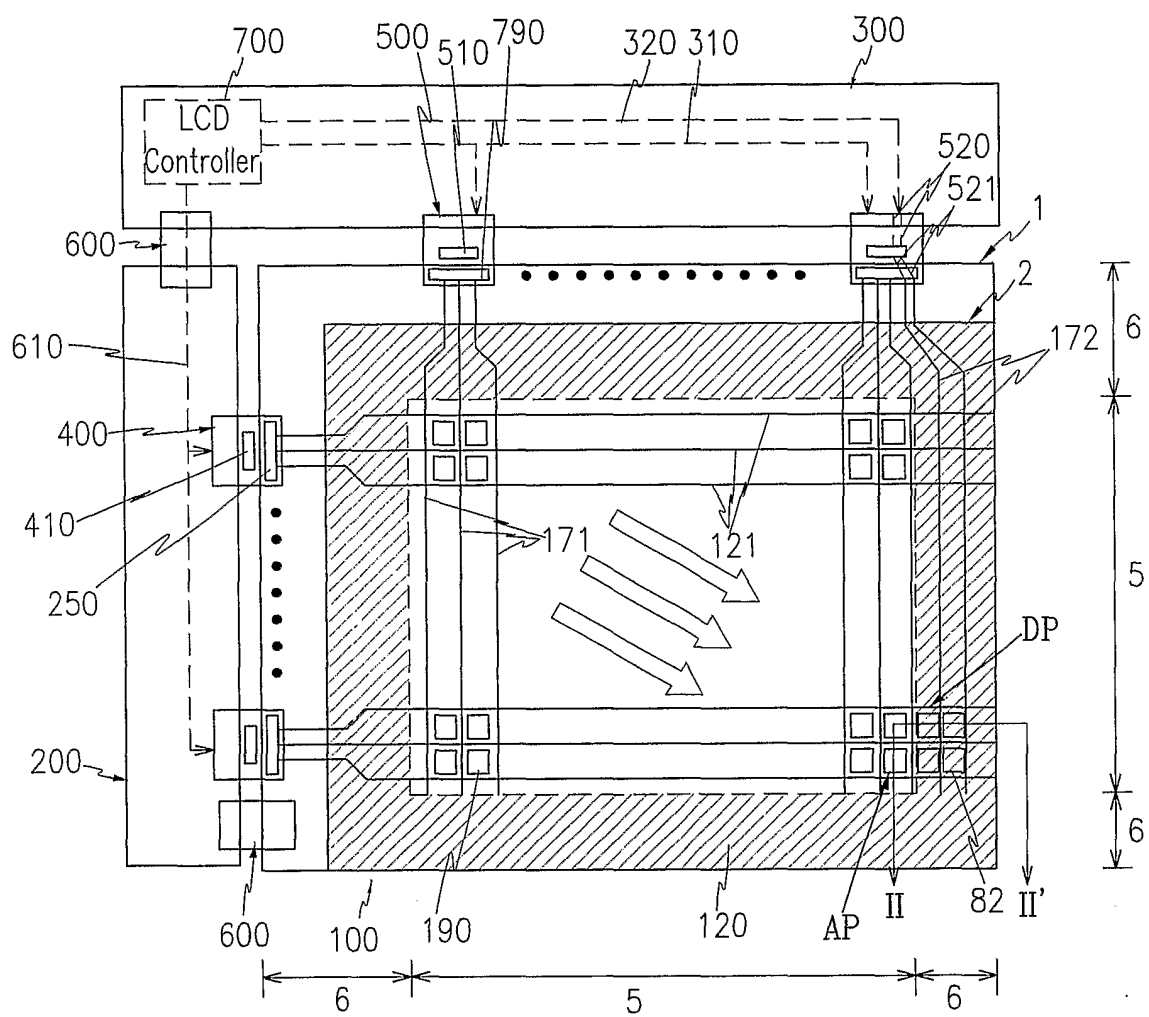


FIG.3

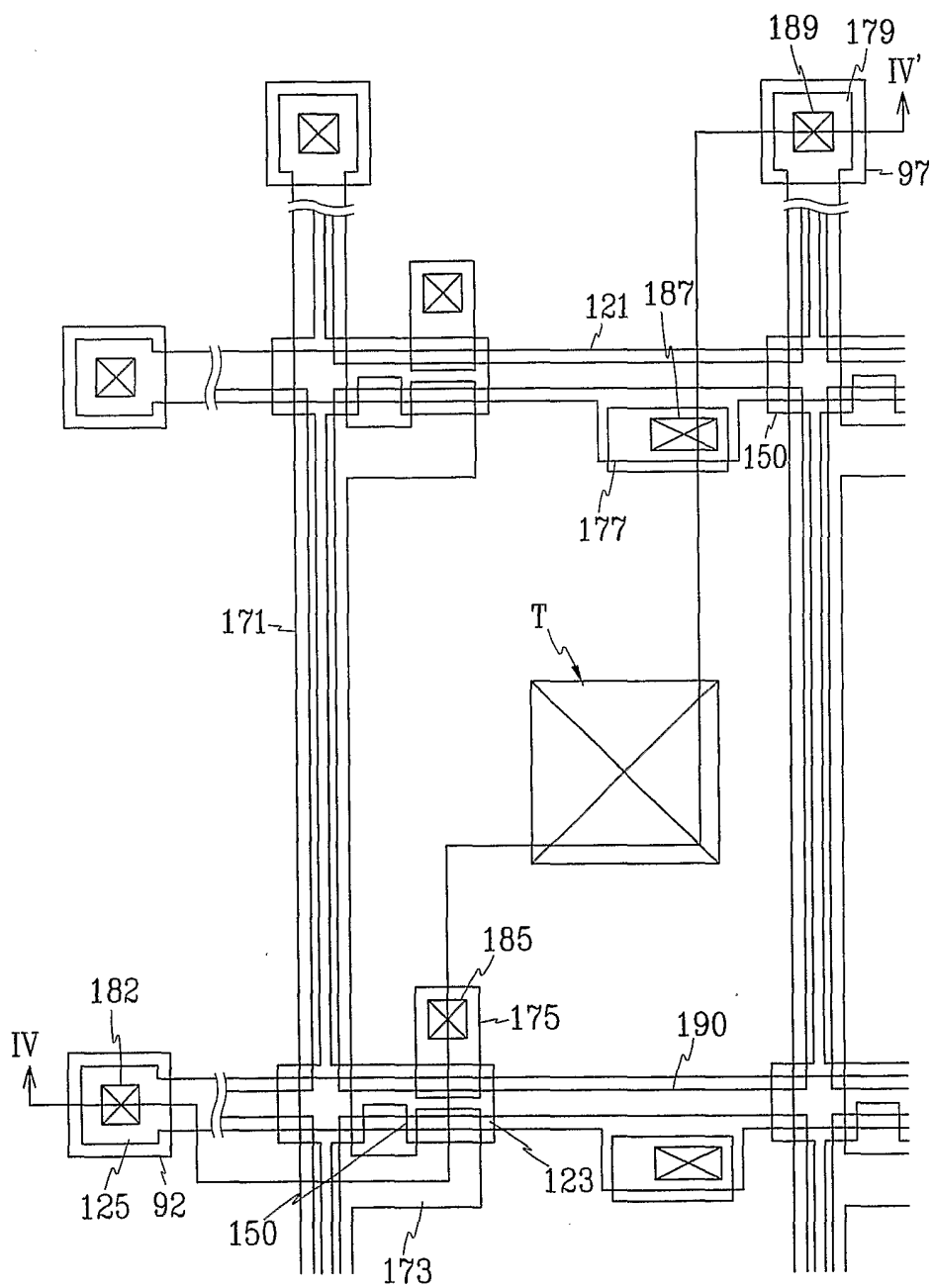
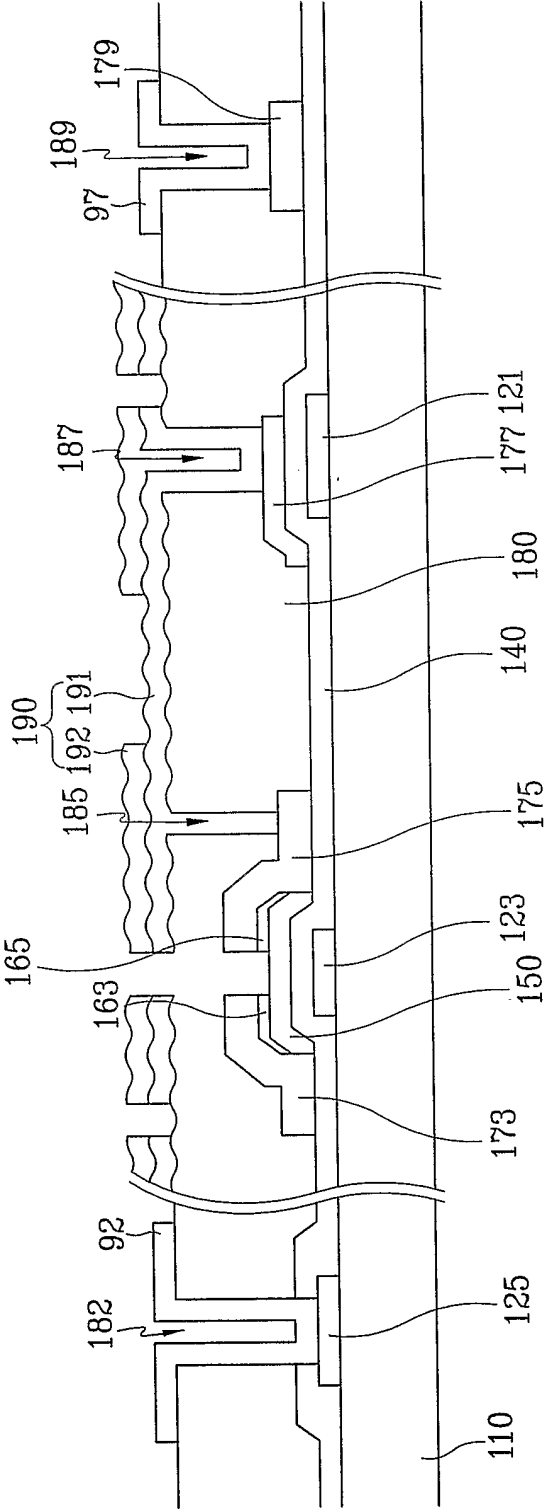


FIG. 4



5/6

FIG.5

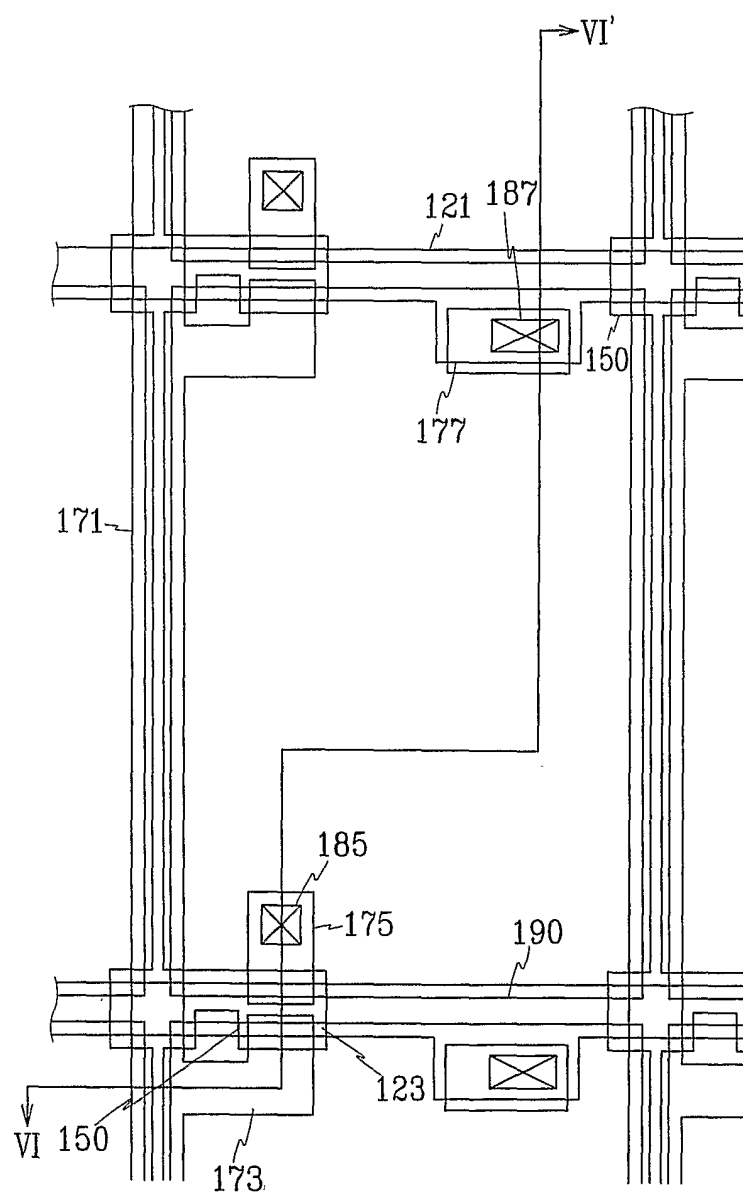
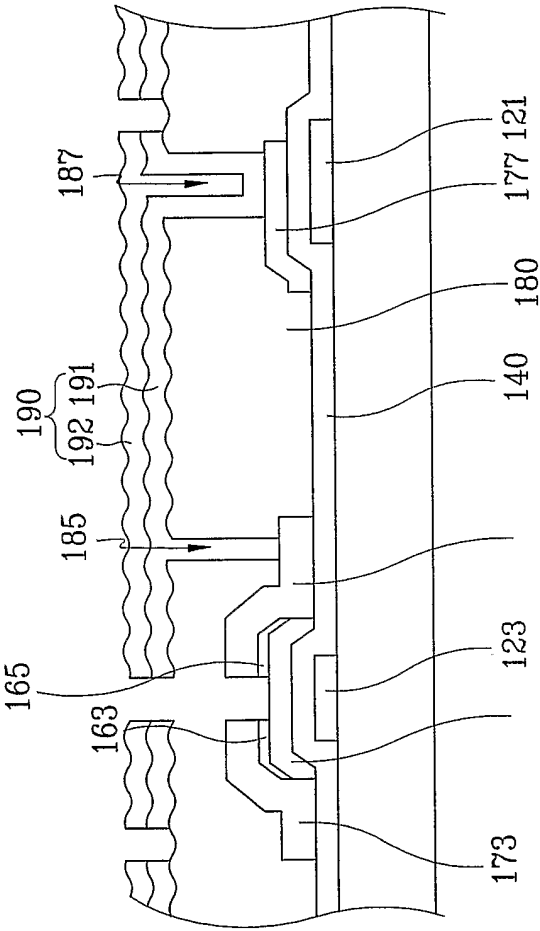


FIG. 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR02/01759

A. CLASSIFICATION OF SUBJECT MATTER**IPC7 G02F 1/1335**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 G0F G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KP JP:IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

KIPO DB

search term:dumy, electrode, reflect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6195140 B1(Sharp Kabushiki Kaisha) 27 February 2001 See the whole document	1-6
A	JP 2002-217587 A(ALPS ELECTRIC CO LTD) 02 August 2002 See the whole document	1-6
A	JP 2002-202521 A(OPTREX CORP, HIROSHIMA OPT CORP) 19 July 2002 See the whole document	1-6

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

15 MAY 2003 (15.05.2003)

Date of mailing of the international search report

16 MAY 2003 (16.05.2003)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR02/01759

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6195140 B1	27-02-2001	JP 2000-19563 A	21-01-2000
JP 2002-217587 A	02-08-2002	KR 2002-0061511 A	24-07-2002
JP 2002-202521 A	19-07-2002	NONE	