(12) UK Patent Application (19) GB (11) 2 043 975 A

(21) Application No 7943735
(22) Date of filing 19 Dec 1979
(30) Priority data
(31) 53/165454
(32) 19 Dec 1978
(33) Japan (JP)
(43) Application published 8 Oct 1980
(51) INT CL³ G06F 15/38 H03K 13/24 // G06F 3/023
(52) Domestic classification G4H 13D 14A 14B 14D 1A DC KU
(56) Documents cited
GB 1448211
GB 1387032
GB 1381159
GB 1293573
GB 1291556
GB 1043330
GB 1018330
(58) Field of search G4A G4H
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(54) Word storage for language translation

(57) A word entered on a keyboard can be translated into another language by comparison with words in a ROM, each accompanied by the translated word and other information e.g. part of speech. The entered and translated words and other information are displayed. A slider 4 can switch the device between dictionary mode (above) and calculator mode, the keyboard indicia being on a sheet slid into a corresponding one of two positions to be visible through the keys.

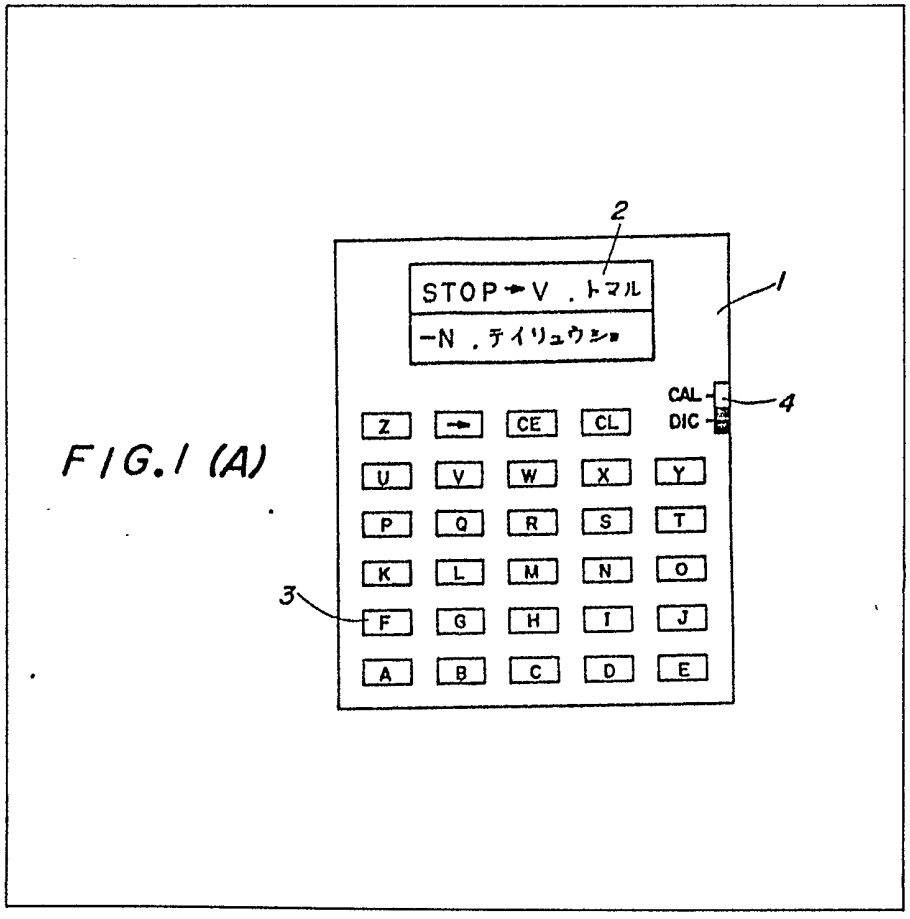

FIG. 1 (A)

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FIG. 1 (A)

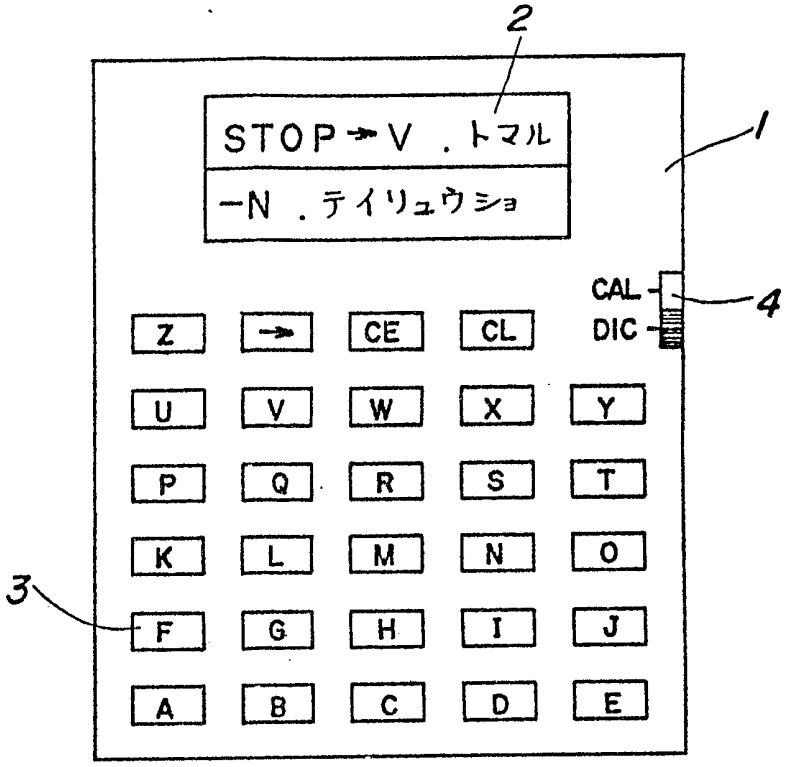

FIG. 1 (B)

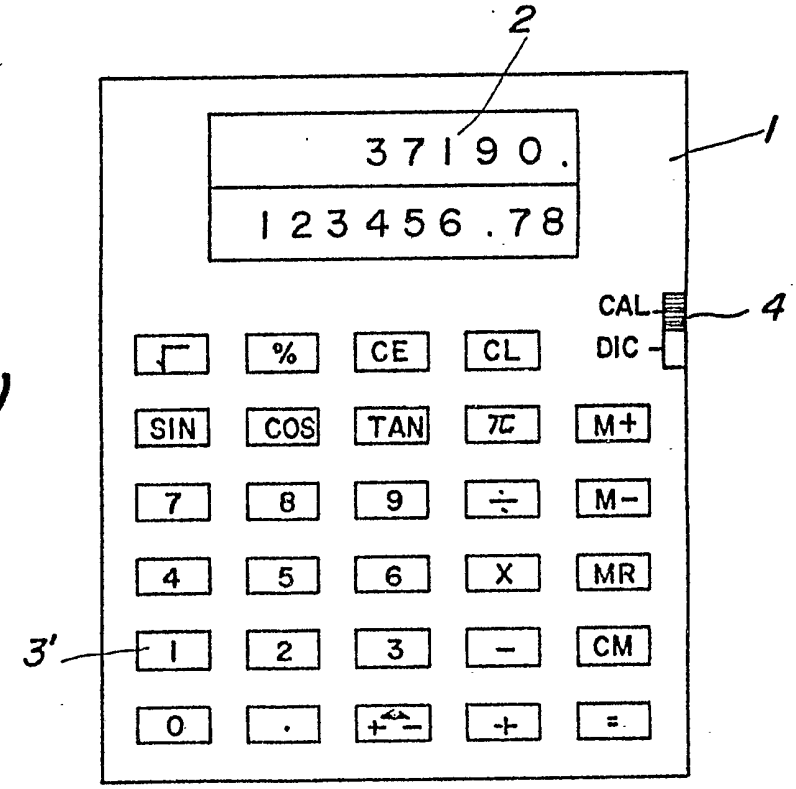

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FIG.2 (A)

37190.
123456.78

FIG.2 (B)

WAY →N・ミチ・ホ
ウコウ・ホウホウ

FIG.2 (C)

STOP →V・トマル
→N・テイリュウショ

FIG.2 (D)

FIVE →N・ゴ〔5
〕

FIG.2 (E)

NOSE →N・ハナ〔
カオ〕

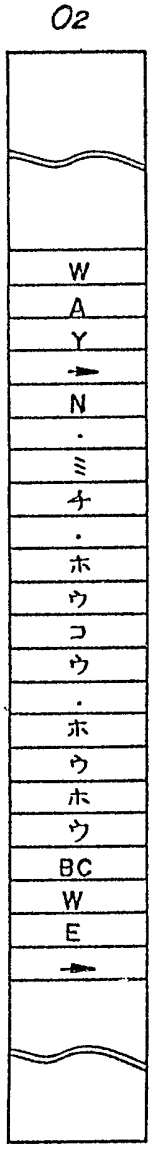

FIG.6

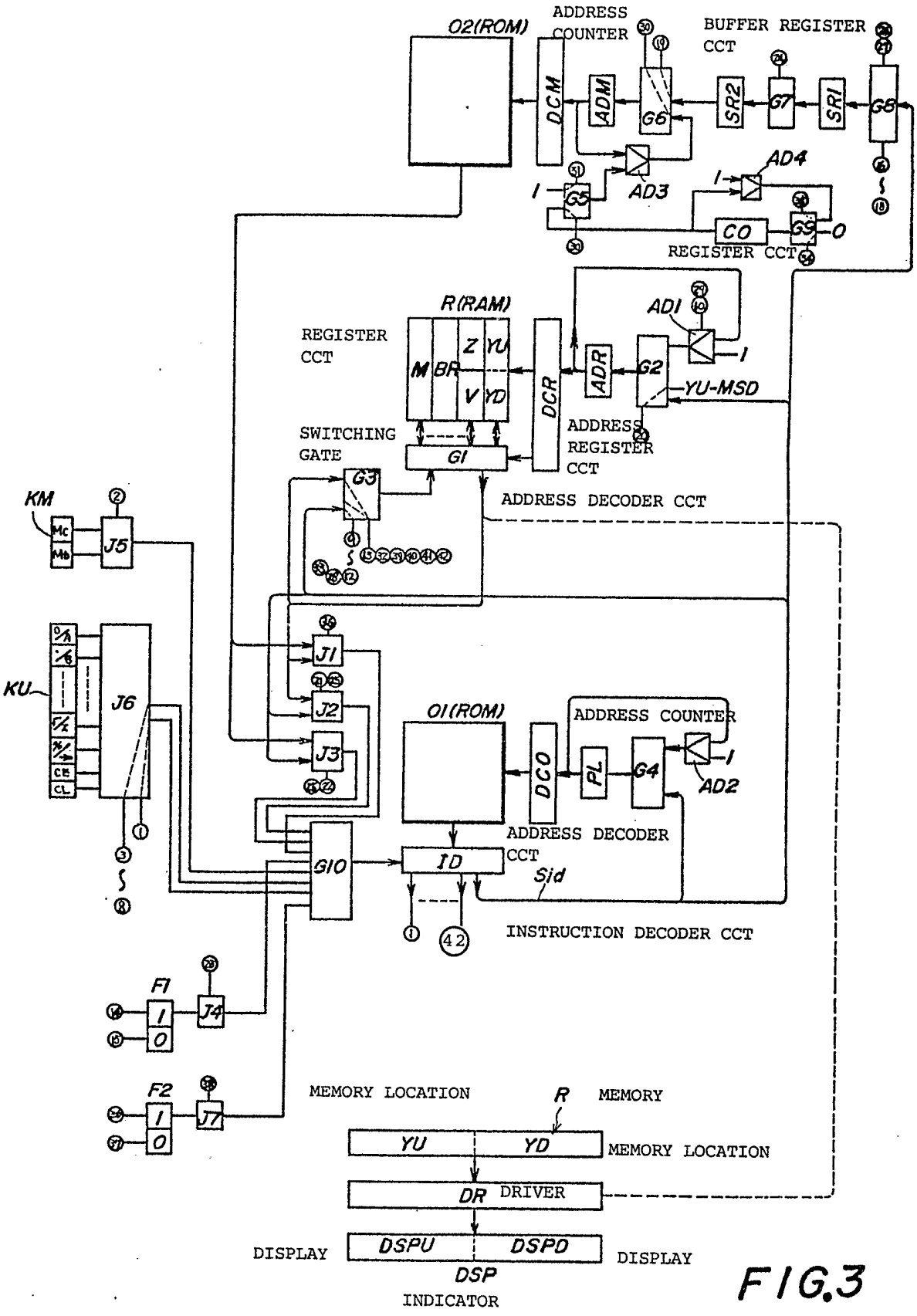
O2(ROM)
ADDRESS COUNTER
BUFFER REGISTER CCT
DCM
ADM
G6
SR2
G7
SR1
G5
AD3
AD4
CO
REGISTER CCT
R(RAM)
REGISTER CCT
M
BR
Z
YU
V
YD
DCR
ADR
G2
ADI
YU-MSD
SWITCHING GATE
GI
ADDRESS REGISTER CCT
G3
ADDRESS DECODER CCT
KM
Mc
Mb
J5
KU
J6
J1
J2
J3
O1(ROM)
DCO
PL
G4
AD2
ADDRESS DECODER CCT
G10
ID
Sid
INSTRUCTION DECODER CCT
F1
J4
F2
J7
MEMORY LOCATION
R MEMORY
YU
YD
MEMORY LOCATION
DR DRIVER
DISPLAY
DSPU
DSPD
DISPLAY
DSP
INDICATOR

FIG.3

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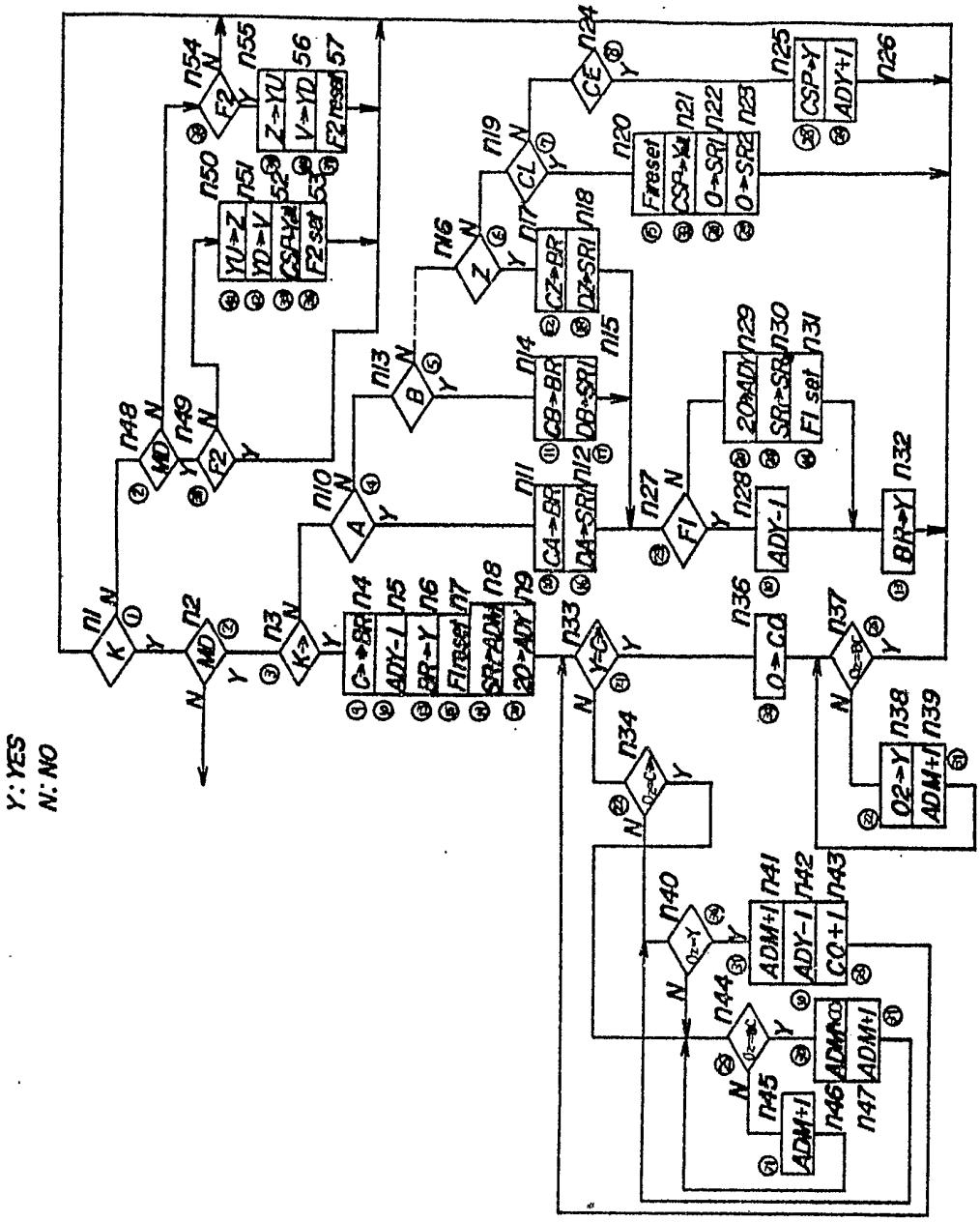

FIG.4

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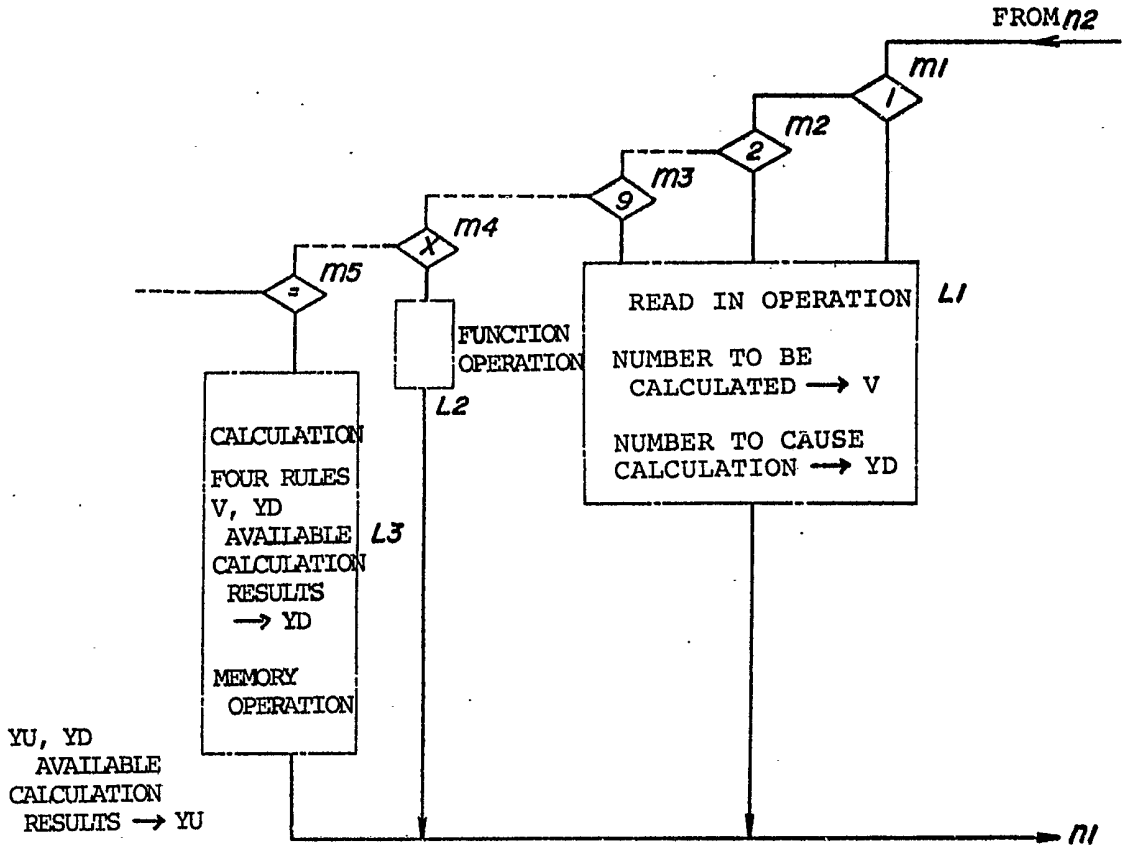

FIG.5

SPECIFICATION

Word information storage device

BACKGROUND OF THE INVENTION

The present invention relates to a word information storage device and more particularly to an electronic dictionary and language interpreter.

Nowadays, electronic dictionaries and language interpreters have been placed in markets which provides for efficient and repid retrieval of word information which is stored in a memory. Outline of such the electronic dictionaries and language interpreters is shown in, for example, Levy U.S. Pat. No. 4,158,236 issued June 12, 1979, entitled "ELECTRONIC DICTIONARY AND LANGUAGE INTERPRETER".

In the electronic dictionaries and language interpreters, it is desirous that a part of speech or other index information relevant to a specific word in question is simultaneously developed.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide an improved electronic dictionary and language interpreter for taking out a part of speech or other index information related to a specific word in question.

A further object of the present invention is to provide an improved electronic dictionary and language interpreter for performing calculation operations in addition to word information retrieval in connection with a specific word with a part of speech or other index information.

A further object of the present invention is to provide an improved electronic dictionary and language interpreter having means for searching and indicating a plurality of parts of speech and/or translated words.

Other objects and further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

To achieve the above objects, pursuant to an embodiment of the present invention, a word information storage device is adapted to obtain parts of speech or other index information in addition to translated words according to the entrance of a specific word. The part of speech and other index information are preliminarily stored in a memory such as ROM together with the relevant translated words. The word information storage device causes retrieval of the parts of speech and other index information, and the translated words corresponding to the specific word entered. The word information storage device is further adapted to function as an electronic calculator by selection. A keyboard is provided to be operated as an alphabetical keyboard in a word information searching mode and as a numeral keyboard in an electronic calculator mode, both caused in the word information storage device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention and wherein:

FIG. 1(A) is a plan view of a combined electronic dictionary and electronic calculator according to the present invention, which is placed in an electronic dictionary mode;

FIG. 1(B) is a plan view of the combined electronic dictionary and electronic calculator identical to that shown in FIG. 1(A), the combined electronic dictionary and electronic calculator being placed in an electronic calculator mode;

FIGS 2(A) to 2(E) are plan views of an indicator of the combined electronic dictionary and electronic calculator of the present invention, showing various indicating states of the indicator;

FIG. 3 is a block diagram of a control circuit incorporated into the combined electronic dictionary and electronic calculator of the present invention;

FIGS. 4 and 5 are flow charts caused with the control circuit shown in FIG. 3; and

FIG. 6 is a schematic and exemplary representation of the contents of a memory used in connection with the present invention.

DESCRIPTION OF THE INVENTION

With reference now to FIGS. 1(A) and 1(B), there is indicated a combined electronic dictionary and electronic calculator of the present invention. In particular, FIG. 1(A) shows the combined electronic dictionary and electronic calculator, referred to only as a combined device hereinafter, placed in an electronic dictionary mode. FIG. 1(B) represents the same combined device operated in an electronic calculator mode.

In Figs. 1(A) and 1(B), there are provided a cabinet 1, an indicator 2, a plurality of keys 3 or 3', and a

mode selection switch 4. The plurality of keys 3 shown in FIG. 1(A) are used in connection with the electronic dictionary mode. The plurality of numeral keys 3' depicted in FIG. 1(B) are operated in conjunction with the electronic calculator mode. Although the alphabetical key 3 is equivalent to the key 3', two separate representations as the key 3 or 3' are adopted to clearly indicate different functions of the alphabetical key 3 and the numeral key 3'. That is, one key has a specific function in the electronic dictionary mode while the same key designates another different function in the electronic calculator mode.

The mode selection switch 4 is actuated to select one from the electronic dictionary mode (DIC) and the electronic calculator mode (CAL). At least two kinds of indicias are labeled on the top of the respective keys 3 and 3'. Instead, the indicias for the keys may be changed in accordance with the selection by the mode selection switch 4 as disclosed in M. KOIKE et al U.S. Pat. Application Ser. No. 26,568 filed April 3, 1979, entitled "THIN KEYBOARD WITH CHANGEABLE KEY INDICIA", assigned to the present applicant. A copy of the specification filed with that U.S. application is hereunto annexed as Appendix 1. As the details of the change of the indicia for the keys are shown in U.S. Pat. Application S. N. 26,568, further description thereof is omitted.

A clear key "CL" and a clear entry key "CE" are operated to cause common operations throughout the two modes. The indicator 2 is a two storied structure. In the electronic dictionary mode, there are indicated a specific word and its corresponding translated word in the indicator 2 from the upper indicator to the lower indicator of the two-stored structure. In the electronic calculator mode, on the other hand, the upper indicator of the two-storied structure in the indicator 2 is used, for example, to show numeral information stored in a memory while the lower indicator thereof is used to indicate numeral information entered and calculated.

FIGS. 2(A) to 2(E) show various examples of indicated states in the two-stored indicator 2. In particular, FIG. 2(A) is an indication in the electronic calculator mode while FIGS. 2(B) to 2(E) are indications in the electronic dictionary mode.

The indications in the electronic dictionary mode are performed in the following principle.

In FIG. 2(B):

WAY→N・ミチ・ホウコウ・ホウホウ

where WAY : an entered word in English

→ : a separation indication

N : an indicia of noun

・ : a separation indication

ミチ, ホウコウ, ホウホウ : three translated words in Japanese corresponding to the entered word

In FIG. 2(C):

stop→V・トマル - N・テイリュウジョ

where stop an entered word in English

→ : a separation indication

V : an indicia of verb

: a separation indication

トマル : a translated word in Japanese as a verb corresponding to the entered word

— : a separation indication

N : the indication of noun

: the separation indication

テイリュウジョ : another translated word in Japanese as a noun corresponding to the entered word

In FIG. 2(D):

FIVE → N・ゴ゛ [5]

where FIVE : an entered word in English

→ : the separation indication

N : the indication of noun

: the separation indication

ゴ゛[5] : a translated word in Japanese corresponding to the entered word, representing a kind of figures by the symbol [5] to thereby divide the translated word from "GO" and the like.

In FIG. 2(E):

NOSE → N・ハナ [カオ]

where NOSE : an entered word in English

→ : the separation indication

N : the indication of noun

: the separation indication

ハナ [カオ] : a translated word in Japanese corresponding to the entered word, showing a part of a face, another translated word of the "face" being provided within a bracket to thereby separate the translated word corresponding to the "NOSE" from that of a flower

FIG. 3 shows a block diagram of a control circuit incorporated into the combined device of the present invention. With reference to FIG. 3, a random access memory (RAM) R is provided which comprises four kinds of register circuits Y, Z, M, and BR. An address register circuit ADR is employed to address the RAM R.

An address decoder circuit DCR is provided for addressing the RAM R. A switching gate G1 is operated to switch the RAM R. An adder and subtractor AD1 is provided to cause adder or subtraction by control. There are provided two gate circuits G2 and G3.

A read only memory (ROM) 01 contains a plurality of programs for causing calculation operations and word retrieval. An element denoted as PL is an address counter for the ROM 01. A circuit defined by DCO is an address decoder circuit for the ROM 01. A circuit shown by ID is an instruction decoder circuit. A circuit denoted by G4 is a gate circuit. A circuit shown by AD2 is an adder. The instruction decoder circuit ID generates micro instructions ① through ㊷ and an operand Sid which are applied to relevant circuit elements as indicated in FIG. 3.

An additional memory depicted by 02 is another read only memory (ROM). A counter denoted as ADM is an address counter fo the RAM 02. A decoder circuit shown by DCM is an address decoder circuit for the RAM 02. A circuit denoted by AD3 is an adder. Circuits indicated by G6, G7, G8 and G9 are each a gate circuit. Circuits indicated by SR1 and SR2 are buffer register circuits. A circuit shown by CO is a register circuit as a counter. A circuit indicated by AD4 is an adder.

An element depicted by KU is a keyboard containing a plurality of keys 3 and 3'. An element denoted by KM represents the mode selection switch 4. A comparison circuit denoted as J_1 is provided for comparing output signals from the ROM 02 with that of the register circuits Y, Z, M, and BR. Another comparison circuit indicated by J2 is employed to compare output signals from the register circuits Y, Z, M, and BR to the operand Sid. A further comparison circuit shown by J_3 functions to accomplish comparison between output signals from the ROM 02 and the operand Sid. A gate circuit G10 is connected so that output signals from the gate circuit G10 control the instruction decoder circuit ID so as to prevent the circuit ID from generationg the micro instructions and allow the same to skip, as used for jump operations of programs.

A circuit shown by F1 is an RS type flip flop circuit. A judge circuit J4 is connected to the RS type flip flop circuit F1 to determine output signals from the flip flop circuit F1. Another RS type flip flop circuit F2 is provided. Another judge circuit J7 is coupled to the RS type flip flop circut F2 to judge the output signals from the flip flop circuit F2. A further judge circuit J5 is connected to the mode selection

switch KM to judge mode selection states. A still further judge circuit F6 is coupled to the keyboard KU to determine key input information. An indicator DSP comprises two separate displays DSPU and DSPD as the two-storied structure. A driver circuit PR is interposed between the indicator DSP and a memory R consisting of two memory locations YU and UD. The contents stored in the memory location YU are indicated in the display DSPU while the contents kept in the memory location YD are shown in the display DSPD.

FIG. 4 shows a flow chart in actuating various circuit elements shown in FIG. 3. In accordance with the flow chart indicated in FIG. 4, the operations of the subject combined device will be described hereinbelow.

All the steps shown in FIG. 4 have respective labels indicating kinds of the microinstructions 1 to 42 developed from the instruction decoder circuit ID. Each micro-instruction is labeled to indicate that it activates its relevant step.

[Electronic Calculator Mode]

The electronic calculator mode is executed where the mode selection switch 4 is placed in DIC position as indicated in FIG. 1(A).

The actuation of the mode selection 4 to the DIC positionis identical to excitation of a switch MD of the mode selection switch KM shown in FIG. 3. As long as no key of the keyboard KU is actuated under the condition that the preceding operations have been placed in the electronic calculator mode before the time, the program repeats steps $n_1 \rightarrow n_{48} \rightarrow n_{54} \rightarrow n_1$. Then when the switch MD is selected so as to execute the electronic dictionary mode, the program advances steps $n_1 \rightarrow n_{48} \rightarrow n_{49}$.

As the flip flop circuit F_2 is placed in a reset state at the final of the preceding electronic calculator mode, the program proceeds to step n_{50}.

In the preceding electronic calculator mode, the two register circuits YU and YD store the contents to be memoried and either calculation results or entered numeral information, respectively. The contents of YU and YD are transferred to the other register circuits Z and V to assure that the contents of Z and V can be continuously utilized in the next electronic calculator mode after the preceding electronic calculator mode has been replaced by the electronic dictionary mode and then the electronic dictionary mode is changed to the next electronic calculator mode. In step n_{52}, suppress code information CSP is introduced into all the storage portions of the Y register circuit comprising the two register circuits YU and YD to become ready for the introduction of the word information in the electronic dictionary mode. That is, the contents of all the storage portions of the Y register circuit are canceled. In step n_{53}, the flip-flop circuit F_2 is turned to be set so that the circuit F_2 memories the conduction of the switch MD. And then the program turns back to step n_1. Then the program advances steps $n_1 \rightarrow n_{48} \rightarrow n_{49} \rightarrow n_1$.

[Enter of A Specific Word for Retrieval Purposes in the Electronic Dictionary Mode]

Prior to the description of the enter of a specific word for retrieval purposes in the electronic dictionary mode, the ROM 02 is described in detail.

FIG. 6 shows the contents of the ROM 02 where a train of code information each representing a character is stored in order.

The ROM 02 stores a plenty of trains.

The order of words each positioned in a leading address of each train is alphabetical, from "A" to "Z". According to a preferred embodiment of the present invention, a specific train of the code information designating a specific English word such as "WAY" and other information thereto are shown in FIG. 6.

The code information corresponding to three characters "W", "A" and "Y" is stored from a leading address of a certain train as indicated in FIG. 6. A specific English word "WAY" is initially stored in the certain train.

A separation indication designating "→" is subsequently stored to indicate that the following character is a character for showing a part of speech related to the specific English word. Code information representing the part of speech is successively stored. In this instance, a character indicative of "N" as noun is stored. Code information indicating another separation indication "." is memoried to divide the part of speech from a translated Japanese word. After the separation indication ".", the translated Japanese word is stored in the form of code information. When there are a plurality of the translated Japanese words, the separation indications "." are allotted to divide them. A boundary code BC is interposed between the translated Japanese words in connection with "WAY" and the following English specific word "WE".

The ROM 02 preliminarily stores a number of trains each containing a specific English word and one or more translated Japanese words together with the indicia of the part of speech as mentioned in connection with FIG. 6. Needless to say, other languages rather than English or Japanese can be used within the knowledge of the present invention.

Turning back to the description about the electronic dictionary mode, the above defined ROM 02

is addressed as follows. In the electronic dictionary mode, one or more translated Japanese words corresponding to a specific English word "WAY" are obtained by the actuation of the alphabetical keys 3 in the order of "W", "A", "Y" and "→" as shown in FIG. 2(B).

After the switch MD is selected to perform the electronic dictionary mode, a certain alphabetical key 3 designating a character "W" is actuated in which case the key actuation is detected in step n_1. And then the program leads to steps $n_1 \rightarrow n_2 \rightarrow n_3$. Step n_3 is performed to detect the actuation of another search key representing "→".

But at the time, step n_{10} is executed because the search key is not actuated. Steps n_{10} through n_{16} are programmed so as to determine what kinds of the alphabetical keys 3 are actuated.

Although detecting procedure in detecting the actuation of the alphabetical key 3 representative of "w" is not shown in FIG. 4, it can be easily recognized from the other detecting procedures in detecting the actuation of the other characters "A", "B" and "Z" as indicated. Provided that the alphabetical key 3 related to the character "B" is actuated, the program advances steps $n_3 \rightarrow n_{10} \rightarrow n_{13} \rightarrow n_{14}$, whereby code information CB corresponding to the character "B" is entered into the register circuit BR in the last n_{14} step, the code information CB being equivalent to that stored in a certain train of the ROM 02. Therefore, when the alphabetical key 3 directed to the character "w" is actuated, code information equal to the character "w" is admitted into the register circuit BR.

In the following step n_{15}, provided that the alphabetical key 3 directed to the character "B" is actuated, step values DB of trains of the ROM 02 for directing all the trains whose leading address has the character of "B" in the form of the code information is temporarily stored in the buffer register circuit SR1. Similarly, when the alphabetical key 3 directed to the character "w" is actuated, the buffer register circuit SR1 is adapted to have the step values of the trains in the ROM 02 for directing all the trains the leading address of which has the character of "w" in the form of the code information.

After the buffer register circuit SR1 receives the step values of the rains, step n_{27} is performed to detect what number of the characters is entered into the control circuit by the keyboard actuation once or more times. As the flip flop circuit F1 is initially placed in a reset state, step n_{29} is executed. 20→ADY caused in step n_{29} means that an address corresponding to the supreme digit of the register circuit Y is preliminarily selected. In step n_{30}, the contents stored in the buffer register circuit SR1 are transferred into the other buffer register circuit SR2 under the conditions where the first character information is now entered. In the following step n_{31}, the flip flop circuit F_1 is turned reset so that steps $n_{27} \rightarrow n_{28}$ are conducted in response to the actuation of the second character "A" belonging to the specific English word "WAY".

In step n_{32}, BR→Y is conducted so that the code information equivalent to the character now entered. "W" is entered to the register circuit Y. As 20→ADY is conducted in step n_{29} in connection with the entrance of the first character "w", the supreme degit of the register circuit Y receives code information CZ equivalent to the first character "w".

As indicated in FIG. 3, the contents of the register circuit Y is indicated in the indicator DSP. The first character "w" entered is displayed in the supreme degit of the indicator DSP. After step n_{32} is executed, the program returns back to step n_1.

Under the circumstances, the second alphabetical key 3 designating "A" is subsequently actuated. An actuation of the second alphabetical key 3 enables step $n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_{10} \rightarrow n_{11}$. In step n_{11}, code information CA equivalent to the character "A" is introduced into the register circuit BR. In step n_{12}, the buffer register circuit SR1 would have address information DA defined to direct to all the leading addresses of the ROM 02 in which the code information equivalent to the character "A" should be stored, if the character "A" were the firstly entered character. Since actually the character "A" is the secondary entered character, the above presumed operation is not carried out.

The program proceeds step $n_{27} \rightarrow n_{28}$ as the flip flop circuit FL is set. In step n_{28}, ADY — 1 is performed which means the subtraction of one address from the addresses stored in the register circuit Y. This is responsive to the following step n_{32} where the code information representative of the alphabetical character stored in the register circuit BR is transmitted to the second degit of the register circuit Y.

As described above, the entered character information is subsequently entered into the register circuit Y by the successive actuation of the alphabetical keys 3 and then displayed in the indicator DSP for confirmation purposes. When erroneous actuation of the alphabetical keys 3 is found out the clear entry key "CE" is energized. In such a case, in step n_{25}, suppress code information is entered into the degit of the register circuit Y which receives now the erroneous character information. Then, in the following step n_{26}, ADY + 1 is conducted to arise the addresses of the register circuit Y by one, namely, to refresh the register circuit Y. Therefore, when the program proceeds to step n_{28} under the condition that a correct character is entered, it is assumed that the same address of the register circuit Y be selected. When it is desired that all the character information be canceled, the clear key "CL" is actuated to conduct steps n_{20} to n_{23}. In such a case, the suppress code information is entered into all the degits of the register circuit Y to clear the buffer register circuits SR1 and SR2 and to allow the flip flop circuit F1 to be reset.

[Execution of Retrieval of One or More Translated Words]

After the specific English word is accurately entered, the search key "→" is actuated to perform the retrieval of one or more translated words. The program advances steps $n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4$. Code information responsive to the actuation of the search key "→" is entered into the register circuit BR in step n_4. In step n_5, by the calculation of ADY — 1, one address is subtracted from the address of the register circuit Y. In step n_6, the register circuit Y has the code information equivalent to "→" which is stored into the register circuit BR. This code information is utilized to indicate the separation indication between the English word entered and the translated Japanese word. The reset state of the flip flop circuit F1 caused in step n_7 is to become responsive to the following introduction of the English word as the entrance of the preceding English word "WAY" is completed. In step n_{30}, the buffer register circuit SR2 has the information of all the leading addresses of the ROM 02 in which the head character should be stored. As the head character is assumed to be "w" according to a preferred embodiment of the present invention, the code information directing to the head character "w" is DZ. Since the code information stored in the buffer register circuit SR2 is transferred to the address counter ADM for the ROM 02 in step n_8, it occurs that the address of the ROM 02 is adapted to select the leading addresses in which the first character "w" should be stored. In the following step n_9, it is set that the supreme degit of the register circuit Y be re-selected. Under the conditions where the entered characters are "WAY", it is apparent that the degit containing the character "w" be adapted for selection purposes.

The following step n_{33} is executed to determine whether output signals from the register circuit Y are equivalent to the code information "C→" designating "→". If so, it is directed that all the retrieval procedures are completed. If the contents of the register circuit Y are not coincident with that code information, step n_{34} is performed.

In step n_{34}, it is determined whether the output signals from the ROM 02 are equivalent to the code information "C→" indicating the separation indication "→". The detection performed in step n_{34} is significant in the statue that the number of the entered English characters to cause the retrieval is larger than the number of the English characters stored in the ROM 02. When the output signals from the ROM 02 represent the code information "C→" under the conditions where the register circuit Y has the code information "C→", steps $n_{34} \rightarrow n_{44}$ are executed so as to cause the retrieval of the following English characters stored in the ROM 02 as described below.

When the English word "WAY" should be searched to find out one or more translated Japanese words, the program advances steps $n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow n_6 \rightarrow n_7 \rightarrow n_8 \rightarrow n_9 \rightarrow n_{33} \rightarrow n_{34}$ immediately after the actuation of the search key. In such a case, the output signals from the ROM 02 is the code information of the character W stored in the leading address of the first train belonging to a group of certain trains which are characterized in that all the leading addresses have the character w. For example, the first train is assumed to be representative of a certain English word such as "WAIT". Accordingly, the register circuit Y provides the output signals representing the character "w". And, it is determined that 02 ≠ C→ and the program proceeds to step n_{40}. As 02 = Y, steps $n_{40} \rightarrow n_{41}$ are executed. For the purpose of successively causing the comparison between the English word entered and one of the English words stored in the ROM 02, in step n_{41}, ADM + 1 is executed to advance the address of the ROM 02 by one so that the code information representing the second character "A" in connection with the word of the first train "WAIT" is developed from the ROM 02. In the following step n_{42}, ADY — 1 is performed to direct the following degit for comparison purposes. At the same time, the code information designating the second character A of the entered word "WAY" is developed from the register circuit Y.

In step n_{43}, CO + 1 is executed to memory the coincident degit between the entered word and one of the words stored in the ROM 02 so as to minimize searching period of time for the following character of the words stored in the ROM 02. Since a coincidence is established between the first character "w" of the entered word "WAY" and the same "w" of the stored word "WAIT", CO + 1 is performed for the register circuit CO to become "1", the register circuit CO being initially reset.

Thereafter, the program returns back to step n_{33} under the condition where in steps n_{41} and n_{42}, the addresses of the register circuit Y and the ROM 02 are advanced by one. As the second characters of the entered word "WAY" and the stored word "WAIT" are both the character "A", the program proceeds to steps $n_{33} \rightarrow n_{34} \rightarrow n_{40} \rightarrow n_{41} \rightarrow n_{42} \rightarrow n_{43}$ to thereby determine CO = 2. Accordingly, the program advances steps $n_{33} \rightarrow n_{34} \rightarrow n_{40}$. The third character "Y" in connection with the entered word "WAY" is stored in the register circuit Y while the third character "I" with respect to the stored word "WAIT" is stored in the ROM 02. Therefore, 02 ≠ Y is established to advance steps $n_{40} \rightarrow n_{44}$.

In step n_{44}, a determination whether the output signals from the ROM 02 are equivalent to the boundary code BC is caused. In the absence of the boundary code BC, the program advances steps $n_{44} \rightarrow n_{45}$ to step up the address of the ROM 02. Under the circumstances, the third character "I" of the stored word "WAIT" is brought out. In step n_{44}, the output signals from the ROM 02 are the code information designating the character "T". Therefore, the program proceeds to step n_{45}. In this way, the address counter ADM for the ROM 02 is counting up until the ROM 02 generates the boundary code BC as the output signals. In other words, the data of the ROM 02 are skipped in connection with the stored word "WAIT". When the boundary code BC develops from the ROM 02, the boundary code BC being stored for indicating that the translated word corresponding to the word "WAIT" is completely

developed, 02 = BC is accomplished to proceed to step n_{46}.

In step n_{46}, ADM + CO is executed under the condition that CO = 2. ADM + 2 is therefore performed so that the address of the ROM 02 to be selected is increased by two. Since the two characters "WA" from the head of the words "WAY" and "WAIT" are coincident, two-degits address of the ROM 02 is skipped. In step n_{47}, ADM + 1 is executed to add one to ADM + CO in step n_{46} with the object of selecting the third character of the word for comparison purposes.

If it is assumed that the word following the word "WAIT" stored in the ROM 02 is "WALL", the ROM 02 develops the code information representing the third character "L" of the stored word "WALL".

Although the condition 02 = Y is tested in step n_{40}, the equation 02 = Y is not established since the register circuit Y maintains the code information designating the third character "Y" of the word "WAY". Accordingly, the program repeats steps $n_{44} \rightarrow n_{45}$ to cause the boundary code BC to develop from the last address of the train containing a specific word and its translated words. After 02 = BC, ADM + CO + 1 is executed. Provided that the word "WAY" is stored immediately after the word "WALL" and its translated words, the ROM 02 provides the code information representing the third character "Y" of the stored word "WAY" by the calculation ADM + CO + 1.

02 = Y is accomplished in step n_{40}. The program proceeds steps $n_{41} \rightarrow n_{42} \rightarrow n_{43} \rightarrow n_{33}$. The register circuit Y is caused to select the lower degit by one in step n_{42}. When the search key "→" is actuated immediately after the introduction of the word "WAY" by means of the alphabetical keys 3, the code information indicating "→" is entered. Therefore, in this instance, the register circuit Y develops the code information representing "→". As Y = C→ is determined in step n_{33}, the program leads to step n_{36}. 0 → CO caused in step n_{36} is to allow the register circuit CO to be reset with the object of being ready for the following retrieval operations as a series of the retrieval operations are completed. The program leads to steps $n_{37} \rightarrow n_{38} \rightarrow n_{39} \rightarrow n_{37}$ where the translated words stored are transferred to the register circuit Y.

That is, before that time, the register circuit Y keeps the code information of "WAY→" which is indicated in the indicator DSP. Then the translated words

"ﾝ・ﾐﾁ ... ﾎﾗﾎﾗ"

in connection with the English word "WAY" are entered into the register circuit Y in addition to the entered word "WAY→", so that the indicator DSP displays the translated words together with the entered English word as shown in FIG. 2(B).

Until the ROM 02 develops the boundary code BC, the output signals from the ROM 02 are introduced into the register circuit Y as caused in step n_{38}. Each time the output signals from the ROM 02 are admitted into the register circuit Y, the following address of the ROM 02 is selected. When 02 = BC is established all the retrieval procedures are completed to thereby return back to step n_1.

Under the circumstances that 02 = C is executed in step n_{34}, step n_{44} and the following steps are conducted as follows. Suppose that it is desired that another specific word "WRIGHT" is subjected to the retrieval procedure and then provided that a further different word, say, "WE", having at least one common character, say, "WE", to the specific word "WEIGHT" is stored before the specific word "WEIGHT", the following steps starting from step n_{44} are available. The common characters "WE" are at the upper position of the words and the further different word "WE" has few characters than the specific word "WEIGHT".

In such a case, Y = C→ is not established in step n_{33} and 02 = C→ is determined in step n_{34}. As the specific word "WEIGHT" is not consistent with the further different word "WE", the program reaches step n_{44} wherein steps $n_{44} \rightarrow n_{45} \rightarrow n_{44}$ are conducted to skip the word "WE".

As described above, the entered English word is displayed in the indicator DSP.

[Electronic Calculator Mode]

The mode selection switch 4 is switched to the electronic calculator mode to thereby make the switch MD shown in FIG. 3 turn off. Before the time, the program leads to steps $n_1 \rightarrow n_{48} \rightarrow n_{49} \rightarrow n_1$. When the switch MD is turned off (MD = 0) to thereby cause steps $n_1 \rightarrow n_{48} \rightarrow n_{54} \rightarrow n_{55}$.

Immediately before the preceding electronic dictionary mode is selected, the contents stored in the register circuit YU for the purpose of memory are transmitted to the register circuit Z in step n_{50}. In step n_{55}, Z→YU is executed. In step n_{51}, the calculation results and the entered numeral information stored in the register circuit YD are sent to the register circuit V. The contents of the register circuit V are return back to the register circuit YD in step n_{56}. Thus the indicator DSP is adapted to show the numeral information with the aim of utilizing it for the electronic calculator mode purposes.

Thereafter, the numeral and function keys 3′ are actuated as the conventional electronic calculator. FIG. 5 shows operations used for the electronic calculator mode. An actuation of the numeral keys 3 enables steps $n_1 \rightarrow n_2 \rightarrow$ ml to be executed. Steps m_1 to m_3 are conducted to determine the kind of the numeral keys actuated. In the following step L1, the entered degit is read in the control circuit. The register circuit YD has the degit entered. When the calculation is terminated or one of the numeral keys 3 is actuated immediately after the actuation of functional keys, the contents preliminarily stored in the

register circuit YD are transferred to the register circuit V and in addition fresh numeral information is entered in the lowest degit of the register circuit YD. Upon the subsequent introduction by the numeral key actuation, the corresponding numeral information is successively, introduced into the register circuit YD.

Thus number to be calculated is entered into the register circuit V while number to cause calculation is admitted to the register circuit YD, both with the aim of being ready for the subsequent calculation. When one of the function keys such as a multiplication key is actuated, the program leads to steps $n_1 \rightarrow n_2 \rightarrow m_1 \rightarrow m_2 \rightarrow m_3 \rightarrow m_4 \rightarrow L2$. Step L2 is executed to memory the kind of the function defined by the one of the function keys, say, multiplication.

Step L2 is performed to cause other function operations such as clear, clear entry, memory clear, or other calculation operations as is well-known.

Upon the actuation of an equal key to obtain the calculation results, the program further leads to $\rightarrow m_5 \rightarrow L3$ to thereby cause a defined calculation.

To cause four rules, the register circuits V and YD are utilized together with other register circuits although not shown in FIG. 5. The calculation results are entered into the register circuit YD so that the display DSPD indicates them. To conduct memory calculation, the register circuits YI and YD are utilized and, if necessary, the other register circuits are available although not shown in FIG. 5. The register circuit YU contains the calculation results, wherein the display DSPU indicates the calculation results.

As described above, the two register circuits YU and YD are effectively available in the electronic calculator mode.

Some of features of the present invention are summarized as follows:

1. A part of speech or other relevant information is provided in conjunction with its translated word corresponding to a specific word entered by means of a keyboard. All of the part of speech, the other relevant information, and the translated word are stored in a memory means. A word equivalent to the specific word entered can be stored in the memory means together with them. It is unnecessary for the word equal to the specific word to be stored in the memory means as far as the specific word entered can be identified.

2. If there are present two or more translated words stored in the memory means, they are developed together with their parts of speech or the other relevant information. In such a case, it is possible that their parts of speech are different.

3. A device of the present invention acts as an electronic dictionary and language interpreter in addition to an electronic calculator. In such a case, an indicator is responsive to the two mode by switching.

4. If there is information used in the first electronic calculator mode, the information is transferred into a memory upon the selection of the electronic dictionary mode. The information is return back to a circuit element used to conduct the second electronic calculator mode in response to the switch to the second electronic calculator mode. The information is transferred to an indicator for displaying purposes immediately after the switch to the second electronic calculator mode.

5. In conducting retrieval procedures in the electronic dictionary mode, if there is present one or more addresses contained within a memory in which one or more characters where already consistent with one or more characters entered by the keyboard actuation, the consistent one or more addresses are skipped with the help of control of an address counter as caused in step n_{46}. An aim of thus skipped retrieval procedures is to shorten a retrieval period of time for the following address.

6. An indicator is provided so that one or more translated words in addition to an entered word are displayed in the electronic dictionary mode. The indicator is structured as a two-storied display wherein the one or more translated words and the entered word are indicated widely from the upper portion to the lower portion in the two-storied display in the electronic dictionary mode. In the electronic calculator mode, the two-storied display is available such that the upper portion is used to indicate the contents of a memory and the lower portion is used to indicate numeral and/or function information entered by the keyboard actuation and to indicate calculation results, and vice versa.

7. A simple keyboard is available as a keyboard used in connection with an electronic calculator mode and a different keyboard utilized in connection with an electronic dictionary mode. The simple keyboard is switched so as to be adopted to one of the two different types of a keyboard, according to switch of a mode selection switch.

8. A clear key and a clear entry key are utilized in both the electronic calculator mode and the electronic dictionary mode to cause canceletion of entered information wholly or partially, respectively.

9. The memory means for containing a great deal of word information comprises a read only memory (ROM).

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications are intended to be included within the scope of the following claims.

CLAIMS

1. A word information storage device comprising:

memory means containing a great deal of first character information in a first language which designates a translated word;

said memory means further containing second character information specifying and indexing said first character information, where said second character information is stored having a relationship with said first character information;

means for addressing said memory means to search a piece of said first character information and said second character information;

means responsive to said addressing means for indicating the piece of the said first character information and said second character information.

2. The device according to claim 1, wherein said second character information represents a special character for characterizing the translated word defined by said first character information.

3. The device according to claim 2, wherein said special character comprises a part of speech of said translated word.

4. The device according to claim 2, wherein said special character comprises an additional character used for aiding to recognize the nature of said translated word.

5. The device according to claim 1, wherein said memory means contains a plurality of combinations of said first character information and said second character information, said addressing means is adapted to address said memory means so as to search the plurality of combinations of said first character information and said second character information, and said indicating means is adapted to indicate the plurality of combinations of said first character information and said second character information.

6. A combination of a word information storage device and an electronic calculator comprising:

memory means containing a great deal of first character information which designates a translated word;

said memory means further containing second character information specifying and indexing said first character information, where said second character information is stored having a relationship with said first character information;

means for addressing said memory means to search a piece of said first character information and said second character information in an electronic word information searching mode;

storage means responsive to said addressing means for storing the piece of said first character information and said second character information;

said storage means further responsive to an input means which is activated to enter information used for an electronic calculator mode so that said storage means causes calculation in said electronic calculator mode to obtain calculation results; and

means responsive to said storage means for indicating said calculation results obtained in said electronic calculator mode and said piece of said first character information and said second character information in said electronic word information searching mode.

7. The combination according to claim 6, wherein said storage means further responsive to a second input means which is activated to enter information specifying said piece of said first character information and said second character information in said electronic word information searching mode,

comparison means for determining equivalency between said information entered by said second input means and said piece of said first character information and said second character information obtained from said memory means;

counting means responsive to said comparison means for counting the number of occurrence of the equivalency generated, and

skipping means responsive to said counting means for causing skipping operations according to counting results determined by said counting means in causing the following determination of the equivalency between said information and said piece of said first character information and said second character information.

8. The combination according to claim 6, wherein such memory means stores a great number of words in such a manner that leading characters are stored in respective leading addresses of all the addresses contained in said memory means,

said storage means is adapted to call back the respective leading addresses at the first time in response to said second input means, and

comparison means responsive to said storage means for determining equivalency between the first information of said information entered by said second input means and said respective leading characters stored in said respective leading addresses.

9. The combination according to claim 6, wherein said indicating means further comprises:

means for receiving and storing calculator information used in connection with the first electronic calculator mode upon selection of the first word information searching mode, and

recovering means responsive to selection of the second electronic calculator mode for recovering said calculator information to said storage means so that said indicating means displays said calculator information.

10. A combination of a word information storage device and an electronic calculator comprising:

memory means containing a great deal of first character information which designates a

translated word;

said memory means further containing second character information specifying and indexing said first character information, where said second character information is stored having a relationship with said first character information;

means for addressing said memory means to search a piece of said first character information and said second character information in an electronic word information searching mode;

register means provided for causing the electronic word information searching mode having a relationship with said addressing means;

said register means further activated for causing an electronic calculator mode; and

means responsive to said addressing means and said register means for indicating the piece of said first character information and said second character information and for indicating calculation results obtained in the electronic calculator mode.

11. A word information storage device comprising:

a memory storing information representative of words of a first language, and, for each word, further information representative of a characteristic of that word;

address means operable to address the memory so as to locate information representing a word and its characteristic; and

means responsive to the located information for indicating said word and characteristic.

12. A device as claimed in claim 11, including input means for entering a word in a second language, said address means being responsive to the input means for locating information representing the translation, into said first language, of said entered word.

13. A combination of a word information storage device and an electronic calculator, substantially as herein described with reference to the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1980. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.