



- (51) International Patent Classification:
H03K 17/22 (2006.01) *H03K 17/14* (2006.01)
- (21) International Application Number:
PCT/EP2020/053601
- (22) International Filing Date:
12 February 2020 (12.02.2020)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
62/804,267 12 February 2019 (12.02.2019) US
62/856,982 04 June 2019 (04.06.2019) US
- (71) Applicant: **AMS INTERNATIONAL AG** [CH/CH];
Eichwiesstrasse 18b, 8645 Jona (CH).
- (72) Inventors: **BONELLI, Andrea**; Viale dei Castagni 18,
06100 Perugia (IT). **CHICCA, Stefania**; Via argine vec-
chio 108, 56019 Vecchiano (IT).
- (74) Agent: **BRYER, Pamela** et al.; MARKS & CLERK LLP,
62-68 Hills Road, Cambridge CB2 1LA (GB).
- (81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: THRESHOLD DETECTOR OF A POWER ON RESET CIRCUIT WITH IMPROVED ACCURACY FOR SWITCHING LEVELS OVER TEMPERATURE VARIATIONS

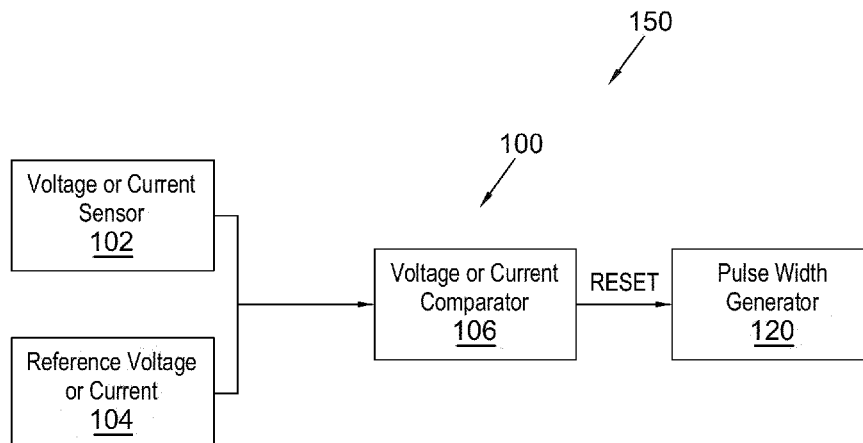


Fig. 1

(57) Abstract: A power on reset circuit includes a threshold detector circuit. The threshold detector circuit includes a power supply voltage, a voltage comparator, first circuitry, second circuitry, and third circuitry. The voltage comparator has first and second input terminals, and an output terminal to provide a reset signal. The first circuitry is operable to convert the power supply voltage to a sensed current, and provides a positive temperature coefficient to the sensed current. The second circuitry is operable to generate, based on the sensed current, a temperature-dependent voltage corresponding to the power supply voltage and to couple the temperature-dependent voltage to the first input of the voltage comparator. The third circuitry is operable to generate, based on the sensed current, a reference voltage and to couple the reference voltage to the second input of the voltage comparator.

(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

THRESHOLD DETECTOR OF A POWER ON RESET CIRCUIT WITH IMPROVED ACCURACY FOR SWITCHING LEVELS OVER TEMPERATURE VARIATIONS

TECHNICAL FIELD

[0001] The disclosure relates to Power On Reset circuits.

BACKGROUND

[0002] A Power On Reset (POR) circuit is present in many electronic devices and more specifically on monolithic integrated circuits (ICs). The POR functions to initialize one or more components of a device to a known state when in the presence of a rising event of the power supply voltage of the device. It does so by asserting its output RESET signal when the supply voltage is below a certain threshold such that the components can be held in a reset state that is a known initial state. The output RESET signal should de-assert when the supply voltage rises above the level for a predictable and stable behavior near the normal operating voltage range of the device.

SUMMARY

[0003] The present disclosure describes POR circuits for selectively initializing one or more components of an electronic device (e.g., a monolithic integrated circuit) to a known state based on a measured power supply voltage of the device. Implementations of the described POR circuit can be used to provide high accuracy of the switching levels without the need for complex circuits such as bandgap voltage or current reference circuits, which tend to be greater in area and have higher quiescent current. As an example, this enables POR circuits to be implemented in a smaller area on a chip (e.g., compared to some other POR circuits).

[0004] In an aspect, the present disclosure describes a power on reset circuit that includes a threshold detector circuit. The threshold detector circuit includes a power supply voltage, a voltage comparator, first circuitry, second circuitry, and third circuitry. The voltage comparator has first and second input terminals, and an output terminal to provide a reset signal. The first circuitry is operable to convert the power supply voltage to a sensed

current, and provides a positive temperature coefficient to the sensed current. The second circuitry is operable to generate, based on the sensed current, a temperature-dependent voltage corresponding to the power supply voltage and to couple the temperature-dependent voltage to the first input of the voltage comparator. The third circuitry is operable to generate, based on the sensed current, a reference voltage and to couple the reference voltage to the second input of the voltage comparator.

[0005] Implementations of this aspect can include one or more of the follow features.

[0006] Some implementations, the first circuitry includes a transistor having a base-emitter voltage that decreases with increasing temperature.

[0007] Some implementations, the first circuitry further includes a resistance network coupled to the transistor. The resistance network includes a resistive element in series with the transistor and a resistive element in parallel with the transistor.

[0008] Some implementations, the resistive element in series with the transistor includes a first resistive element and a second resistive element connected to one electrically at a node. The resistive element in parallel with the transistor is connected electrically to the node.

[0009] Some implementations, each of the second and third circuitries includes a respective transistor. A base-emitter voltage of the transistor in the second circuitry is more sensitive to temperature than is a base-emitter voltage of the transistor in the third circuitry.

[0010] Some implementations, the transistor in the second circuitry has a larger emitter area than the transistor in the third circuitry.

[0011] Some implementations, an aspect ratio of the transistor in the second circuitry is greater than an aspect ratio of the transistor in the third circuitry.

[0012] Some implementations, a ratio of the aspect ratio of the transistor in the second circuitry to the aspect ratio of the transistor in the third circuitry is 10.

[0013] Some implementations, the voltage comparator is operable to provide, as the reset signal, a first signal having a first voltage value when the temperature-dependent voltage coupled to the first input of the voltage comparator is greater than the reference voltage coupled to the second input of the voltage comparator. Further, the voltage

comparator is operable to provide, as the reset signal, a second signal having a second voltage value when the temperature-dependent voltage coupled to the first input of the voltage comparator is less than the reference voltage coupled to the second input of the voltage comparator. The first voltage value is less than the second voltage value.

[0014] Some implementations, the first voltage value corresponds to a digital 0, and the second voltage value corresponds to a digital 1.

[0015] Some implementations, the power on reset circuit includes a pulse width generator. The pulse width generator is operable to receive the reset signal and generate a control signal for initializing one or more components of an electronic device based on the reset signal.

[0016] Some implementations, the electronic device is a monolithic integrated circuit.

[0017] Some implementations, the monolithic integrated circuit is part of the monolithic integrated circuit.

[0018] The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features and advantages will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 is a functional block diagram of an example threshold detector of a POR circuit.

[0020] FIG. 2 is a diagram of an example threshold detector of a POR circuit.

[0021] FIG. 3 is a diagram of another example threshold detector of a POR circuit.

DETAILED DESCRIPTION

[0022] In general, a POR circuit is partitioned into two functional stages: a threshold detector and a pulse width generator. The threshold detector is operable to detect when the supply voltage is above or below a certain supply voltage level for the device to

operate and in response, generate a reset signal to trigger the operation of the pulse width generator. The pulse width generator is operable, when triggered, to generate a control signal for initiating one or more components of the electronic device (e.g., a control signal having a pulse with a duration that is long enough to cause the components coupled to the POR circuit to initialize). The present description focuses on the threshold detector circuit.

[0023] FIG. 1 is a functional block diagram of an example threshold detector 100 of a POR circuit 150. The threshold detector 100 includes a supply voltage sensor 102, a reference voltage or current 104, and a voltage or current comparator 106.

[0024] In an example operation of the threshold detector 100, the supply voltage 102 measures a power supply voltage (e.g., the voltage of an electrical signal providing power to an electronic device, such as a monolithic integrated circuit), and provides an indication of the measured voltage to the voltage or current comparator 106. The voltage or current comparator 106 compares the measured voltage to the reference voltage or current 104, and selectively generates a RESET signal based on a comparison. The RESET signal is provided to a pulse width generator 150, which generates a control signal to initialize one or more components of the electronic device components to a known state (e.g., to “reset” the components to a known state due to changes in the supply voltage, such as when the supply voltage is above or below a certain supply voltage required for the device to operate properly).

[0025] An important function of the POR circuit is to reset the components (e.g., generate a RESET signal to control the operation of the pulse width generator 120) in the presence of a falling event of the device's voltage supply to disable some or all functionality of the device when the voltage is too low for predictable behavior. In some cases, the switching levels for rising and falling supply voltages do not overlap, but the rising switching levels can be higher than the falling switching levels. For example, the POR can generate a RESET signal when the supply voltage exceeds a threshold voltage $V_{threshold,high}$, and generate a RESET signal when the supply voltage decreases below a threshold voltage $V_{threshold,low}$, where $V_{threshold,high}$ is greater than $V_{threshold,low}$.

[0026] The operation of a POR circuit is constrained by area and quiescent current. As this circuit generally operates only during power up and power down, the physical area

(e.g., the area of a chip) that can be dedicated to this functionality is relatively small compared to the area allotted for implementing other functionality of the device. Further, in embodiments where ICs are operating from a battery, it is important that the quiescent current be of the same order of magnitude as the total leakage current of a device, for example less than 1 μA .

[0027] A problem to address when designing POR circuit for monolithic IC is the variation of the switching levels in presence of process and temperature variations. In many implementations, these circuits show high inaccuracy due to the drift of various device parameters such as the threshold voltage V_{th} of metal-oxide-semiconductor (MOS) transistors, the base-emitter voltage V_{be} of bipolar transistors, and the parameter β and the output resistance of MOS transistors. This inaccuracy is particularly important when operating at a low voltage supply (e.g., 1.8 V or below). In the presence of a high spread of the switching level, the POR circuit may de-assert either at a supply voltage that is too low when the reset of the circuit cannot be guaranteed or when the switching level is too high (e.g., above the minimum operating voltage of the device) with the consequence that the device does not power up.

[0028] One approach to reducing the spread of the switching levels is to design POR circuits with switching levels that are a function of the ratio of device parameters so as to avoid dependency on the absolute accuracy of device parameters. This is because, in IC process technology, it is relatively easy to obtain an accurate ratio between parameters of the same type of devices, but it is relatively difficult to design for absolute values.

[0029] FIG. 2 shows an example of a threshold detector 200 of a POR circuit 250 in which a voltage comparator 202 (e.g., an operational amplifier) is used to generate a RESET signal to trigger a pulse width generator (not shown in FIG. 2) to generate a control signal for initiating one or more components of the electronic device. When the voltage at the “-” terminal of the voltage comparator 202 is greater than the voltage at the “+” terminal of the voltage comparator 202, the power supply voltage V_{DD} is sufficiently high for the device to operate, the RESET signal is thus low (e.g., a digital 0), and the device is able to operate. Conversely, when the voltage at the “-” terminal of the voltage comparator 202 is less than the voltage at the “+” terminal of the voltage comparator 202, the power supply

voltage V_{DD} is insufficiently high for the device to operate, the RESET signal is high (e.g., a digital 1), and the other device functions controlled by the POR circuit 250 are disabled (e.g., via a control signal generated by a pulse width generator).

[0030] In the illustrated POR circuit 250, a bipolar transistor Q_2 is biased from transistor M_3 to generate a relatively stable voltage reference $V_{be,2}$. A resistance R_1 , a current mirror formed of transistors M_1 and M_2 , a second resistance R_2 and a second bipolar transistor Q_1 are provided to generate a voltage proportional to the power supply voltage V_{DD} . The ratio of W_1 and W_2 of the transistors M_1 and M_2 , respectively, in the illustrated example is 2:1 ($W_1 = 2 * W_2$), and the transistors M_2 and M_3 are substantially the same as one another, where W_N is channel width and L_N is channel length of a MOS transistor M_N .

[0031] A voltage comparator 202 is operable to generate an output signal (RESET) indicative of the relative values of the reference voltage (at the "+" terminal) and the sensed voltage (at the "-" terminal). The RESET signal is indicative of whether the power supply voltage V_{DD} is sufficiently high for operation of some other device. The switching level depends on the area ratio between Q_1 and Q_2 , where the area of Q_1 is N times (e.g., 8) larger than the area of Q_2 . Q_1 can be implemented, for example, as N parallel transistors substantially the same as the transistor Q_2 . The ratio of R_1 and R_2 provides a relatively accurate switching level.

[0032] In operation, the power supply voltage V_{DD} is sensed and converted to a corresponding current (I_{sense}) in a first branch of the circuit that includes M_1 and R_1 . The sensed current is scaled (e.g., by a factor of 0.5) and mirrored, and flows substantially equally in the second and third branches of the circuit (one branch includes M_2 , R_2 and Q_1 ; the other branch includes M_3 and Q_2). Thus, in the illustrated example, a current $I_{sense}/2$ flows in each of the second and third branches of the circuit.

[0033] Because of the logarithmic dependency of V_{be} in respect to its bias current, Q_2 has a base-emitter voltage V_{be} that remains relatively constant. Thus, a voltage in the third branch that is coupled to an input of the voltage comparator 202 serves as a reference voltage.

[0034] As the voltage V_{DD} increases, the current I_{sense} increases substantially linearly, and thus the voltage across R_2 also increases substantially linearly. A voltage in

the second branch corresponds to the sensed voltage and is coupled to an input of the voltage comparator 202.

[0035] The switching level of the POR circuit 250 in FIG. 2 is reached when the voltage at the inputs of the voltage comparator 202 are equal, and can be given by the following equation:

$$V_{SWITCH} = 2 \frac{R_1}{R_2} V_T \ln(8) + V_{GS1} \quad (\text{eq. 1})$$

where V_T is KT/q , and is ~ 26 mV at 300 K.

[0036] The term V_{GS1} is relatively small and so can be neglected here. Notably, the switching level depends on the ratio of devices (R_1/R_2 and Q_1/Q_2) rather than absolute value of device parameters. Further, the switching levels have a positive temperature coefficient from the V_T factor.

[0037] Because the switching level depends on the ratio of devices (R_1/R_2 and Q_1/Q_2), a potential problem arises for devices operating at low supply voltages because the temperature coefficient can be about 2.5m V/°C, causing high variation in V_{SWITCH} , especially if the operating temperature range is wide.

[0038] The effects of this temperature drift can be compensated for by precisely controlling the temperature coefficient of the supply sensing current. As an example, FIG. 3 shows a modified circuit 300 that compensates for the temperature drift of the switching levels of the type of POR circuit of FIG. 2 and preserves the setting of the switching levels from device parameters ratio rather than absolute accuracy.

[0039] As shown in FIG. 3, the modified circuit 300 resolves the drift over temperature by adding a positive temperature coefficient to the sensed current I_{sense} . In the circuit 300 of FIG. 3, the resistance R_1 of FIG. 2 is replaced with a network of resistances R_3 , R_4 , R_5 and a transistor Q_3 . In some embodiments, the resistance R_5 may be the base resistance in parallel with the $1/g_m$ of the bipolar transistor Q_3 .

[0040] The circuit 300 of FIG. 3 is operable to generate a sense current I_{sense} that increases with increasing temperature. In particular, Q_3 has a base-emitter voltage (V_{be}) that decreases with increasing temperature (e.g., by approximately 2.5mV/°C), which pulls

down the voltage at the node connecting R_3 , R_4 , and R_5 . This, in turn, increases the voltage across R_3 , resulting in a higher sense current I_{sense} .

[0041] Also, as temperature increases, the current flowing through R_2 increases. Since Q_1 has a larger (emitter) area than Q_2 , Q_1 is more sensitive to changes in temperature. In particular, $(V_{be,Q1} - V_{be,Q2})$ has a negative temperature coefficient. Adding a positive temperature coefficient to the sensed current I_{sense} thus can help compensate for temperature drift.

[0042] The switching level of the circuit in FIG. 3 can be approximated by the following equation:

$$V_{SWITCH} = \frac{2}{R_2} V_T \ln(NQ) \frac{R_3(R_4 + R_5) + R_4 \cdot R_5}{R_4 + R_5} + V_{be,Q3} \frac{R_4}{R_4 + R_5} + V_{GS1} \quad (\text{eq. 2})$$

where NQ is the aspect ratio between Q_1 and Q_2 (e.g., 10 in the example embodiment shown in FIG. 3).

[0043] In this equation, V_T and $V_{be,Q3}$ have opposite temperature coefficients (e.g., V_T increases with increasing temperature, whereas $V_{be,Q3}$ decreases with increasing temperature). Therefore, with proper sizing of R_3 , R_4 and R_5 , it is possible to keep the switching levels approximately constant over the temperature range. For example, values for the various components can be selected such that the changes caused by V_T and $V_{be,Q3}$ tend to cancel out one another over the temperature range of interest.

[0044] The circuit 300 of FIG. 3 thus can compensate for the effect of temperature variations by the insertion of a precise temperature dependency for the supply sensing current. In particular, the circuit 300 of FIG. 3 provides a first order correction of the temperature drift of the switching levels. This feature thus can provide high accuracy of the switching levels without the need for complex circuits such as bandgap voltage or current reference circuits, which tend to be greater in area and have higher quiescent current. As an example, computer simulations indicate that the circuit 300 can provide a reduction of $4440 \mu\text{m}^2$ (e.g., a reduction of 30.4%) compared to some other circuits.

[0045] The techniques described here can be used in a wide range of monolithic ICs.

[0046] Although the example circuit 300 of FIG. 3 employs PNP bipolar transistors (e.g., transistors having a layer of N-doped semiconductor positioned between two P-doped layers), NPN transistors (e.g., transistors having a layer of P-doped semiconductor positioned between two N-doped layers) can be used in some implementations. Further, the specific relative sizes of the various transistors (e.g., Q_1 and Q_2 ; M_1 and M_2 , M_3) can vary from the examples describes above.

[0047] While this specification contains many details, these should not be construed as limitations on the scope of what may be claimed, but rather as descriptions of features specific to particular examples. Certain features that are described in this specification in the context of separate implementations can also be combined. Conversely, various features that are described in the context of a single implementation can also be implemented in multiple embodiments separately or in any suitable sub-combination.

[0048] A number of embodiments have been described. Nevertheless, various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other implementations are within the scope of the claims.

WHAT IS CLAIMED IS:

1. A power on reset circuit comprising:
 - a threshold detector circuit including:
 - a power supply voltage;
 - a voltage comparator having first and second input terminals, the voltage comparator further having an output terminal to provide a reset signal;
 - first circuitry operable to convert the power supply voltage to a sensed current, wherein the first circuitry provides a positive temperature coefficient to the sensed current;
 - second circuitry operable to generate, based on the sensed current, a temperature-dependent voltage corresponding to the power supply voltage and to couple the temperature-dependent voltage to the first input of the voltage comparator; and
 - third circuitry operable to generate, based on the sensed current, a reference voltage and to couple the reference voltage to the second input of the voltage comparator.
2. The power on reset circuit of claim 1, wherein the first circuitry includes a transistor having a base-emitter voltage that decreases with increasing temperature.
3. The power on reset circuit of claim 2, wherein the first circuitry further includes a resistance network coupled to the transistor, wherein the resistance network includes a resistive element in series with the transistor and a resistive element in parallel with the transistor.
4. The power on reset circuit of claim 3, wherein the resistive element in series with the transistor includes a first resistive element and a second resistive element connected to one electrically at a node, and wherein the resistive element in parallel with the transistor is connected electrically to the node.

5. The power on reset circuit of claim 1, wherein each of the second and third circuitries includes a respective transistor, wherein a base-emitter voltage of the transistor in the second circuitry is more sensitive to temperature than is a base-emitter voltage of the transistor in the third circuitry.

6. The power on reset circuit of claim 5 wherein the transistor in the second circuitry has a larger emitter area than the transistor in the third circuitry.

7. The power on reset circuit of claim 5, wherein an aspect ratio of the transistor in the second circuitry is greater than an aspect ratio of the transistor in the third circuitry.

8. The power on reset circuit of claim 7, where a ratio of the aspect ratio of the transistor in the second circuitry to the aspect ratio of the transistor in the third circuitry is 10.

9. The power on reset circuit of claim 1, wherein the voltage comparator is operable to:

provide, as the reset signal, a first signal having a first voltage value when the temperature-dependent voltage coupled to the first input of the voltage comparator is greater than the reference voltage coupled to the second input of the voltage comparator, and

provide, as the reset signal, a second signal having a second voltage value when the temperature-dependent voltage coupled to the first input of the voltage comparator is less than the reference voltage coupled to the second input of the voltage comparator,

wherein the first voltage value is less than the second voltage value.

10. The power on reset circuit of claim 9, wherein the first voltage value corresponds to a digital 0, and wherein the second voltage value corresponds to a digital 1.

11. The power on reset circuit of claim 1, further comprising a pulse width generator, wherein the pulse width generator is operable to receive the reset signal and generate a control signal for initializing one or more components of an electronic device based on the reset signal.

12. The power on reset circuit of claim 11, wherein the electronic device is a monolithic integrated circuit.

13. The power on reset circuit of claim 12, wherein the power on reset circuit is part of the monolithic integrated circuit.

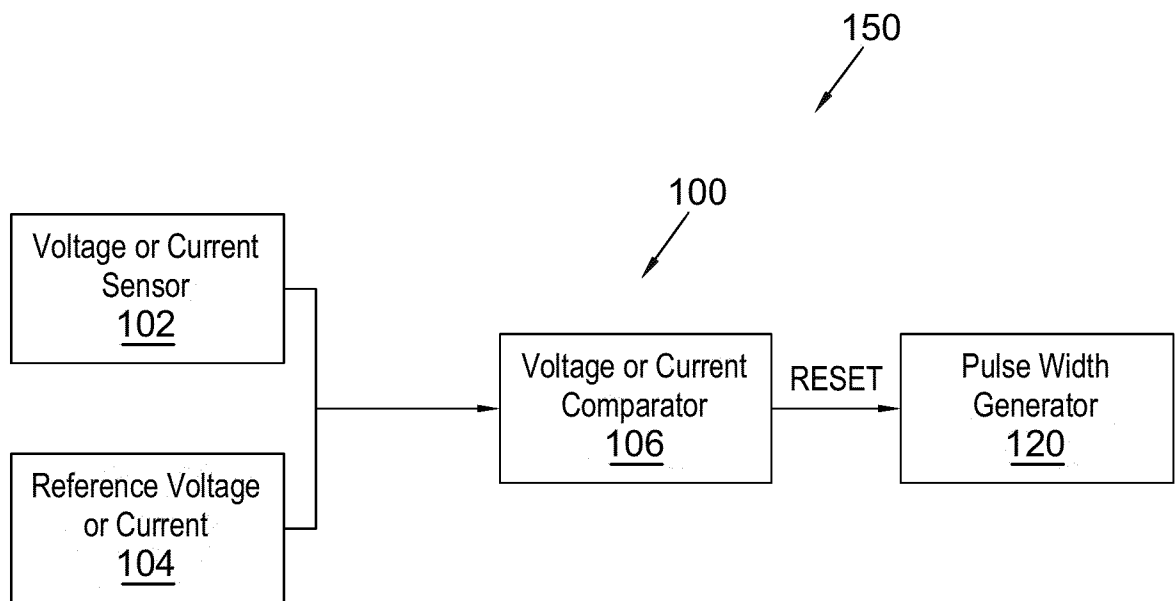


Fig. 1

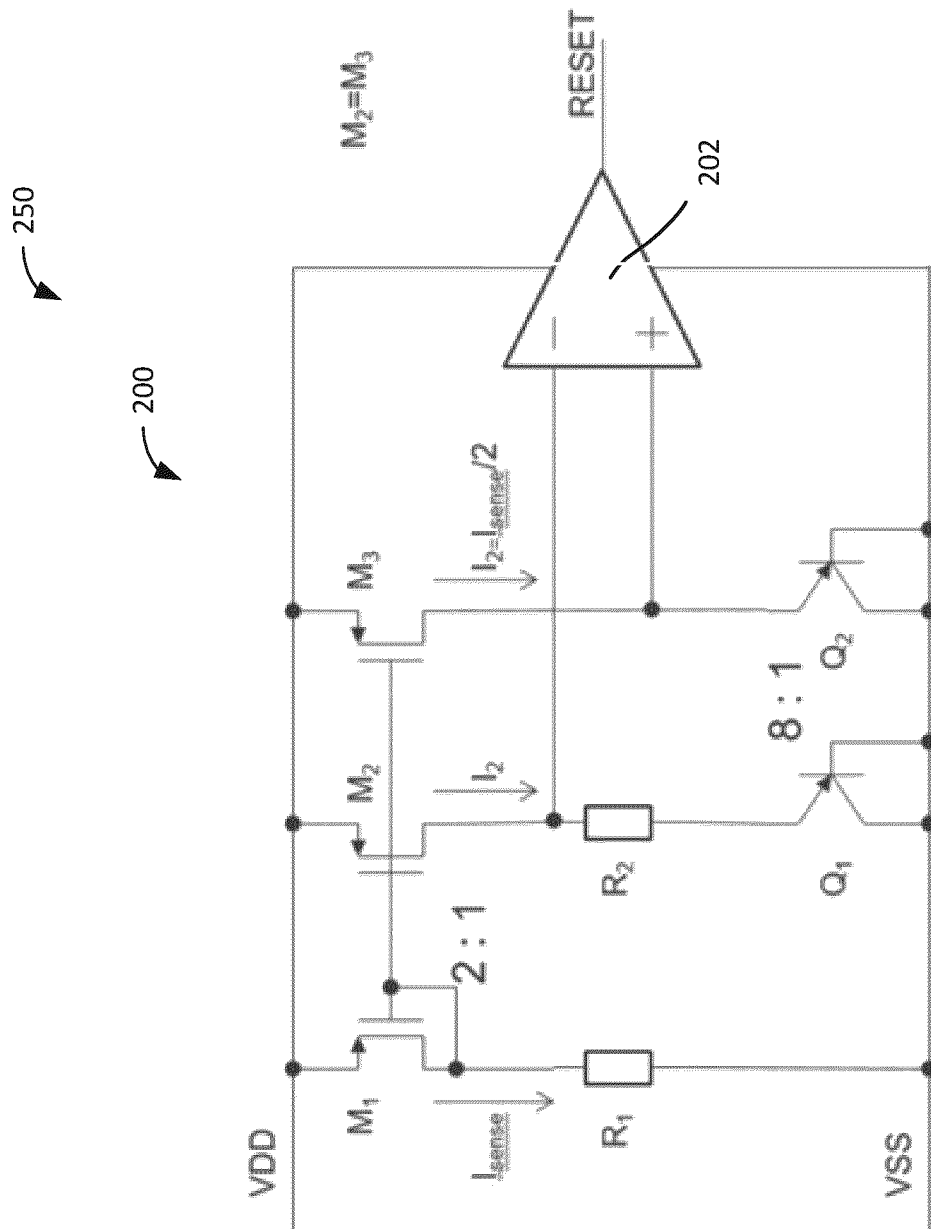


FIG. 2

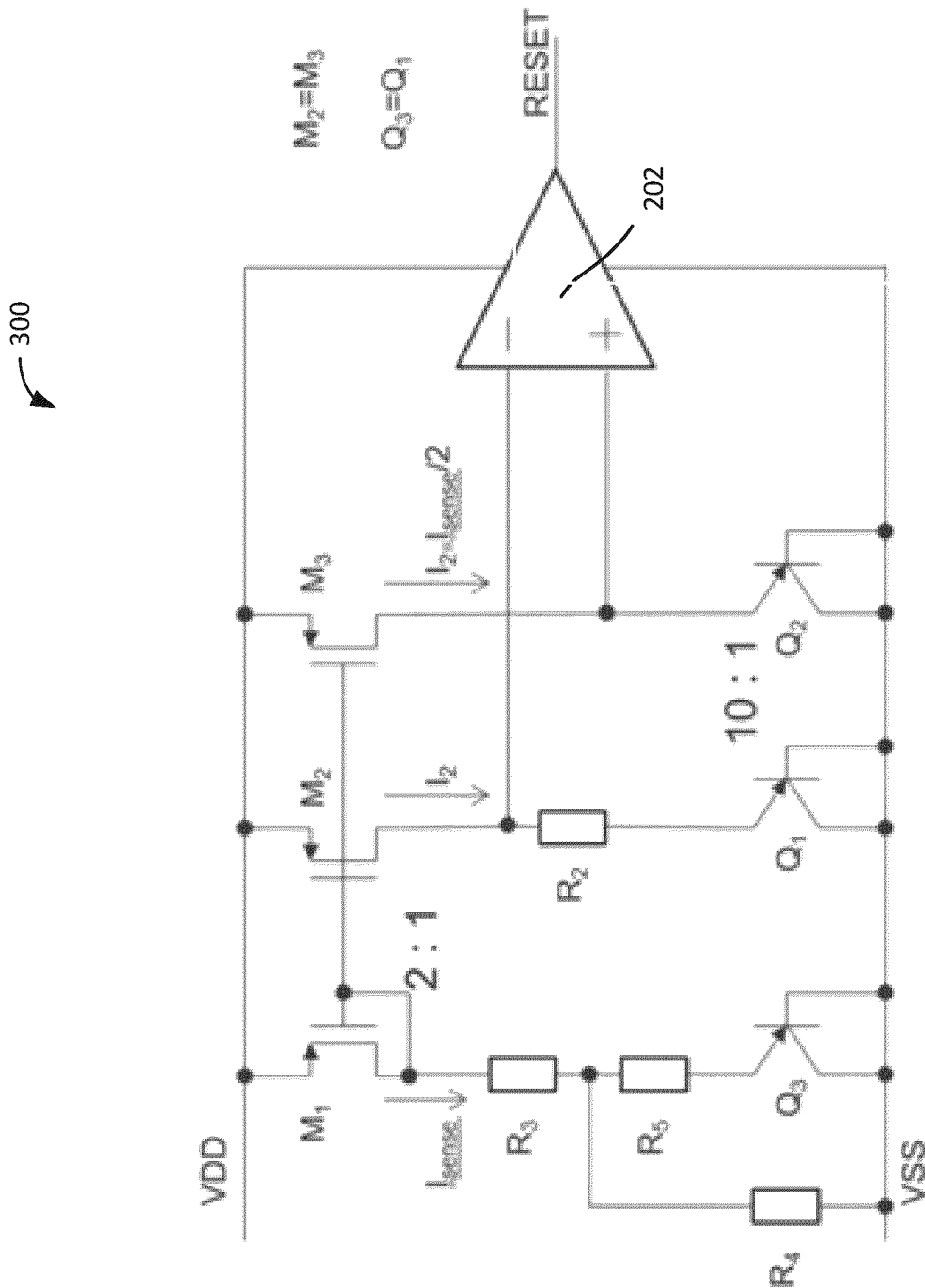


Fig. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/053601

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/22 H03K17/14
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 437 614 B1 (CHEN LIN-CHIEN [TW]) 20 August 2002 (2002-08-20)	1,2,9-13
A	column 2, line 63 - line 67; figure 2 column 3, line 1 - line 41	3-8
A	----- JP H08 186484 A (NIPPON ELECTRIC IC MICROCOMPUT) 16 July 1996 (1996-07-16) figure 4	1-13
A	----- EP 0 575 687 A1 (SGS THOMSON MICROELECTRONICS [IT]) 29 December 1993 (1993-12-29) column 1, line 1 - line 19; figure 2	1-13
A	----- US 2002/011882 A1 (OZEKI YOSHITOMO [JP] ET AL) 31 January 2002 (2002-01-31) paragraph [0025]; figure 6	1-13
	----- -/-	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 April 2020

Date of mailing of the international search report

30/04/2020

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

O'Reilly, Siobhan

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/053601

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 492 848 B1 (LEE DO-YOUNG [KR]) 10 December 2002 (2002-12-10) column 4, line 27 - line 67; figures 4,5 column 5, line 1 - line 20 column 3, line 60 - line 64 -----	1-13
A	US 2004/189356 A1 (WADA MASAHARU [JP]) 30 September 2004 (2004-09-30) figures 2, 3,10 -----	1-13
A	CN 107 707 232 A (SHANGHAI BELLING CO LTD) 16 February 2018 (2018-02-16) paragraph [0030]; figure 2 -----	1-13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2020/053601

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6437614	B1	20-08-2002	NONE
JP H08186484	A	16-07-1996	JP 3071654 B2 31-07-2000 JP H08186484 A 16-07-1996
EP 0575687	A1	29-12-1993	DE 69217209 D1 13-03-1997 DE 69217209 T2 15-05-1997 EP 0575687 A1 29-12-1993 JP H0690154 A 29-03-1994 US 5528184 A 18-06-1996
US 2002011882	A1	31-01-2002	JP 2001077681 A 23-03-2001 US 2002011882 A1 31-01-2002
US 6492848	B1	10-12-2002	JP 4694674 B2 08-06-2011 JP 2001044814 A 16-02-2001 KR 20010005079 A 15-01-2001 US 6492848 B1 10-12-2002
US 2004189356	A1	30-09-2004	JP 2004304632 A 28-10-2004 US 2004189356 A1 30-09-2004
CN 107707232	A	16-02-2018	NONE

2/3

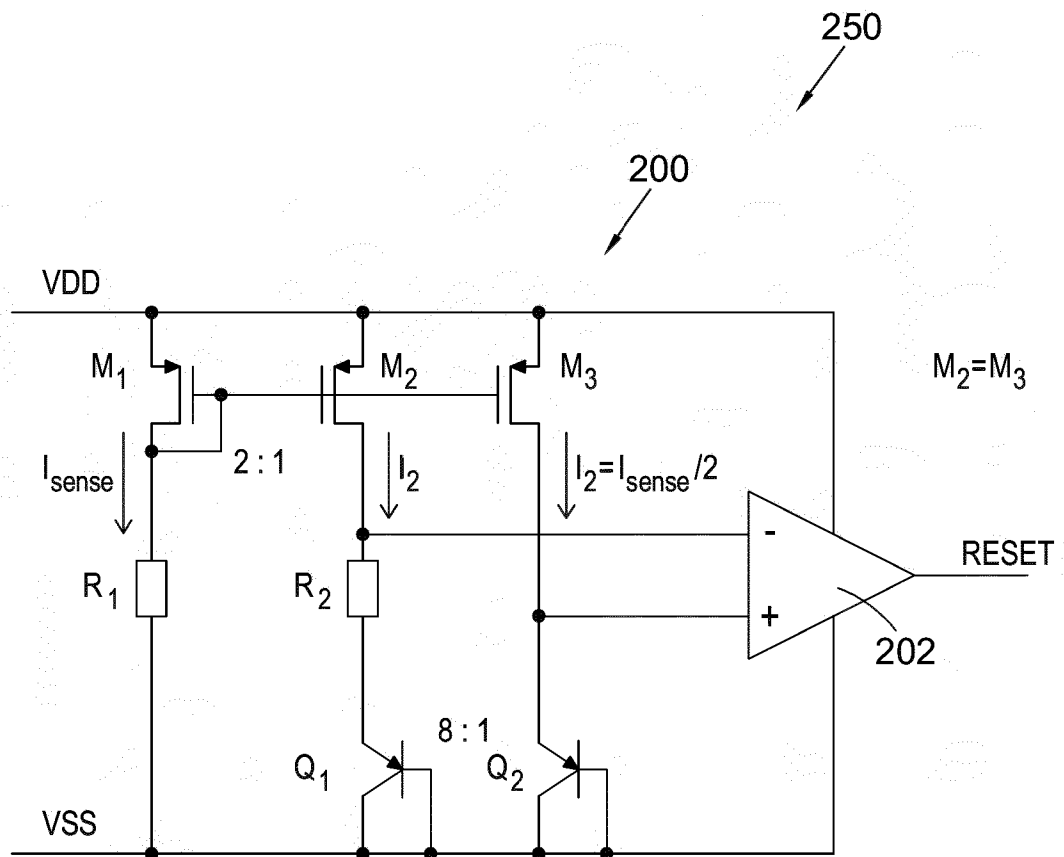


Fig. 2

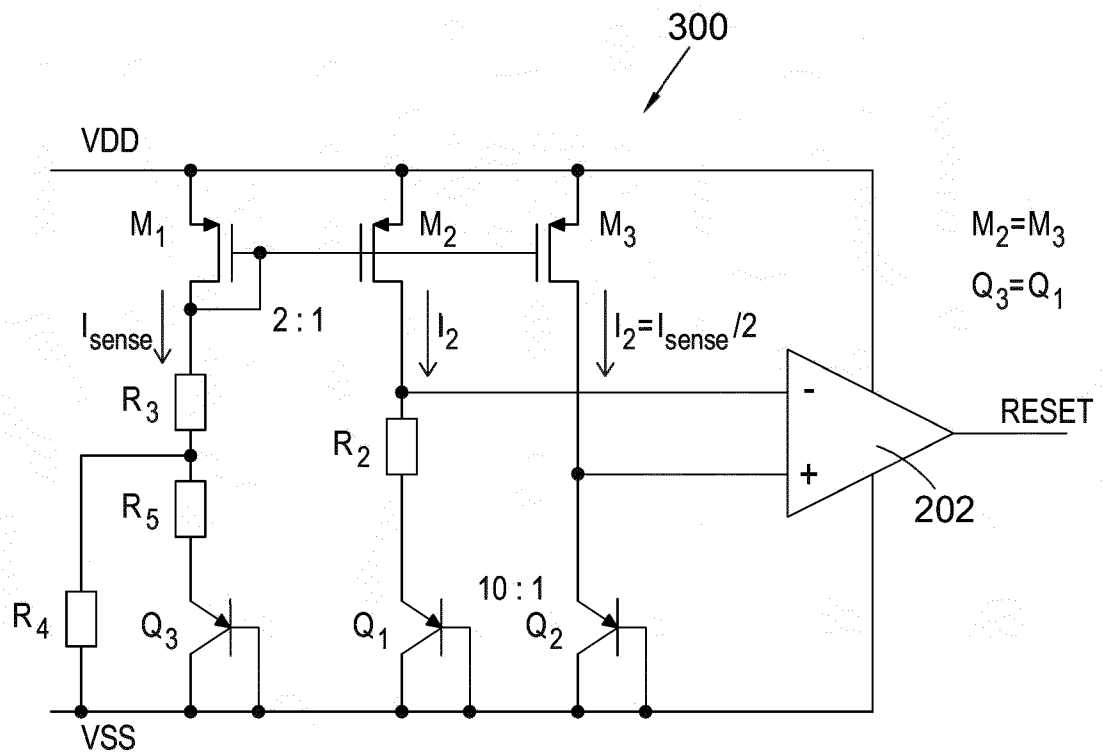


Fig. 3