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(71) Demandeur/Applicant:
BUTTERFLY NETWORK, INC., US

(72) Inventeurs/Inventors:
CHEN, KAILIANG, US;
FIFE, KEITH G., US;
SANCHEZ, NEVADA J., US;
CASPER, ANDREW J., US;
RALSTON, TYLER S., US

(74) Agent: SMART & BIGGAR

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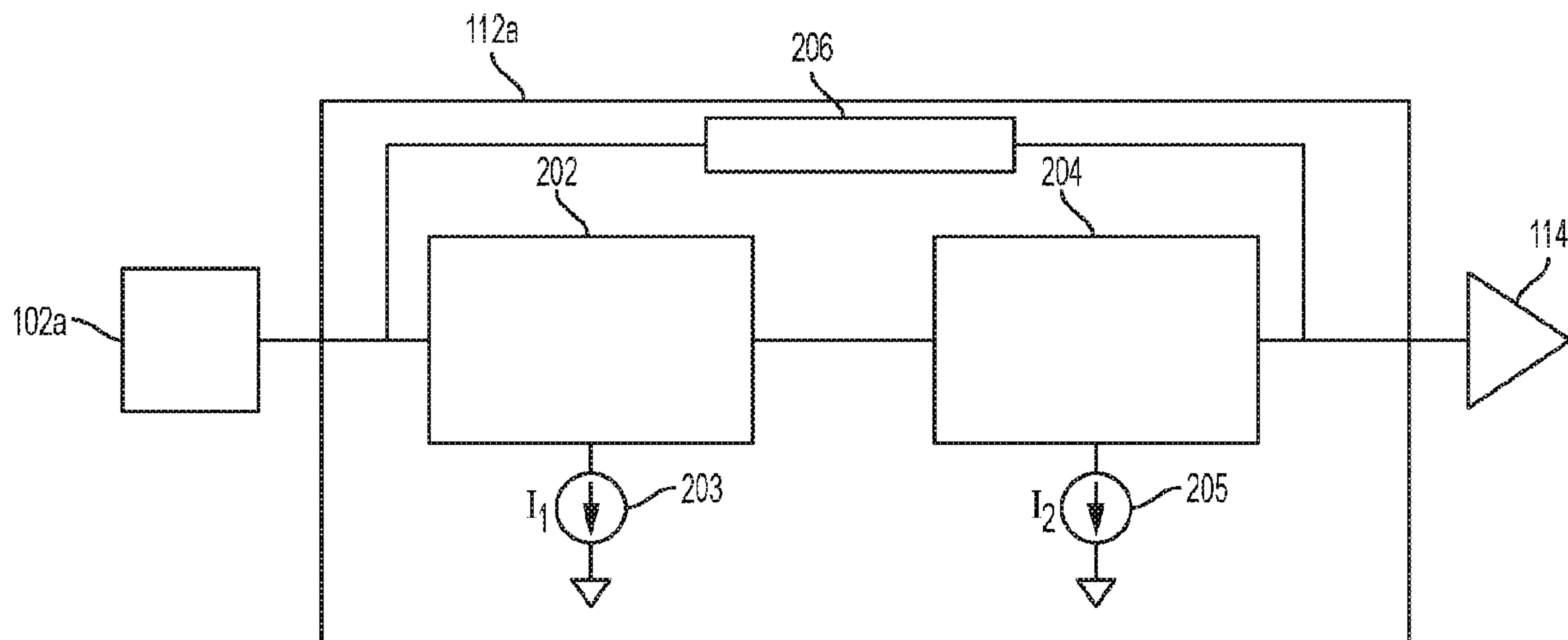


FIG. 2

(57) Abrégé/Abstract:

A variable current trans-impedance amplifier (TIA) for an ultrasound device is described. The TIA may be coupled to an ultrasonic transducer to amplify an output signal of the ultrasonic transducer representing an ultrasound signal received by the ultrasonic transducer. During acquisition of the ultrasound signal by the ultrasonic transducer, one or more current sources in the TIA may be varied.

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(71) Applicant: BUTTERFLY NETWORK, INC. [US/US];
530 Old Whitfield Street, Guilford, CT 06437 (US).

(72) Inventors: CHEN, Kailiang; 7 River Colony, Guilford, CT 06437 (US). FIFE, Keith, G.; 635 Matadero Avenue, Palo Alto, CA 94306 (US). SANCHEZ, Nevada, J.; 1280 Little Meadow Road, Guilford, CT 06437 (US). CASPER, Andrew, J.; 161 East Main Street, Unit 205, Clinton, CT 06413 (US). RALSTON, Tyler, S.; 56 Beach Park Road, Clinton, CT 06413 (US).

(74) Agent: FRANKLIN, Thomas, A.; Wolf, Greenfield & Sacks, P.C., 600 Atlantic Avenue, Boston, MA 02210-2206 (US).

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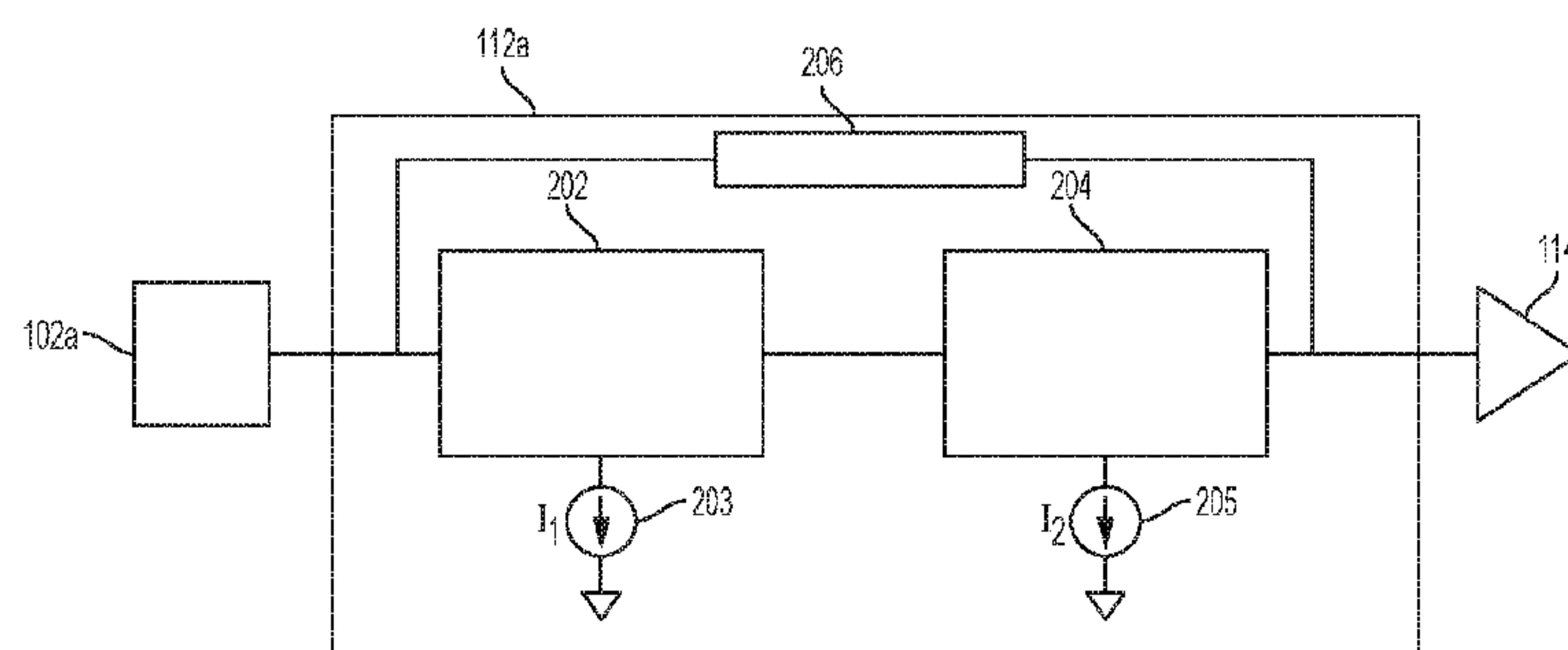


FIG. 2

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(57) Abstract: A variable current trans-impedance amplifier (TIA) for an ultrasound device is described. The TIA may be coupled to an ultrasonic transducer to amplify an output signal of the ultrasonic transducer representing an ultrasound signal received by the ultrasonic transducer. During acquisition of the ultrasound signal by the ultrasonic transducer, one or more current sources in the TIA may be varied.

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TRANS-IMPEDANCE AMPLIFIER FOR ULTRASOUND DEVICE AND RELATED APPARATUS AND METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation claiming the benefit under 35 U.S.C. §120 of U.S. Patent Application Serial No. 14/957,395 filed December 2, 2015 under Attorney Docket No. B1348.70023US00 and entitled “TRANS-IMPEDANCE AMPLIFIER FOR ULTRASOUND DEVICE AND RELATED APPARATUS AND METHODS,” which is hereby incorporated herein by reference in its entirety.

BACKGROUND

Field

[0002] The present application relates to ultrasound devices having an amplifier for amplifying received ultrasound signals.

Related Art

[0003] Ultrasound probes often include one or more ultrasound sensors which sense ultrasound signals and produce corresponding electrical signals. The electrical signals are processed in the analog or digital domain. Sometimes, ultrasound images are generated from the processed electrical signals.

BRIEF SUMMARY

[0004] According to an aspect of the present application, an ultrasound apparatus is provided, comprising an ultrasound sensor and a variable current trans-impedance amplifier (TIA). The variable current TIA is coupled to the ultrasound sensor and configured to receive and amplify an output signal from the ultrasound sensor. The variable current TIA has a variable current source.

[0005] According to an aspect of the present application, a method is provided, comprising acquiring an ultrasound signal with an ultrasound sensor during an acquisition period and outputting, from the ultrasound sensor, an analog electrical signal representing the

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ultrasound signal. The method further comprises amplifying the electrical signal with a variable current trans-impedance amplifier (TIA), including varying a current of the variable current TIA during the acquisition period.

[0006] According to an aspect of the present application, a method is provided, comprising acquiring an ultrasound signal with an ultrasound sensor during an acquisition period and outputting, from the ultrasound sensor, an analog electrical signal representing the ultrasound signal. The method further comprises amplifying the electrical signal with a variable current trans-impedance amplifier (TIA), including decreasing a noise floor of the variable current TIA during the acquisition period.

BRIEF DESCRIPTION OF DRAWINGS

[0007] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0008] FIG. 1 is a block diagram of an ultrasound device including an amplifier for amplifying an ultrasound signal, according to a non-limiting embodiment of the present application.

[0009] FIG. 2 illustrates the amplifier of FIG. 1 in greater detail, coupled to the ultrasonic transducer and averaging circuit of FIG. 1, according to a non-limiting embodiment of the present application.

[0010] FIG. 3A is a circuit diagram illustrating an implementation of the amplifier of FIG. 2, according to a non-limiting embodiment of the present application.

[0011] FIG. 3B is a circuit diagram of an implementation of one variable impedance circuit of FIG. 3A, according to a non-limiting embodiment of the present application.

[0012] FIG. 3C is a circuit diagram of an implementation of another variable impedance circuit of FIG. 3A, according to a non-limiting embodiment of the present application

[0013] FIG. 4 is a graph illustrating the behavior of two variable current sources of an amplifier during an acquisition period, as may be implemented by the amplifier of FIGs. 2 and 3A, according to a non-limiting embodiment of the present application.

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[0014] FIG. 5 is a graph illustrating an electrical signal representing an ultrasound signal, and a noise floor of an amplifier during an acquisition period, according to a non-limiting embodiment of the present application.

DETAILED DESCRIPTION

[0015] Aspects of the present application relate to amplification circuitry for an ultrasound device. An ultrasound device may include one or more ultrasonic transducers configured to receive ultrasound signals and produce electrical output signals. Thus, the ultrasonic transducers may be operated as ultrasound sensors. The ultrasound device may include one or more amplifiers for amplifying the electrical output signals. The power consumed by, the noise generated by, and the linear signal amplification quality provided by, the amplifier may depend on an amount of current consumed by the amplifier. In some embodiments, the amplifier has a variable current source. The variable current source is adjusted during acquisition of an ultrasound signal to maintain the noise level of the amplifier below the signal level and to maintain linear amplification, while at the same time reducing the amount of power consumed by the amplifier. In some embodiments, the amplifier is a TIA.

[0016] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0017] FIG. 1 illustrates a circuit for processing received ultrasound signals, according to a non-limiting embodiment of the present application. The circuit 100 includes N ultrasonic transducers 102a...102n, wherein N is an integer. The ultrasonic transducers are sensors in some embodiments, producing electrical signals representing received ultrasound signals. The ultrasonic transducers may also transmit ultrasound signals in some embodiments. The ultrasonic transducers may be capacitive micromachined ultrasonic transducers (CMUTs) in some embodiments. The ultrasonic transducers may be piezoelectric micromachined ultrasonic transducers (PMUTs) in some embodiments. Further alternative types of ultrasonic transducers may be used in other embodiments.

[0018] The circuit 100 further comprises N circuitry channels 104a...104n. The circuitry channels may correspond to a respective ultrasonic transducer 102a...102n. For

example, there may be eight ultrasonic transducers 102a...102n and eight corresponding circuitry channels 104a...104n. In some embodiments, the number of ultrasonic transducers 102a...102n may be greater than the number of circuitry channels.

[0019] The circuitry channels 104a...104n may include transmit circuitry, receive circuitry, or both. The transmit circuitry may include transmit decoders 106a...106n coupled to respective pulsers 108a...108n. The pulsers 108a...108n may control the respective ultrasonic transducers 102a...102n to emit ultrasound signals.

[0020] The receive circuitry of the circuitry channels 104a...104n may receive the electrical signals output from respective ultrasonic transducers 102a...102n. In the illustrated example, each circuitry channel 104a...104n includes a respective receive switch 110a...110n and an amplifier 112a...112n. The receive switches 110a...110n may be controlled to activate/deactivate readout of an electrical signal from a given ultrasonic transducer 102a...102n. More generally, the receive switches 110a...110n may be receive circuits, since alternatives to a switch may be employed to perform the same function. The amplifiers 112a...112n, as well as amplifier 300 of FIG. 3 (described below), may be TIAs in some embodiments. One or more of the amplifiers 112a...112n may be variable current amplifiers. As will be described further below, the current of the amplifiers may be varied during an acquisition period, thus adjusting the power consumption, noise level, and linearity of the amplifiers. The amplifiers 112a...112n may output analog signals.

[0021] The circuit 100 further comprises an averaging circuit 114, which is also referred to herein as a summer or a summing amplifier. In some embodiments, the averaging circuit 114 is a buffer or an amplifier. The averaging circuit 114 may receive output signals from one or more of the amplifiers 112a...112n and may provide an averaged output signal. The averaged output signal may be formed in part by adding or subtracting the signals from the various amplifiers 112a...112n. The averaging circuit 114 may include a variable feedback resistance. The value of the variable feedback resistance may be adjusted dynamically based upon the number of amplifiers 112a...112n from which the averaging circuit receives signals. In some embodiments, the variable resistance may include N resistance settings. That is, the variable resistance may have a number of resistance settings corresponding to the number of circuitry channels 104a...104n. Thus, the average output signal may also be formed in part by application of the selected resistance to the combined signal received at the inputs of the averaging circuit 114.

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[0022] The averaging circuit 114 is coupled to an auto-zero block 116. The auto-zero block 116 is coupled to a programmable gain amplifier 118 which includes an attenuator 120 and a fixed gain amplifier 122. The programmable gain amplifier 118 is coupled to an ADC 126 via ADC drivers 124. In the illustrated example, the ADC drivers 124 include a first ADC driver 125a and a second ADC driver 125b. The ADC 126 digitizes the signal(s) from the averaging circuit 114.

[0023] While FIG. 1 illustrates a number of components as part of a circuit of an ultrasound device, it should be appreciated that the various aspects described herein are not limited to the exact components or configuration of components illustrated. For example, aspects of the present application relate to the amplifiers 112a...112n, and the components illustrated downstream of those amplifiers in circuit 100 are optional in some embodiments.

[0024] The components of FIG. 1 may be located on a single substrate or on different substrates. For example, as illustrated, the ultrasonic transducers 102a...102n may be on a first substrate 128a and the remaining illustrated components may be on a second substrate 128b. The first and/or second substrates may be semiconductor substrates, such as silicon substrates. In an alternative embodiment, the components of FIG. 1 may be on a single substrate. For example, the ultrasonic transducers 102a...102n and the illustrated circuitry may be monolithically integrated on the same semiconductor die. Such integration may be facilitated by using CMUTs as the ultrasonic transducers.

[0025] According to an embodiment, the components of FIG. 1 form part of an ultrasound probe. The ultrasound probe may be handheld. In some embodiments, the components of FIG. 1 form part of an ultrasound patch configured to be worn by a patient.

[0026] FIG. 2 illustrates a non-limiting example of the amplifier 112a of FIG. 1 in greater detail. The same configuration may be used for the other amplifiers 112n of FIG. 1. For context, the ultrasonic transducer 102a and averaging circuit 114 are also illustrated, while for simplicity the receive switch 110a is omitted.

[0027] In this non-limiting embodiment, the amplifier 112a is implemented as a two-stage operational amplifier (“op-amp” for short). The first stage 202 is coupled to the ultrasonic transducer 102a. The second stage 204 is coupled between the first stage 202 and the averaging circuit 114. The second stage 204 provides the output signal of the amplifier 112a, in this non-limiting example.

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[0028] The first stage 202 and second stage 204 each have a variable current source. The variable current source 203 is provided for the first stage 202 and sinks a current **I1**. The variable current source 205 is provided for the second stage 204 and sinks a current **I2**. Although the variable current sources 203 and 205 are illustrated as distinct from the respective stages 202 and 204, they may be considered part of the respective stages.

[0029] With a two-stage amplifier construction as shown in FIG. 2, the noise and linearity of the amplified signal may be controlled independently. The noise of the amplifier 112a is impacted primarily by the first stage 202. The linearity of the amplifier 112a is impacted primarily by the second stage 204. More generally, the same may be true for a multi-stage amplifier having two or more stages, such that the noise of the amplifier is impacted primarily by the first stage and the linearity of the amplifier is impacted primarily by the last stage. Applicant has appreciated that during acquisition of an ultrasound signal, referred to herein as an acquisition period, the noise and linearity of the amplified signal may vary in importance. When the ultrasound signal is initially received, early in the acquisition period and corresponding to shallow depths when the ultrasound signal is a reflected signal, the associated noise will be relatively low compared to the received signal amplitude, but the linearity of the amplified signal may be of relatively high importance. However, later during the acquisition period, corresponding to greater depths when the ultrasound signal is a reflected signal, the ultrasound signal is likely to become smaller, and thus the noise of the signal is of increased importance. Thus, the amplifier 112a of FIG. 2 is designed to allow for independent and variable control of noise and linearity. The control may be provided via the variable current sources 203 and 205.

[0030] Early during an acquisition period, the variable current source 203 may be controlled to sink a relatively small amount of current, while the current source 205 may be controlled to sink a relatively large amount of current. In such a scenario, the second stage 204 may operate to control the linearity of the amplified signal produced by the amplifier 112a, while the first stage 202 may control the noise of the amplified signal 202 to a lesser extent than that to which it is capable. Later in the acquisition period, the current sunk by the variable current source 203 may be increased while the current sunk by the variable current source 205 may be decreased. As the current sunk by the variable current source 203 is increased, the first stage 202 may operate to control the noise of the amplifier 112a to a greater extent. As the current sunk by the variable current source 205 is decreased, the second stage 204 may operate to control the linearity of the amplifier 112a to a lesser extent. Thus, dynamic current biasing of

the amplifier 112a, and first stage 202 and second stage 204 more specifically, may be implemented to control the power, noise, and linearity characteristics of the amplifier during an acquisition period.

[0031] The dynamic control of current sources 203 and 205 may be achieved using a digital controller, an example being shown in FIG. 3A. The variable current sources 203 and 205 may each include two or more programmable current settings. The greater the number of settings, the greater the control over the current sunk by the current sources 203 and 205.

[0032] The amplifier 112a also includes a variable feedback impedance 206. In some embodiments, the variable feedback impedance is a variable RC feedback circuit. An example of the variable RC feedback circuit is illustrated in FIG. 3A and described in connection with that figure. The feedback impedance determines the transimpedance gain of the transimpedance amplifier, such that the input current signal may be converted into an output voltage of varying amplitude.

[0033] It should be appreciated from FIG. 2 and the foregoing description that an embodiment of the application provides a multi-stage TIA having two or more independently controllable variable current sources, with a variable feedback impedance. The variable current sources may allow for dynamic current biasing of the TIA, for example during an acquisition period. Thus, the power consumption, noise, and linearity of the amplifier may be adjusted during the acquisition period.

[0034] FIG. 3A is a circuit diagram illustrating an implementation of the amplifier 112a of FIG. 2, according to a non-limiting embodiment of the present application. The amplifier 300 has an input 302 and an output 304. The input 302 may be coupled to an ultrasonic transducer or a receive switch, as described previously in connection with FIGs. 1 and 2, and may receive an electrical signal representing an ultrasound signal received by the ultrasonic transducer. The output 304 may provide an amplified output signal of the amplifier 112a, and may be coupled to an averaging circuit or other component to which it is desired to provide the amplified output signal.

[0035] The amplifier 300 includes a first stage 306 and a second stage 308, which may be implementations of the first stage 202 and second stage 204 of FIG. 2, respectively. The first stage 306 includes an NMOS transistor 310 having a gate configured to receive the signal at input 302. PMOS transistor 312 and PMOS transistor 314 have their gates coupled, with the drain of PMOS transistor 312 coupled to the drain of NMOS transistor 310. The gate of

transistor 312 is coupled to its drain. Transistors 312 and 314 are also configured to receive a power supply voltage **VDDA**. The first stage 306 further comprises NMOS transistor 316 having a gate configured to receive a bias voltage provided by an RC circuit. The RC circuit includes two resistors, of value R , with a capacitor C_b coupled in parallel with one of the resistors. The other resistor receives the power supply voltage **VDDA**. The drain of PMOS transistor 314 is coupled to the drain of NMOS transistor 316. An example value for R is 50 kOhm and an example value for C_b is 10 pF, although alternatives for both are possible, such as +/- 20% of those values listed, or any value or range of values within such ranges.

[0036] The second stage 308 includes a PMOS transistor 318 configured to receive the output of the first stage 306. In particular, the gate of PMOS transistor 318 is coupled to a node between transistors 314 and 316 of the first stage 306. The source of PMOS transistor 318 receives **VDDA**. A variable impedance circuit 320 is also provided in the second stage 308. The variable impedance circuit 320 includes a variable capacitor C_C in series with a variable resistor R_Z , and thus is a variable RC circuit in this embodiment. Variable impedance circuit 320 may provide stable operation of the amplifier 300 when the gain of the amplifier, or the currents of the currents sources, are varied. Thus, the variable impedance circuit may be provided to maintain stable operation of the amplifier 300 for all the current magnitudes sunk by the variable current sources 321 and 325. That is, the values of C_C and R_Z may be adjusted during operation of the amplifier 300 to account for the different current settings programmed by the digital controller 330

[0037] A variable current source is provided for each of the stages 306 and 308. The variable current source 321 for the first stage 306 includes three parallel connected current sources 322a, 322b, and 322c. Current source 322a sinks a current I_A , current source 322b sinks a current $2I_A$, and current source 322c sinks a current $4I_A$. The current sources 322a-322c are coupled to the first stage 306 by respective switches 324a, 324b, and 324c, which effectively provides 3 bits (8 states) of control of the current. The current I_A may equal 100 microAmps or +/-20% of that value, or any value or range of values within such ranges, as examples.

[0038] The variable current source 325 for the second stage 308 includes three parallel connected current sources 326a, 326b, and 326c. Current source 326a sinks a current I_B , current source 326b sinks a current $2I_B$, and current source 326c sinks a current $4I_B$. The current sources 326a-326c are coupled to the second stage 308 by respective switches 328a, 328b, and 328c, which effectively provides 3 bits (8 states) of control of the current. The current I_B may equal

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50 microAmps or +/-20% of that value, or any value or range of values within such ranges, as examples.

[0039] While FIG. 3A illustrates variable current sources each include three parallel-coupled current sources, it should be appreciated that not all aspects of the present application are limited in this manner. That is, variable current sources may be implemented in various manners, including alternative manners to those illustrated. For example, more or fewer than three current sources may be coupled in parallel to create a variable current source. Also, the magnitudes of the current sources may be different than those illustrated in FIG. 3A. Any suitable magnitudes may be provided to allow for operation over a desired range of currents.

[0040] A digital controller 330 is provided to control operation of the variable current sources 321 and 325. The digital controller provides control signals to (digitally) program the currents of the variable current sources. In the illustrated example, the digital controller 330 provides one or more switching signals **S1** to control operation of the switches 324a-324c, and one or more switching signals **S2** to control operation of the switches 328a-328c. In this manner, the amount of current sunk by the variable current sources may be varied independently during operation of the amplifier 300, for example during an acquisition period. According to a non-limiting example, the digital controller 330 decreases the current sunk by variable current source 325 during the acquisition period and increases the current sunk by variable current source 321 during the acquisition period through suitable operation of the switching signals **S1** and **S2**.

[0041] The digital controller 330 may be any suitable type of controller. The digital controller may include integrated circuitry. In some embodiments, the digital controller 330 may include or be part of an application specific integrated circuit (ASIC). In some embodiments, the digital controller 330 may not be specific to the amplifier 300. For example, a digital controller may be provided to control more than one component of the circuit of FIG. 1, one of which may be the amplifiers 112a...112n.

[0042] The amplifier 300 further includes a variable feedback impedance 332 formed by variable capacitor C_f and variable resistor R_f . The capacitor C_f and resistor R_f may be coupled between the output 304 and the input 302, and may be in parallel with each other. The variable feedback impedance 332 may control the gain of the amplifier 300. Thus, the values of C_f and R_f may be adjusted to vary the amplifier's gain.

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[0043] The variable feedback impedance 332 and the variable impedance circuit 320 may be controlled in any suitable manner. In one embodiment, the digital controller 330 may set the values of the feedback impedances. However, alternatives manners of control may be used.

[0044] It should be appreciated that the described groupings of components in connection with FIG. 3A are not limiting. For example, while certain components illustrated in that figure are described as being part of a first stage or a second stage, the identification of the first and second stages is not limiting. The first and second stages may include more, fewer, or different components than those illustrated.

[0045] FIG. 3B is a circuit diagram of an implementation of the variable impedance circuit 320 of FIG. 3A, according to a non-limiting embodiment of the present application. The variable impedance circuit 320 includes a number of switches 340a...340n configured in parallel and configured to receive respective control signals **SWa...SWn**. In some embodiments, the digital controller 330 may provide the control signals **SWa...SWn**, although alternatives may be used. Each switch is coupled in series with a respective capacitor C_C and resistor R_Z . The impedance of the variable impedance circuit 320 may be adjusted during an acquisition period through suitable provision of the control signals **SWa...SWn**. Any suitable number of parallel signal paths may be provided, so that the illustrated example of two parallel signal paths is non-limiting. The number of parallel signal paths and the capacitance and resistive values provided may be selected to provide sufficient control of the feedback impedance to account for the variable operation of the amplifier across the range of operating scenarios resulting from the variation of the variable current sources. For example, for a given amplifier gain dictated by variable feedback impedance 332, appropriate settings of variable impedance circuit 320 may be selected. In some embodiments, a lookup table may be utilized to determine the appropriate settings of variable impedance circuit 320 based on a given gain set by variable feedback impedance 332.

[0046] In both FIGs. 3A and 3B, the values of C_C and R_Z may be selected to provide desired operating characteristics. As examples, R_Z may be equal to 3 kOhms in some embodiments, and C_C may be equal to 300 fF. Alternatives for both are possible. For example, they may assume values within +/- 20% of those values listed, or any value or range of values within such ranges.

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[0047] FIG. 3C is a circuit diagram of an implementation of the variable impedance circuit 332 of FIG. 3A, according to a non-limiting embodiment of the present application. The variable impedance circuit 332 includes a number of complementary switches 350a, 350b...350n. Each switch receives respective control signals **SLa**, **SLb**...**SLn** and **SHa**, **SHb**...**SHn**. The control signals may be provided by the digital controller 330 in some embodiments, although alternatives may be used. The complementary switches are coupled to respective parallel-connected RC circuits C_f , R_f . While three complementary switches are shown in FIG. 3C, any suitable number may be provided to allow for sufficient control of the gain of the amplifier 300.

[0048] In both FIGs. 3A and 3C, the values of C_f and R_f may be selected to provide desired operating characteristics. As examples, R_f may be equal to 180 kOhms in some embodiments, and C_f may be equal to 84 fF. Alternatives for both are possible. For example, they may assume values within +/- 20% of those values listed, or any value or range of values within such ranges.

[0049] FIG. 4 is a graph illustrating the behavior of two variable current sources of a variable current amplifier during an acquisition period, as may be implemented by the amplifier of FIGs. 2 and 3A, which again may be a TIA. For example, the illustrated behavior may be implemented by the variable current sources 203 and 205 of FIG. 2. The x-axis represents time during an acquisition period, ranging from **t0** to **t8**. The y-axis represents the current of the current source, having values ranging from **I0** to **I8**. The values of **t0-t8** and **I0-I8** may be any suitable values for operation of a given ultrasound system, as the various aspects described herein are not limited to implementation of any specific time or current values. Also, the number of time intervals during an acquisition period is non-limiting, as more or fewer may be implemented. The number of current values which may be implemented is non-limiting, as more or fewer may be implemented.

[0050] Curve 402 represents the current of a variable current source of a second stage of a variable current amplifier. Thus, curve 402 may represent the current of current source 205 of FIG. 2. Curve 404 represents the current of a variable current source of a first stage of the variable current amplifier. Thus, curve 404 may represent the current of current source 203 of FIG. 2.

[0051] FIG. 4 illustrates that the currents of the first and second stages of the variable current amplifier move in opposing directions during the acquisition period. That is, curve 402

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decreases moving from time **t0** to time **t8**, while curve 404 increases during the same time. As previously described in connection with FIG. 2, the first and second stages of the variable current amplifier may impact different characteristics of the variable current amplifier behavior, such as noise and linearity. Thus, when operating in the manner illustrated in FIG. 4, the impact of the two stages of the variable current amplifier may vary during the acquisition period. That is, the impact of the second stage may be greater initially, up to time **t4**, while the impact of the first stage may be greater thereafter, from time **t4** to time **t8**.

[0052] As previously described in connection with FIG. 3A, the currents of the two stages of a two-stage op-amp being used to implement a variable current amplifier may be controlled by digital codes. Thus, the current values **I0-I7** of FIG. 4 may correspond to different digital codes set by a digital controller, such as digital controller 330 of FIG. 3A.

[0053] While FIG. 4 illustrates that the currents in the first and second stages of the amplifier switch at the same times, not all embodiments are limited in this respect. For example, the current in the second stage could be adjusted at times offset from those at which the current in the first stage is adjusted. Likewise, the currents of the two stages need not be adjusted the same number of times during an acquisition period.

[0054] As described previously, an aspect of the present application provides an amplifier with a variable current source which is controlled to adjust the noise of the amplifier during an acquisition period. FIG. 5 illustrates an example of such operation.

[0055] In FIG. 5, the voltage of an electrical signal 502 output by an ultrasonic transducer, and thus representing a detected ultrasound signal, is illustrated as a function of time. Dashed line 504 represents the noise floor of an amplifier used to amplify the electrical signal 502, and may correspond to the noise floor of an amplifier of the types described herein, such as amplifier 112a. It can be seen that during the acquisition period, the magnitude of the electrical signal decreases. Likewise, the noise floor of the amplifier is decreased. Such a decrease in the noise floor may be achieved by controlling the current sunk by a variable current source of the amplifier in the manner described previously herein. For example, referring to FIG. 2, the variable current source 203 may be increased during the acquisition period to decrease the noise floor of the amplifier 112a. The noise floor may be adjusted to a level which provides an acceptable signal-to-noise ratio (SNR).

[0056] FIG. 5 also illustrates a constant noise floor 506. It can be seen that while the constant noise floor 506 is at the same level as dashed line 504 toward the end of the acquisition

period, the constant noise floor 506 is lower than the value of the dashed line 504 up to that point. As has been described herein, the noise level of an amplifier may be dependent on the current consumed by the amplifier, and in such situations it should be appreciated that operating with a constant noise floor 506 requires significantly more current (and therefore power) than operating according to dashed line 504. Thus, aspects of the present application providing for a variable current amplifier to amplify ultrasound signals may provide substantial power savings compared to amplifiers operating with a constant noise level.

[0057] The amount of power savings may be significant. For example, in the circuit 100, the amplifiers 112a...112n may consume a significant amount of power. In some embodiments, the amplifiers 112a...112n may consume more power than any other components of the circuit 100. Accordingly, reducing the power consumption of the amplifiers 112a...112n may provide a significant reduction in power of the circuit 100. In some embodiments, utilizing variable current amplifiers of the types described herein may provide up to a 25% power reduction, up to a 40% power reduction, up to a 50% power reduction, or any range or value within such ranges, in terms of the operation of the amplifier. The resulting power reduction for the circuit 100 may be up to 10%, up to 20%, up to 25%, or any range or value within such ranges.

[0058] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described.

[0059] As an example, certain embodiments described herein have focused on two-stage amplifiers. However, the techniques described herein may apply to multi-stage amplifiers having two or more stages. When more than two stages are used, the first stage may predominantly control the noise of the amplifier, while the last stage may predominantly control the linearity of the amplifier.

[0060] As described, some aspects may be embodied as one or more methods. The acts performed as part of the method(s) may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than

illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0061] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0062] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, *i.e.*, elements that are conjunctively present in some cases and disjunctively present in other cases.

[0063] As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements.

[0064] As used herein, the term “between” used in a numerical context is to be inclusive unless indicated otherwise. For example, “between A and B” includes A and B unless indicated otherwise.

[0065] In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, *i.e.*, to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively.

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CLAIMS

1. An ultrasound apparatus, comprising:
 - an ultrasound sensor;
 - a variable current trans-impedance amplifier (TIA) coupled to the ultrasound sensor and configured to receive and amplify an output signal from the ultrasound sensor, the variable current TIA having a variable current source.
2. The ultrasound apparatus of claim 1, the variable current TIA being a two-stage operational amplifier having a first stage and a second stage, wherein the variable current source includes a first variable current source coupled to the first stage and a second variable current source coupled to the second stage.
3. The ultrasound apparatus of claim 2, wherein the first and second variable current sources are independently controllable.
4. The ultrasound apparatus of claim 2, wherein the first and second variable current sources are digitally programmable.
5. The ultrasound apparatus of claim 2, wherein the first stage is arranged to receive the output signal from the ultrasound sensor and the second stage is arranged to provide an output signal of the variable current TIA.
6. The ultrasound apparatus of claim 2, wherein the variable current TIA further comprises a variable feedback RC circuit coupled between an output terminal of the variable current TIA and a node representing an input to the second stage.
7. The ultrasound apparatus of claim 1, further comprising a control circuit coupled to the variable current source and configured to control an amount of current through the variable current source.

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8. The ultrasound apparatus of claim 1, wherein the ultrasound sensor and the variable current TIA are monolithically integrated on a semiconductor chip.

9. The ultrasound apparatus of claim 1, the variable current TIA being a multi-stage operational amplifier having a first stage and a last stage, wherein the variable current source includes a first variable current source coupled to the first stage and a second variable current source coupled to the last stage.

10. A method, comprising:

acquiring an ultrasound signal with an ultrasound sensor during an acquisition period and outputting, from the ultrasound sensor, an analog electrical signal representing the ultrasound signal; and

amplifying the electrical signal with a variable current trans-impedance amplifier (TIA), including varying a current of the variable current TIA during the acquisition period.

11. The method of claim 10, wherein the variable current TIA is a two-stage operational amplifier having a first stage and a second stage, and wherein varying a current of the variable current TIA during the acquisition period includes independently varying a current of the first stage and a current of the second stage.

12. The method of claim 11, wherein the variable current TIA further comprises a first variable current source coupled to the first stage a second variable current source coupled to the second stage, and wherein independently varying a current of the first stage and a current of the second stage comprises digitally programming the first and second variable current sources.

13. The method of claim 11, wherein independently varying a current of the first stage and a current of the second stage further comprises increasing the current of the first stage during the acquisition period and decreasing the current of the second stage during the acquisition period.

14. The method of claim 10, further comprising varying a feedback capacitance or feedback resistance of the variable current TIA during the acquisition period.

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15. The method of claim 14, wherein varying the feedback capacitance or feedback resistance further comprises varying the feedback capacitance or feedback resistance in concert with varying the current.

16. A method, comprising:

acquiring an ultrasound signal with an ultrasound sensor during an acquisition period and outputting, from the ultrasound sensor, an analog electrical signal representing the ultrasound signal; and

amplifying the electrical signal with a variable current trans-impedance amplifier (TIA), including decreasing a noise floor of the variable current TIA during the acquisition period.

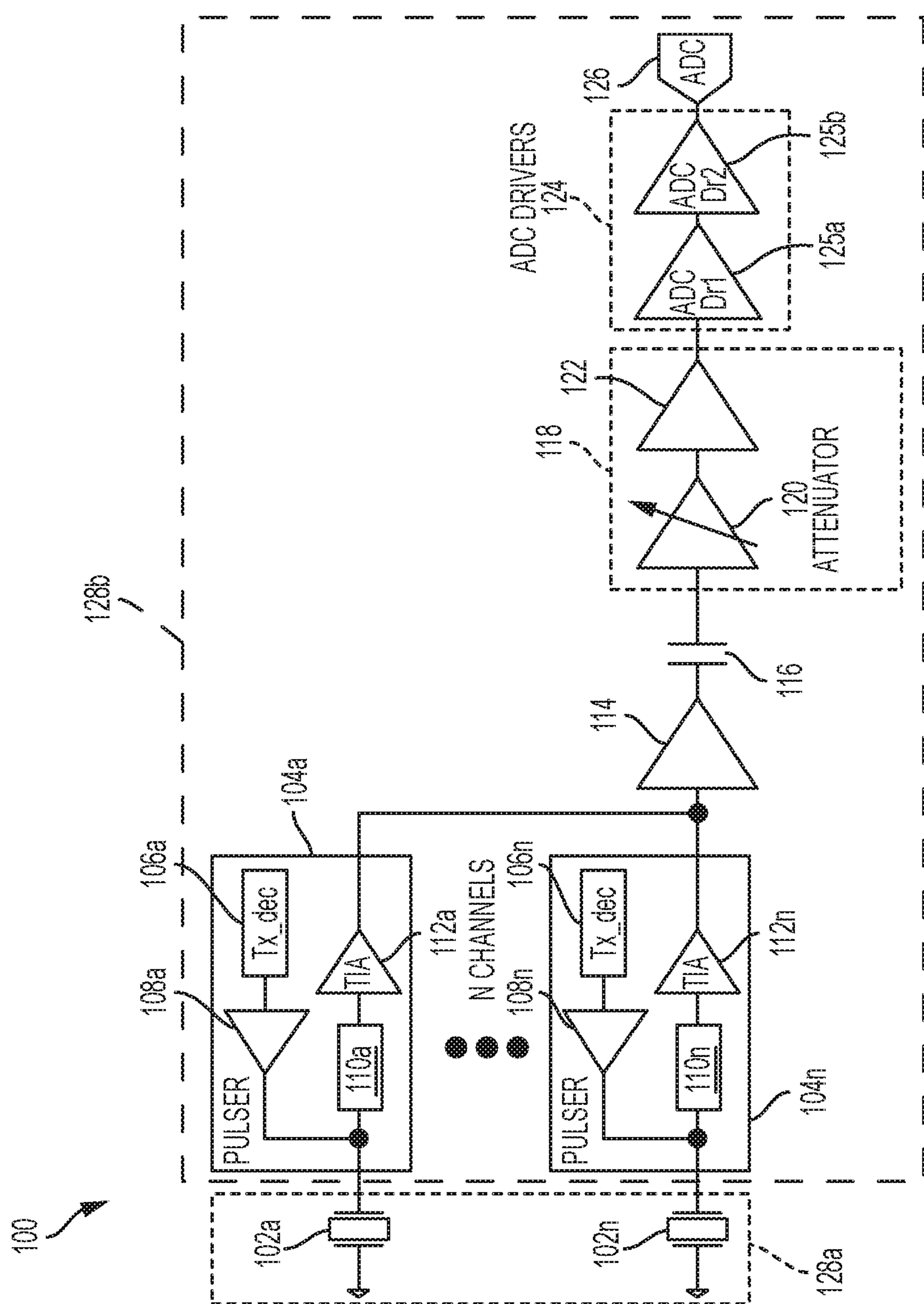


FIG. 1

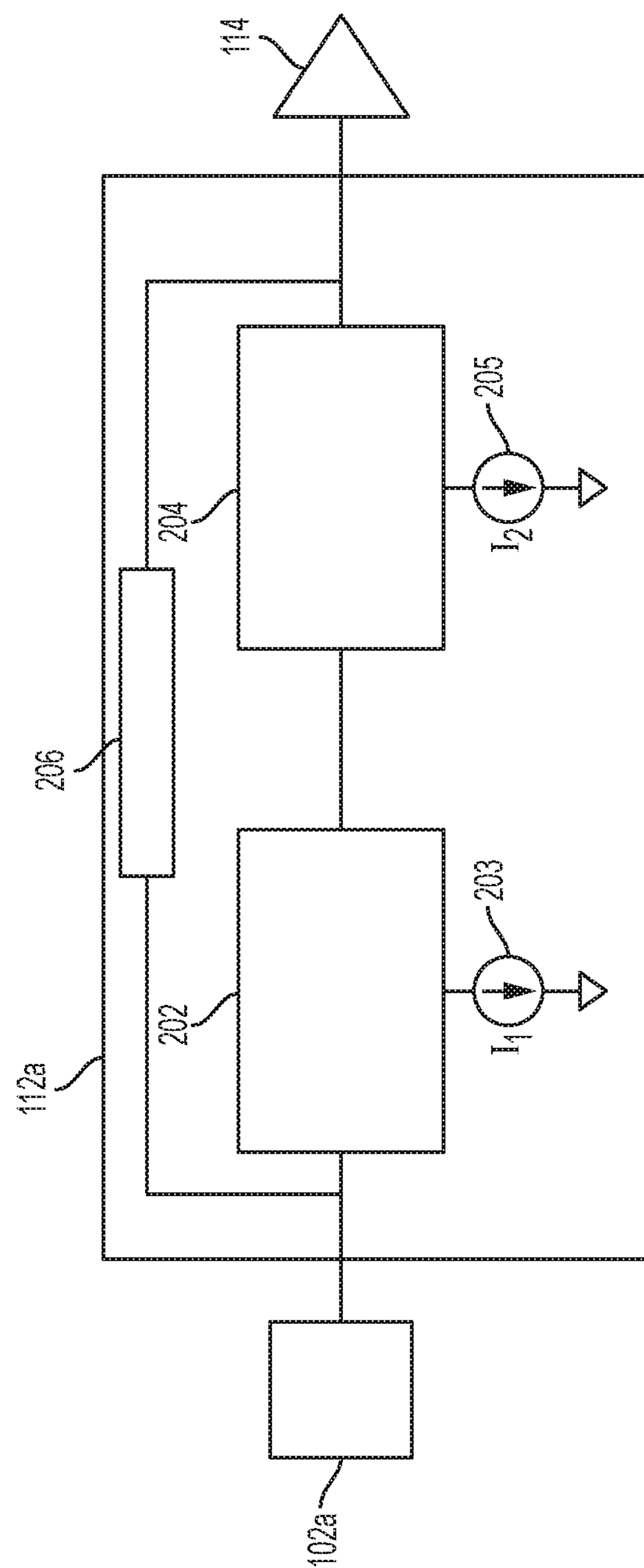


FIG. 2

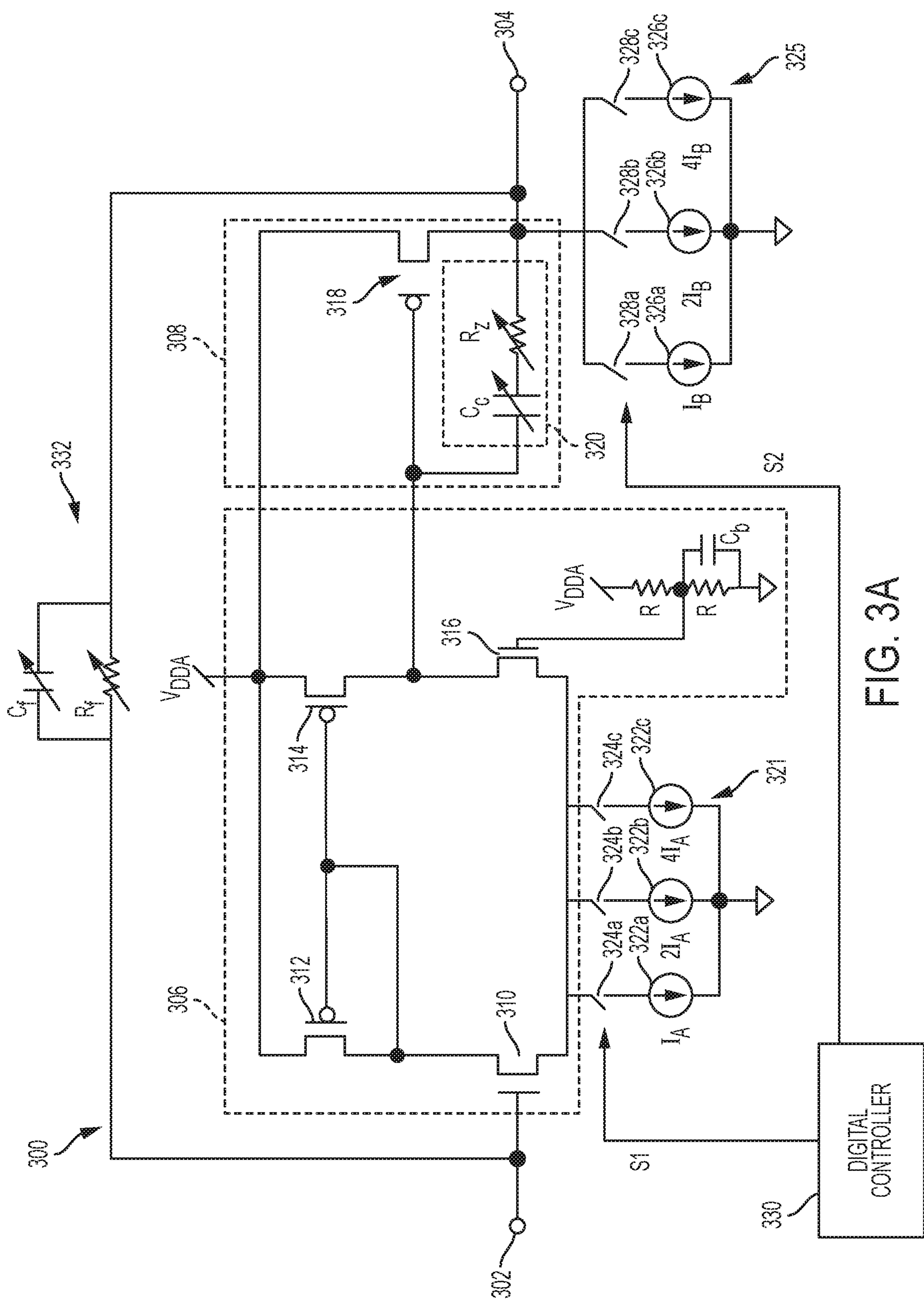


FIG. 3A

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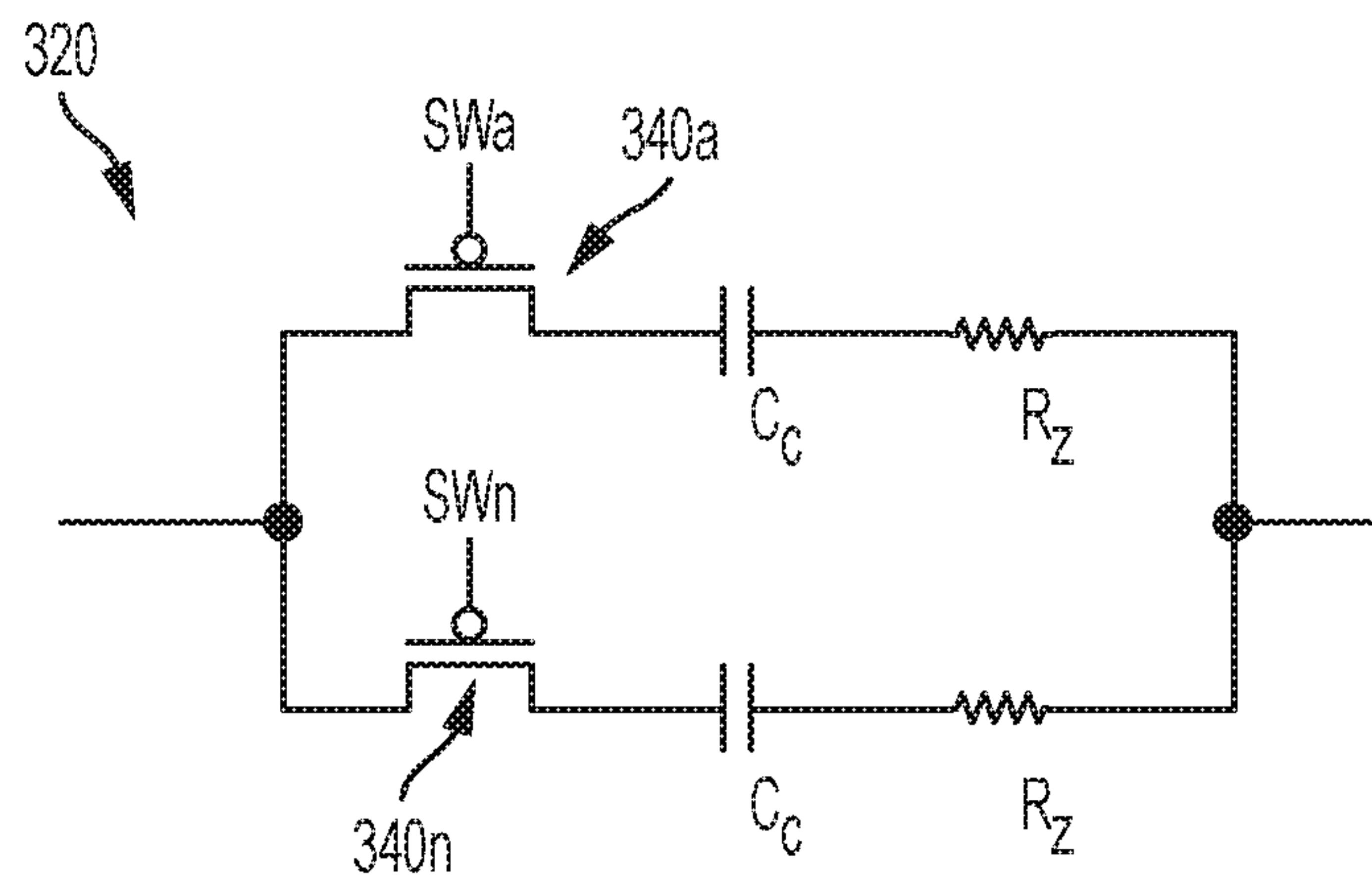


FIG. 3B

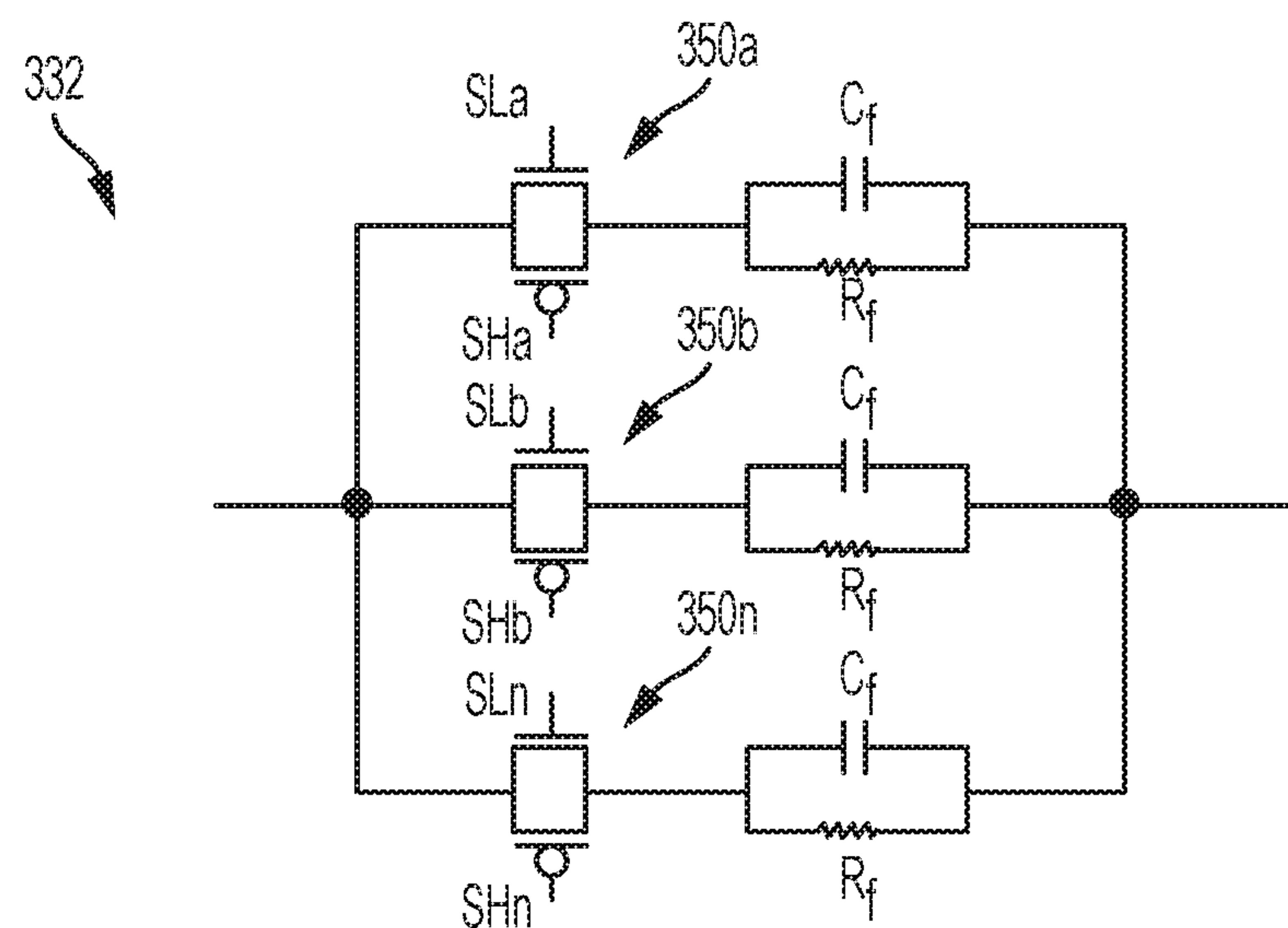


FIG. 3C

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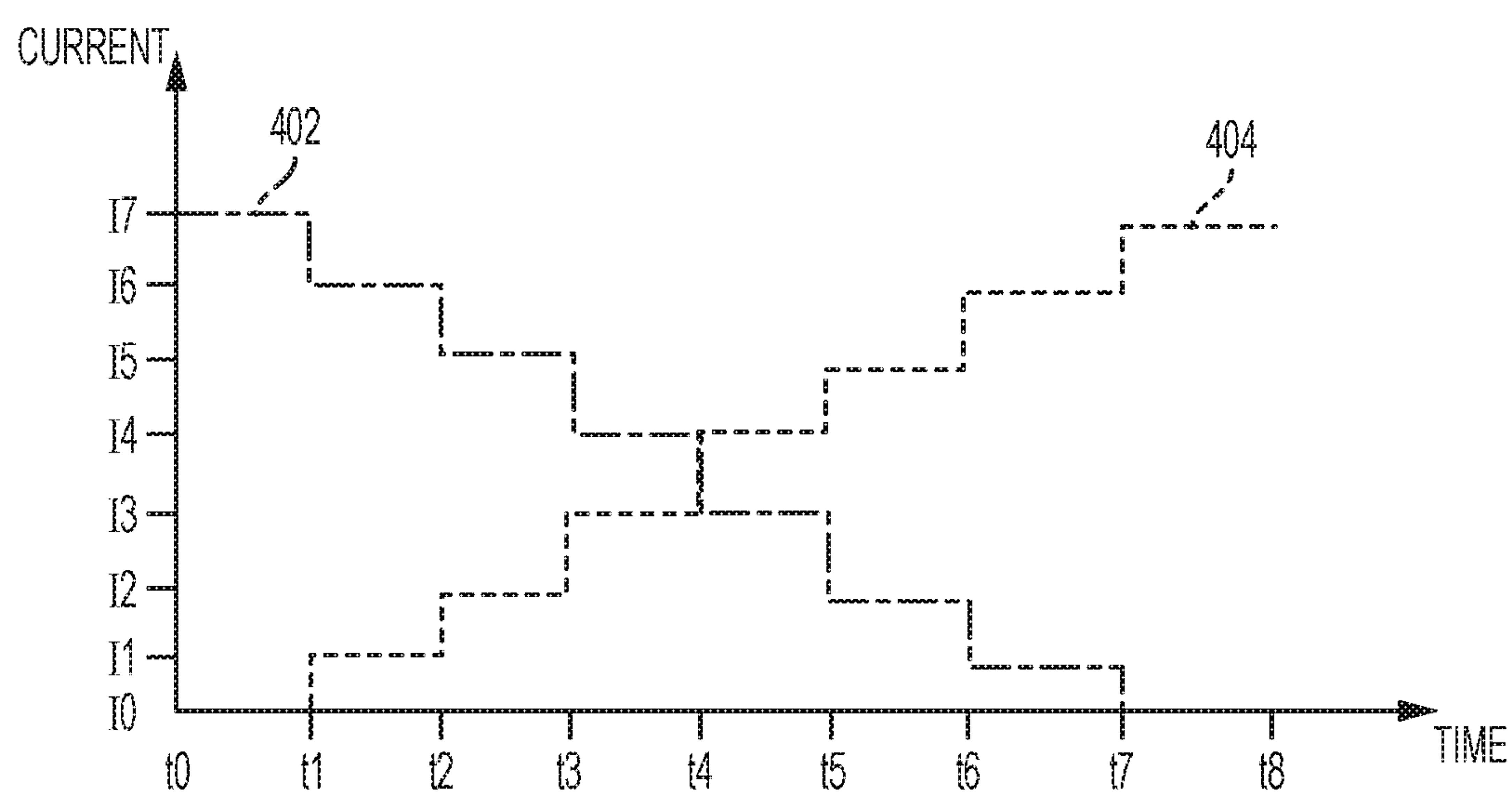


FIG. 4

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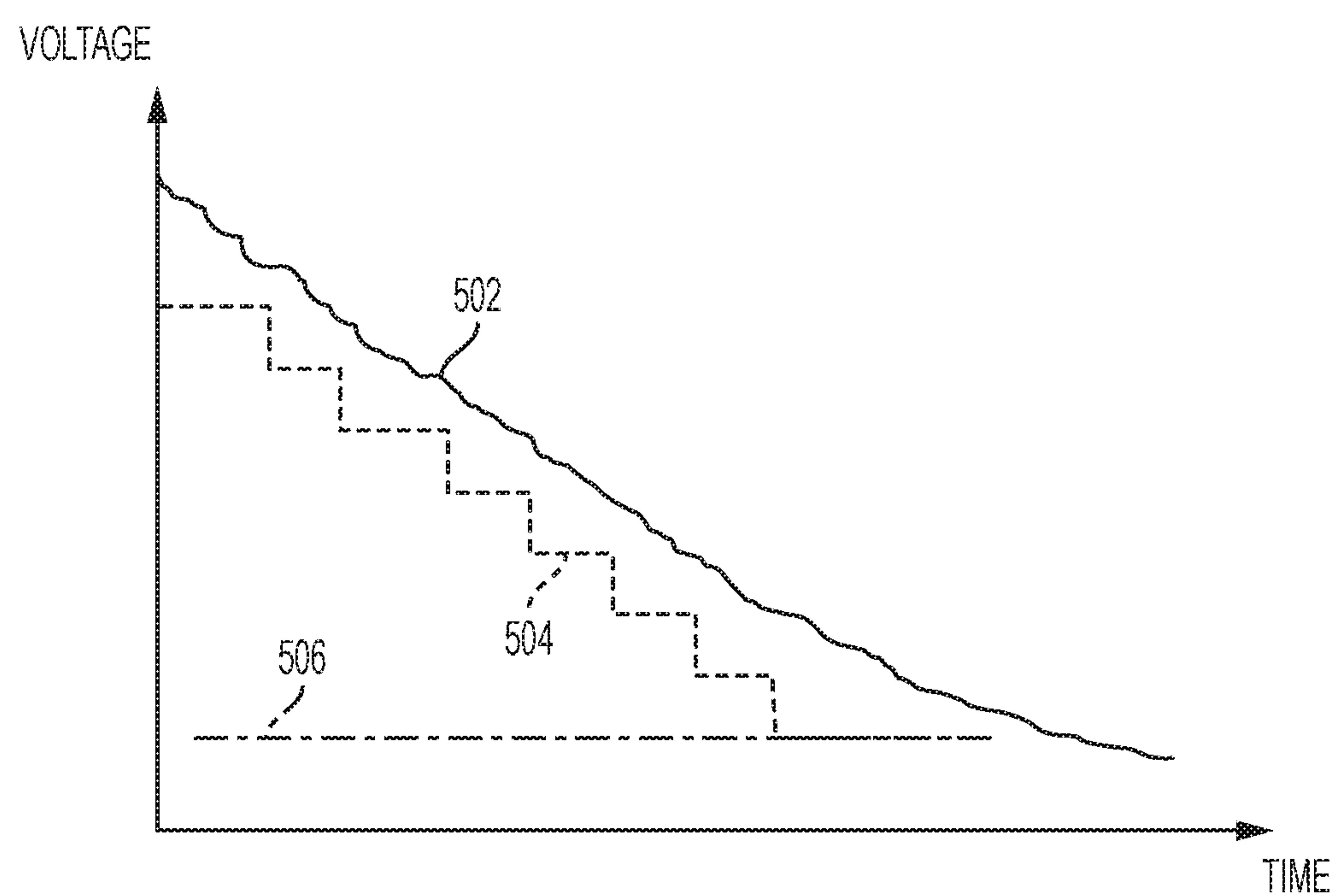


FIG. 5

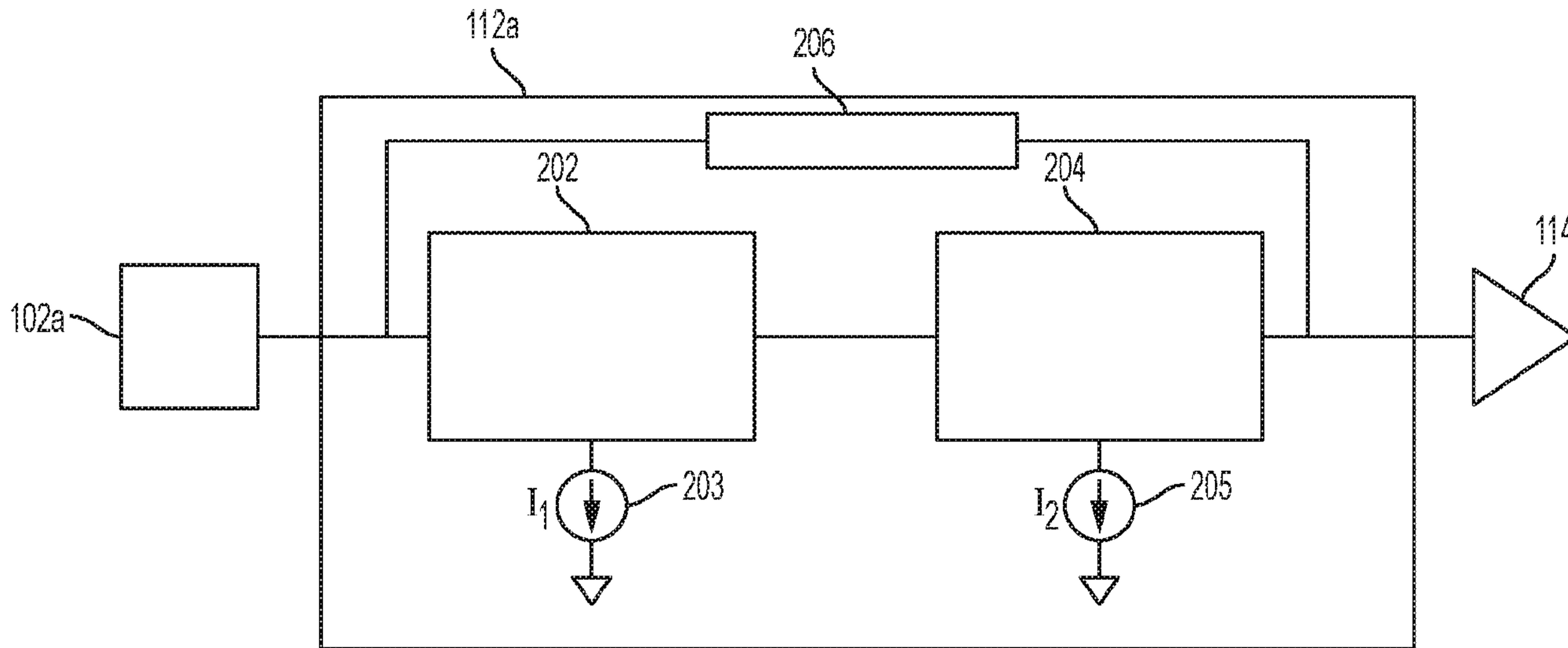


FIG. 2