



- (51) **International Patent Classification:**
H01L 31/0224 (2006.01) *H01L 31/18* (2006.01)
- (21) **International Application Number:**
PCT/NL2012/050067
- (22) **International Filing Date:**
8 February 2012 (08.02.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
2006160 8 February 2011 (08.02.2011) NL
2006161 8 February 2011 (08.02.2011) NL
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- (81) **Designated States (unless otherwise indicated, for every
kind of national protection available):** AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD,
SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States (unless otherwise indicated, for every
kind of regional protection available):** ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

Published:

- without international search report and to be republished
upon receipt of that report (Rule 48.2(g))

(54) **Title:** A METHOD OF MANUFACTURING A SOLAR CELL AND A SOLAR CELL

(57) **Abstract:** In the solar cell manufacture a diffusion resistance layer (22A) of electrically insulating material is provided onto the first side (11) of a semiconductor substrate (10), and patterned in accordance with a predefined pattern of selective emitter regions (30) to be applied into the semiconductor substrate; dopant species are provided into the semiconductor substrate (10) to form the selective emitter regions (30) comprising p-type charge carriers. Subsequently, selective dopant diffusion regions (31) are created through controlled diffusion of further dopant species through the diffusion resistance layer (22a), the selective emitter regions (30) and the diffusion regions (31) jointly operating as emitter. The diffusion resistance layer (22) will also extend into any through-hole (20) in the substrate(10).



A method of manufacturing a solar cell and a solar cell

FIELD OF THE INVENTION

The invention relates to a method of manufacturing a solar
5 cell comprising a semiconductor substrate with a first and a
second side, back contacts at the second side and emitter regions
defined at the first side, conductors extending from the first
side to the second side.

The invention further relates to such a solar cell and a solar
10 panel comprising such solar cell.

BACKGROUND OF THE INVENTION

Solar cells are large area semiconductor devices which
convert radiation (i.e. sunlight) into electricity. One important
15 class of solar cells is the group of back-contacted solar cells,
meaning that both ohmic contacts to the two oppositely doped
regions of the solar cells are placed on the second, i.e. back
surface of the solar cell. This class of solar cells reduces
shadowing losses caused by the front metal contact grid on
20 standard solar cells. Suitably, an emitter is provided on the
front or first side (the terms side and surface are hereinafter
used interchangeably) of the semiconductor substrate (hereinafter also
referred to as substrate). Therewith it is achieved that the
junction between the oppositely charged regions in the substrate
25 is close to the front surface which receives the incoming
radiation. Typically, the emitter extends along the conductors
through the substrate to its second side.

An example of such a solar cell is known from US3.903.428.
This patent proposes the vias for the conductors. Patent EP0985233
30 is another example. After creating the via, phosphorous or any
other dopant is introduced in both surfaces of the substrate
including the walls of the vias in order to create a homogeneous
and continuous emitter on both surfaces of the substrate. This
results in a double carrier collecting junction, since the
35 junction is not only present near the front surface, but also near
the back surface, and hence is double. The patent gives the

example wherein the substrate is p-type doped and the emitter is n-type doped. Possible techniques to form an n-emitter include the screen printing of a phosphorous containing paste on the areas of the cell where an emitter is to be created; the use of a gaseous source such as POCl_3 ; spin-on and spray-on deposition techniques. Techniques such as ion implantation would be possible but not at an industrial level as yet; the solar cell is a large scale and relatively cheap product per m^2 surface area, when compared to other silicon based products such as integrated circuits.

J. Szlufcik et al., *Opto-Electr. Rev.*, **8** (2000), 299-305 have worked on an alternative for the homogeneous emitter. This is called a selective emitter. Herein, the emitter is partially present below the metallic conductor, particularly a grid of conductors, and partially below a surface passivation. The emitter region below the surface passivation is shallow and lowly doped, while the selective emitter beneath the metal conductor is highly doped and extends more deeply into the substrate. Due to its high doping level, the selective emitter gives rise to lowly resistive contacts with the metal. The shallow extension and low doping of the emitter region, also diffusion region beneath an effective surface passivation reduces the emitter dark saturation current. Szlufcik et al. propose the use of screen printing of phosphorous paste on the locations where the selective emitter is to be formed. These locations are for instance defined in the form of a finger pattern. Thereafter, a diffusion step occurs. The areas where the doping is directly deposited are deeply diffused whereas the areas in between the "fingers" are shallowly diffused due to gas phase transportation of doping at the surface. The subsequent surface passivation is suitably applied by phase enhanced Chemical Vapour Deposition (PECVD) and is for instance a SiN_x -layer. This silicon nitride layer also forms the antireflection coating (ARC) typically present on the front surface (i.e. first side) of the semiconductor substrate. Alternatively, use can be made of a diffusion barrier. The doping, typically indicated as phosphorous doping, is then typically provided from the gas phase as POCl_3 and thereafter diffused through the diffusion barrier so as to create

a lowly doped shallow diffusion region. Such a diffusion barrier could also be screen printed on the surface. It is then typically a paste with SiO_2 as active component.

WO2010/052565 discloses a process for two-stage doping leading to a selective emitter. According to the process, a substrate (i.e. wafer) is provided with an oxide, particularly a thermal oxide, extending on all sides. The oxide is locally opened by means of a laser. Subsequent to cleansing of the oxide, so as to reduce the oxide thickness, doping is carried out by means of phosphorous diffusion. Herein, a high dopant area is formed in the opened region of the oxide, while the dopant further diffuses through the oxide layer. After removal of the remnants of the oxide layer an anti-reflection coating is provided. It is a first disadvantage of this process that the diffusion speed through the oxide layer is determined by the combination of thermal oxidation and cleansing. An appropriate control of the thickness of the remaining oxide in such a multistep process is all but evident. Furthermore, the thermal oxidation occurs in view of its temperature at the beginning of the process, resulting therein the diffusion occurs on all sides, unless a further nitride stop layer is provided prior to diffusion. Hence, the overall process is being made complex as a consequence of the application of a two stage doping process through opening and thinning a thermal oxide layer.

Recently, it has been observed that the use of n-type doped semiconductor substrates may lead to higher efficiencies. This requires certain modifications; for a p-type diffusion, typically boron is used, whereas phosphorous is used for the n-type diffusion. Boron diffusion however requires a higher temperature than phosphorous-diffusion. When diffusing the phosphorous, with Boron being present at the same side, then care has to be taken that the phosphorous does not diffuse into the p-type region with boron dopant. One manner of controlling is to apply a laser scribing process subsequently so as to achieve a proper isolation. An alternative manner of controlling, as known from WO2009/064183, is the application of a pre-diffusion step for the diffusion of

phosphorous. It turns out possible in this manner, to apply the phosphorous doping step before the boron doping step. In order to achieve this, the first side is blocked against doping upon provision of the doping on the second side and the second side is blocked against doping while doping the first side.

However, a problem with using boron as the p-type dopant is the risk for creation of boron-rich layers at the substrate surface. Boron diffusion is for instance applied as BBr_3 in an oxygen atmosphere. This converts the BBr_3 to liquid boron oxide (B_2O_3) and gaseous brome (Br_2). The liquid boron oxide condenses on the silicon wafer surface. Chemical reaction with the silicon surface produces silicon oxide (SiO_2) and elemental boron. The SiO_2 is partly dissolved in the liquid B_2O_3 , resulting in a mixed-phase B_2O_3 - SiO_2 system, also known as boron silicate glass (BSG). Mainly during the heat treatment, the elemental boron diffuses according to the boron gradient into the silicon wafer as well as into the BSG system. During this process a very high concentration of boron ("boron pile up") can occur at the surface of the wafer that transforms a surface layer of the silicon wafer into a SiB compound, forming a boron rich layer (BRL). The Si-B compound is particularly hexaborylsilicon (SiB_6). This boron rich layer is however commonly associated with degradation of the carrier lifetime in the bulk of the wafer. The problem tends to become more pronounced due to the presence of through-holes in the substrate, as the effective surface area of the substrate therewith increases and give rise to variations in diffusion of the boron compounds across the wafer.

The method known from WO2009/064183 does not address the problem how to achieve an emitter which does not result in the creation of a boron rich layer.

The method known from WO2010/052565 does not address the complexities of using an n-type substrate, in which the phosphorous doping needs to be replaced by boron doping in an appropriate manner. It is not apparent how to modify the disclosed flowcharts for p-type processes, taking into account the different

temperature regimes of boron and phosphorous doping and taking into account the issues in relation to undesired boron diffusion.

Moreover, also the via formation faces issues when using an n-type substrate. One example of a process for forming back-
5 contacted solar cells, is known from WO2009/067005 A1. This process teaches the provision of aluminum paste that is annealed in the heat treatment. The annealing results in melting and thus a better filling of the via. It further results in alloying of the silicon substrate with the aluminum. But aluminum is also a p-type
10 dopant. Such p-type dopant may diffuse into the n-type substrate and recombine with the n-type charge carriers during the heat treatment. A substrate zone with a very low dopant concentration may then be generated. This substrate zone around the via could act as an insulation so as to prevent that currents running
15 through the via from or to the emitter region will result in leakage currents into the substrate directly.

However, aluminum is known to diffuse in silicon very quickly. In view of the presence of the first and second terminals of opposite polarity adjacent to each other on the second side of
20 the substrate, and the extension of the field region into the semiconductor substrate, a reliability risk is present in that the aluminum will generate a leakage path between the via and the field region.

A further process is known from WO2010/049268A1. As part
25 thereof, a passivation layer is then provided both on the first side and on the walls of the through-holes. The passivation layer further functions as an anti-reflection layer and is specified to be preferably a PECVD deposited silicon nitride layer. However, the extension of the usually hard and rigid passivation layer of
30 typically nearly 100 nm thickness in the through-holes typically introduces stresses resulting from differential thermal expansion (and contraction) during and after heat treatments and in thermal cycling during use. Moreover, the process steps for forming the via cannot be isolated from the rest of the process.

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SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a process for manufacturing a solar cell wherein a selective emitter can be combined with conductors extending through the semiconductor substrate.

5 It is a further object to provide a solar cell having both a selective emitter and conductors extending through the substrate in combination with back contacts. Most suitably the semiconductor substrate has n-type conductivity.

This object is achieved in a method of manufacturing a solar
10 cell comprising the steps of:

- providing a semiconductor substrate having an opposed first and second side and comprising n-type charge carriers of a first conductivity type;
- providing through-holes in the substrate, extending from the
15 first side to the second side;
- applying a diffusion resistance layer of electrically insulating material onto the first side, and into the through-holes;
- patterning said diffusion resistance layer in accordance with
20 a predefined pattern of selective emitter regions to be applied into the semiconductor substrate;
- providing dopant species into the semiconductor substrate to form the selective emitter regions comprising p-type charge carriers;
- 25 - creating selective dopant diffusion regions through controlled diffusion of further dopant species through the diffusion resistance layer, the selective emitter regions and the diffusion regions jointly operating as emitter,
- applying conductive material on the selective emitter
30 regions, so as to form conductors from said selective emitter regions into said through-holes towards the second side of the semiconductor substrate, and
- providing back contacts on the second side of the semiconductor substrate, a first group of said back contacts being
35 coupled to said conductors, a second of said back contacts being

coupled to a field region present at the second side of the semiconductor substrate.

According to the invention, selective emitter regions are combined with dopant diffusion regions. By limiting the diffusion across the diffusion resistance layer, particularly to a diffusion rate at most equal to the diffusion in the semiconductor substrate, the creation of boron rich layers will be reduced to limited areas, i.e. the selective emitter regions. Additionally, the provision of highly doped, selective emitter regions leads to a reduction in contact resistance with any conductor to be applied thereon. The issue of boron-rich layers may furthermore be solved either by the application of the conductor, i.e. typically as a metal paste or by conversion of the boron rich layer into an oxide, for instance with a low-temperature oxidation step. Conductors are applied on the selective emitters, and at least substantially aligned therewith, and extend into the through-holes to form vias.

Particularly, the diffusion resistance layer furthermore acts as a diffusion barrier against metal diffusion. The metal in the through-hole forms part of the conductor (or via) provided through the substrate in one suitable embodiment with terminals at the second or rear side - e.g. a back-contacted solar cell.

Preferably, the thickness of the diffusion resistance layer is 1 to 30 nm, more preferably in the range of 2 to 20 nm, most preferably in the range of 3 to 10 nm. More specifically, the resulting dopant concentration in the selective emitter is preferably at least 10 times as high as in the selective dopant diffusion region. More preferably, this ratio of doping concentrations is at least 100.

The diffusion resistance layer is suitably chosen from at least one layer of silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide or other insulating material combinations, for instance comprising tantalum or titanium.. It is not excluded that a multilayer stack is used, such as a multilayer stack of silicon oxide, silicon nitride and silicon oxide (ONO). Preferably an

oxide is applied, and more preferably a high temperature oxide (HTO).

Most preferably, the diffusion resistance layer is applied, for instance, with Low -Pressure Chemical Vapour Deposition (LPCVD), Atomic Layer Deposition (ALD) and thermal oxidation in the form of Rapid Thermal Anneal (RTA), as known to the skilled person. Thin layers may be applied herewith in a suitable thicknesses and densities so as to optimize the diffusion rate of boron.

In accordance with a second aspect of the invention, a solar cell is provided that comprises a semiconductor substrate with a front or first and an opposed rear or second side and provided with n-type dopant species in a first concentration. At least one selective emitter region is defined adjacent to the front side and comprises p-type dopant species. A diffusion region comprising p-type dopant species surrounds said at least one selective emitter region, said diffusion region and said at least one selective emitter region jointly operating as an emitter. A field region is defined adjacent to the rear side and comprises n-type dopant species at a concentration higher than the first concentration, which emitter, substrate and field region together define a p-i-n diode. Vias are present extending through the substrate so as to connect first terminals to the selective emitter regions.

The device of the invention combines the presence of selective emitters in n-type substrates with an adequate protection of said substrates against metal diffusion out of the vias. As such, a device has been created, on the basis of the process of the invention, which combines a very good device performance with robustness and low contact resistances. For sake of clarity, the term 'via' is used herein to refer to an electrical conductor in a through-hole. The via is suitably a completely filled through-hole, although it is not excluded that voids could be left in the via due to limitations in the manufacturing process. The diffusion resistance layer is preferably present in the through-hole so as to avoid the generation of boron-rich silicon layers. While the diffusion

resistance layer on the front side of the substrate could be removed in an etching treatment, the diffusion resistance layer inside the through-hole is likely maintained.

Suitably, a diffusion resistance layer overlies the diffusion
5 region, at least on the first side and more preferably also along walls of any via extending from the first side to the second side. Such diffusion resistance layer is suitable to define the diffusion region in an appropriate concentration. It is however not excluded that the diffusion resistance layer is removed in an
10 etching step after the provision of the diffusion region into the substrate through the diffusion resistance layer. If removed, another adhesion layer is suitably applied.

Typically, the substrate is a monocrystalline semiconductor substrate. More suitably, a passivation layer, also operating as
15 an anti-reflection coating is present on the first side.

In a further embodiment, the field region is applied patternwise, such that a first portion destined for provision of the through-hole is kept outside the field region. This eliminates the need of the provision of a trench or groove or the like in a
20 separate step. Still, the walls of the through-hole and any extension of the emitter region applied thereto may and suitable will extend to the rear side of the substrate. This is deemed beneficial for improved robustness. Particularly an opened substrate surface such as a groove or trench may give rise to
25 contamination and/or to increased diffusion along the substrate surface. Such effects can only harm the device operation and lifetime.

Moreover, the extension of the through-hole from the front to the rear side of the substrate furthermore facilitates the
30 application of the conductor by means of electroplating or electroless deposition rather than by screenprinting a metal paste. Such replacement is for instance beneficial in order to lower alignment tolerance between the definition of (selective) emitter regions and conductors. When applying said conductors by
35 means of electroplating it is most suitable that the metal paste is replaced completely rather than merely in the through-holes,

i.e. for the definition of conductors on the front side, on the rear side and in the through-holes. The filling of through-holes by means of electroplating may be achieved for instance by a bridge process, but alternatively by coating or printing a conductor in the through-hole, so as to coat the through-hole wall. Examples of printable conductor materials suitable as a plating base include conductive polymers, such as polyethylenedioxythiophene (PEDOT), conductive epoxies, silver, for instance in the form of nanoparticles and the like. PEDOT is for instance commercially available as an aqueous dispersion, mixed with polystyrene sulfonic acid. This aqueous composition excellently wets an oxide or nitride surface. In an electroplating bridge process a distance between two electroplated portions is bridged. The two portions of the through-holes are typically the front and rear side. Bridge formation may be supported by bridge formation means, for instance the temporary provision of an electrode within the through-hole so as to provide a local voltage difference adequate for the electroplating process.

Applying conductors on the front side by means of electroplating is particularly suitable in combination with the definition of selective emitter regions. It may be suitable to apply an intermediate adhesion layer on the selective emitter regions. Such adhesion layer may be beneficial for reduction of contact resistance and the prevention of any undesired contamination. Examples of such materials are for instance polysilicon, titanium nitride, tungsten, tungsten nitride, titanium tungsten nitride, silver, aluminum and any alloys therewith.

According to a further aspect of the invention, a method of manufacturing a solar cell is provided, comprising the steps of:

providing a semiconductor substrate having an opposed first and second side and comprising n-type charge carriers;

providing dopant species into the semiconductor substrate to form the emitter regions comprising p-type charge carriers;

providing through-holes into the semiconductor substrate, extending from the first side towards or to the second side;

providing conductors extending from said emitter regions to the second side of the semiconductor substrate through the through-holes comprising the step of electroplating said conductors in said through-holes.

5 According to again a further aspect of the invention, a solar cell is provided comprising a semiconductor substrate with a first side and an opposed second side, which semiconductor substrate is provided with n-type dopant species in a first concentration; an emitter region present adjacent to the first side and comprising
10 p-type dopant species; a field region present adjacent to the second side and comprising n-type dopant species at a concentration higher than the first concentration, which emitter, substrate and field region together constituting a p-i-n diode; and a via extending from the first side to the second side
15 of the semiconductor substrate and coupled on the first side of the substrate to the emitter region and on the second side to a back contact, and comprising electroplated metal.

In accordance with these aspects of the invention, a method of electroplating the vias is provided, as well as a solar cell
20 comprising the resulting vias. It has been observed by the inventors that several features, particularly when applied in combination may be used to replace the commonly used screenprinting by electroplating. Such replacement allows to reduce the size of the vias substantially, for instance with 50%
25 or more, preferably with 75% or more. Therewith the diameter of the via may be reduced to less than 100 microns, preferably less than 50 microns, more preferably less than 25 microns. This immediately leads to an increase in available surface area and thus to an increase of efficiency.

30 A first feature enabling electroplating are particularly the provision of selective emitter regions exposed on the first side. These can be used as an initial plating base. The term 'initial plating base' is used to express that the selective emitter regions could be the plating base themselves or one or more
35 intermediate conductive layers applied on the exposed selective emitters could be used as plating base. A second feature enabling

the use of the electroplating is the provision of the patterned field region. This prevents the need for applying an additional trench from the second side, As a result thereof, the via is substantially straight, and the risk of short-circuitry on the second side as a consequence of the electroplating process is reduced. A further feature of the invention is the provision of an appropriate barrier layer in the through-hole, which is for instance the diffusion resistance layer.

In accordance with a further aspect of the invention, a method of manufacturing a solar cell is provided comprising the steps of:

- Providing a semiconductor substrate having a first and an opposed second side and a plurality of through-holes extending from the first side to the second side, which semiconductor substrate is provided with an emitter region and with a field region, which field region comprises charge carriers of a first conductivity type and is defined adjacent to the second side, which emitter region comprises charge carriers of a second conductivity type, opposed to the first conductivity type, and is defined adjacent to the first side;
- Applying a barrier layer onto the first side and into the through-holes;
- Applying an anti-reflective coating onto the barrier layer on the first side of the substrate;
- Applying conductive material into the through-holes so as to form vias, wherein the barrier layer is a diffusion resistance layer preventing acid-catalysed diffusion of metal during via formation into the semiconductor substrate.

Furthermore, in accordance with the invention, a solar cell is provided comprising a semiconductor substrate having a first and an opposed second side and a plurality of vias extending from the first side to the second side, which semiconductor substrate is provided with an emitter region and with a field region, which field region comprises charge carriers of a first conductivity type and is defined adjacent to the second side, which emitter

region comprises charge carriers of a second conductivity type, opposed to the first conductivity type, and is defined adjacent to the first side, which vias comprise conductive material in a through-hole for electrically coupling the emitter region to first terminals on the second side of the semiconductor substrate, at least one second terminal being electrically coupled to the field region. Herein a barrier layer is present on the first side of the semiconductor substrate and in the through-holes, said barrier layer being a diffusion resistance layer acting as a diffusion barrier against acid-catalyzed diffusion of metal into the semiconductor substrate during via formation and acting as an adhesion layer on the first side of the semiconductor substrate for an anti-reflective coating present thereon.

In accordance with the invention, a diffusion resistance layer is provided prior to deposition of the antireflection coating. The diffusion resistance layer effectively fulfills the functions of adhesive layer for the antireflection coating and of diffusion barrier for the prevention of acid-catalysed diffusion of metal into the semiconductor substrate during via formation.

While the diffusion resistance layer extends both on the first side and into the vias, the antireflection coating is merely providing onto the first side of the substrate. This difference is achieved, particularly, in that different deposition processes are used for the diffusion barrier layer and the antireflection layer.

Most suitably, the barrier layer is an electrically insulating layer, which further contributes to the prevention of shunting.

The present invention is based on the insight that a barrier layer needs to be deposited such as to be suitable for use within a through-hole needs to be stable under acid-catalysed conditions, particularly in the presence of acid in a solvent. Thereto, both the material and the deposition conditions have an impact.

Most suitably, the barrier layer (i.e. the diffusion resistance layer) has a thickness of at least 2 nm, more preferably of at least 3 nm, or even of at least 5 nm. Preferably,

the thickness is at most 25 nm, more preferably at most 15 nm and more preferably 10 nm.

Suitably, the diffusion resistance layer is a conformal barrier layer. As a conformal layer, the barrier layer suitably is characterized in a very good step coverage and a small thickness variation. The step coverage is suitably at least 95%, more preferably at least 98% and even more preferably 99.5% or even closer to the absolute limit of 100% step coverage. Particularly inside the through-hole a step coverage of virtually 100% is desired. The thickness variation on the first side of the semiconductor substrate and inside the through-holes of at most 50%, more preferably at most 25% and even more preferably at most 15%. It is not excluded that there is a difference in thickness of the barrier layer on the first side of the semiconductor substrate and in the through-holes. Preferably, this thickness difference is however limited to 100%, more preferably 50%, more preferably 30% of the thinnest layer.

Most preferably, the barrier layer is deposited with atomic layer deposition. This technique has been found to provide a dense and well-ordered layer that meets the requirements of functioning as a barrier layer. It can moreover be deposited with a very high step coverage up to 100% and not merely on planar surfaces but also in trenches and through-holes with a high aspect ratio. In accordance with the present invention, the aspect ratio of the through-holes is suitably between 5 and 50, preferably between 10 and 25.

A wide variety of materials is available for deposition as a barrier layer, for instance hafnium oxide, silicon oxide, silicon nitride. Multilayers, for instance stacks of silicon oxide and silicon nitride, including ONO, NO, NON, ON, ONONO stacks may be applied alternatively. Suitably, the materials used as a barrier layer are free of metals suitable as a dopant of the semiconductor substrate. Thereto, aluminum oxide is deemed not appropriate. One additional advantage of the use of a conformal barrier layer is that any texture defined on the first side is not flattened off. Furthermore, any subsequent antireflection coating can be deposited on a smooth surface, which likely leads to an optimal

deposition process and hence, a homogeneous layer. Such resulting antireflection coating with a low thickness variation has a beneficial effect on the transmission of radiation into the substrate.

5 In one embodiment, the barrier layer is deposited prior to doping the semiconductor substrate for creation of the emitter region. The barrier then serves the function as a diffusion resistance layer. Suitably, the emitter region is formed by diffusion of a boron dopant at a high temperature of for instance 700-1100°C,
10 preferably between 900-1000°C. Both in view of the high temperature and the small size of the boron atom, it is possible that a barrier layer against acid-catalysed diffusion may further act as a diffusion resistance layer that enables controlled diffusion.

15 Suitably, the barrier layer is selected such that the dopant species of the second conductivity type (i.e. boron) will diffuse through the barrier layer at a diffusion rate that is at most substantially equal to a diffusion rate of the said dopant species of the second conductivity in the semiconductor substrate. It is
20 herein not excluded that the boron diffusion may be in the form of diffusion of boron oxide.

In a further embodiment, the barrier layer is defined as a passivation layer, separately or as a combination with a further layer. This has the advantage that there is a larger design
25 freedom in choosing the antireflection coating. Examples include an antireflection coating comprising nanorods; an antireflection coating comprising a first and a second sublayer, for instance of oxide and nitride; a layer stack of different materials, a layer comprising a core-shell structure such as known from WO2009/050639
30 and WO2010/018490, for instance of titanium oxide and titanium nitride particles.

In one embodiment, the conductive material is applied as a metal paste composition. Such metal paste composition comprises rheology aids, anti-oxidants, a solvent, and an organic acid as a
35 basis of the flux. Typically use is made of rosin as the organic acid on which the flux is based. An activator responsible for

attacking metal surfaces resulting in cleaning is typically present but could be left out or be present in minor amounts ("Low activity"). The flux is responsible for removal of underlying passivation layers and the prevention of oxidation of the metal, so as to ensure that a proper low-resistive contact is formed. In order to protect the barrier layer inside the through-hole, the metal paste composition used for filling the through-hole preferably is chosen to be a metal paste composition with a low acid value, for instance lower than 150 and preferably lower than 130. The acid value is related to the organic acid and corresponds to the KOH mg equivalent. The acid value is determined using a simple KOH titration. One suitable metal paste is for instance a low activity silver paste sold by Heraeus under the tradename HeraSol SOL 109.

In an alternative embodiment, the conductive material is applied by means of electroplating or electroless deposition rather than by screen printing a metal paste. Such replacement is for instance beneficial in order to lower alignment tolerance between the definition of (selective) emitters and conductors.

It will be understood that any features discussed hereabove in relation to one aspect and/or illustrated in the figure description may be combined with other aspects as discussed, unless clearly contradictory.

BRIEF INTRODUCTION OF THE FIGURES

These and other aspects of the invention will be further elucidated with reference to the figures in which:

Fig 1-6 are diagrammatical, cross-sectional views of consecutive steps in a first embodiment of the method of the invention;

Fig. 7 is a diagrammatical top view on the first side of the solar cell;

Fig. 8 is an enlarged view of a portion of Fig. 7;

Fig. 9-13 are diagrammatical, cross sectional views of consecutive steps in a second embodiment of the method of the invention;

Fig. 14 is an enlarged view of Fig. 5.

DETAILED DESCRIPTION OF ILLUSTRATED EMBODIMENTS

The Figures are not drawn to scale and merely intended for illustrative purposes. Equal reference numerals in different figures refer to like or equal parts.

Fig 1-5 show in cross-sectional, diagrammatical view several stages of the method of the invention, resulting in the device shown in Fig. 6. Fig. 14 discloses another diagrammatical view corresponding to Fig. 5, which more precisely shows the layer sequences of the boron diffusion region 31, the diffusion resistance layer 22A, 22B on the first side 11 and extending into the through-hole 20, as well as a subsequently applied antireflection coating 32A, 32B on the first or front side 11 and the second or rear side 12.

As a first step, Fig. 1 shows a semiconductor substrate 10 with a front side 11 and a rear side 12. The front side is the side that is intended for receiving irradiation during use; the solar cell will be assembled on its rear side 12 to a carrier. It typically has been texturized in advance of doping processes. The semiconductor substrate 10 of this example is a mono-crystalline silicon substrate. While silicon substrates constitute the best available compromise between manufacturing costs and quality, it is not excluded that alternative substrates are used. Such alternative substrates could be made of III-V materials, but more likely incorporate one or more layers of a different material, such as a III-V material, or SiGe, SiC and the like as known to the skilled person. The semiconductor substrate is doped with a dopant of the first conductivity type, which is in the preferred example n-type. The doping concentration is moderate, for instance $10^{16} / \text{cm}^3$. The semiconductor substrate 10 is provided at both the front side 11 and the rear side 12 with a region of n+-doped material. Suitably, use is made of phosphorous doping in a manner known to the skilled person, for instance by vapor deposition. In one embodiment, the phosphorous doping is applied on the rear side 12 only, so as to define region 13B. The front side 11 is therein blocked from diffusion, for instance with a back-to-back

arrangement of substrates 10. According to another embodiment, the phosphorous doping is diffused into the regions 13A, 13B of the substrate 10 by a heat treatment of approximately 850°C for 5-50 minutes in an atmosphere containing O₂ and P₂O₅ vapour. This results in the formation of a silicon oxide film (not shown) which incorporates P₂O₅. At the interface the substrate and the silicon oxide film, the P₂O₅ is reduced to elemental phosphorous, which diffuses into said regions 13A, 13B. Subsequently, the silicon oxide film is removed by dipping the substrate in a 1-50% HF solution for about 0.5-10 minutes, or exposing the substrate to a HF vapour.

Fig.2 shows the substrate 10 in a second stage, after an etching treatment. Herein, the region 13A at the front side 11 is removed by etching, for instance using a mixed solution of 1-30% HF and 0.1-50% HNO₃. This result in a substrate 10 that has been doped at its rear side 12 with a dopant species of the first conductivity type to define at least one field region 13B. Moreover, a plurality of trenches 35 are etched at the rear side 12 of the substrate 10 located where thereafter through holes 20 will be created, or through-holes 20 have been created. The trenches 35 are typically in the order of 1 - 7 mm in width, while the depth is conveniently chosen such that the doped region 13B at the rear side 12 (back-surface field) is obstructed by etching away typically 0.4 - 2 micron of silicon. These trenches 35 can also be etched near the edge of the substrate 10. Moreover, a through-hole 20 is provided into the semiconductor substrate 10, within the boundaries of the trench region 35, and extends from the front side 11 to the rear side 12 thereof. Typically, a plurality of through-holes 20 is applied in a single solar cell, so as to reduce a lateral distance over which generated current has to be transported to a terminal. The through-holes are typically applied by laser etching, although other forms of etching, such as reactive ion etching or a combination of reactive ion etching and wet-etching are not excluded. While the through-hole 20 is shown to be straight, it is not excluded that the through-hole 20 is further modified to have a varying diameter, or

that any sharp edges at its top and bottom side, i.e. on the front side 11 and the rear side 12 are removed. The diameter of the through-hole is typically in the order of 5-300 microns.

Fig. 3 shows the substrate 10 in a third stage, after
5 application of a diffusion resistance layer 22. The diffusion resistance layer 22 is suitably applied by chemical vapour deposition or thermal oxidation, and more preferably by low pressure chemical vapour deposition (LPCVD), atomic layer deposition (ALD) or a rapid thermal anneal (RTA). Such state of
10 the art techniques can be applied to provide a diffusion resistance layer of good thickness uniformity which covers the substrate sides. The diffusion resistance layer suitably comprises an inorganic material such as an oxide or a nitride of silicon, titanium, tantalum, mixtures thereof, combinations thereof (a
15 sublayer of SiO_2 , and a sublayer of SiN). Use of an oxide layer, particularly a silicon oxide film, is preferred, as it allows diffusion of boron into the semiconductor substrate 10 at a reduced rate. The exact composition as well as density of the diffusion resistance layer may be varied by tuning of the
20 composition of the gas.

In the present embodiment, the diffusion resistance layer 22 is particularly intended so as to prevent a boron rich layer that is believed to be responsive for fast carrier lifetime degradation in the bulk of the substrate 10. The diffusion resistance layer is
25 further intended to create selective emitter regions. However, it is not excluded, and it may even be advantageous, that outside the selective emitter regions p+ material is present but in a lower dopant concentration, particularly resulting from diffusion through the diffusion resistance layer. The diffusion resistance
30 layer 22 may have a relatively low thickness, for instance in the order of 0.5-5 nm.

It is not excluded that the diffusion resistance layer is applied with an alternative technique, such as a low temperature oxide, for instance a Plasma enhanced chemical vapour deposition
35 (PECVD). Upon providing a boron oxide - in situ converted from a boron source such as boron tribromide (BBr_3) - the boron oxide

then tends to be absorbed, at least partially, in the low temperature oxide, resulting in a boron silicate glass. Reduction of the boron diffusion may then be achieved by operating in an atmosphere substantially free of hydrogen, and more particularly in an inert atmosphere such as nitrogen (N₂) or argon.

As shown in Fig. 3, the diffusion resistance layer 22 of this embodiment extends both on the front side 11, the rear side 12 and on walls of the through-holes 20. This is the consequence of application thereof in a chemical vapour deposition step without blocking of any of the sides to prevent the application of the barrier layer 22. However, that is not deemed necessary. For instance, either the front side 11 or the rear side 12 may be blocked from deposition of the chemical vapour, particularly in a back-to-back arrangement of the semiconductor substrates 10. It is even possible, in line therewith, to apply a stacked arrangement such that both the front side 11 and the rear side 12 of the stacked substrates 10 will not be exposed. This provides freedom to deposit alternative layers on the front side than in the through-hole. For instance, the through-hole 20 may contain a nitrogen-containing diffusion resistance layer 22, while the front side 11 is provided with a high temperature oxide layer as diffusion resistance layer 22A allowing boron diffusion at a reduced rate. The diffusion resistance layer 22A is then subsequently opened in accordance with a predefined pattern so as to create apertures 25.

The provision of such pattern is suitably carried out with photolithography, typically by using a mask, as known to the skilled person. In the present domain of solar cells, high resolution patterning such as known from integrated circuit manufacturing is however not required. A more simplistic solution as the screenprinting of a local mask around an aperture area, and thereafter providing an etchant liquid in the thus created, screenprinted basin, is not excluded. Such a mask is suitably removed again prior to the subsequent high temperature doping step. Alternatively, one could use a screen printing slurry or an inkjet printing slurry, which includes an etchant in itself. One

particularly preferred embodiment, is the use of a screenprinting slurry or paste based on a borate acid etchant. This enables to etch the diffusion resistance layer 22A and to provide doping into the semiconductor substrate 10 in a single step.

5 It is herein not evident that any material apparently suitable as a barrier layer may be applied. The microstructure and properties of many materials, and particularly electrically insulating materials, turns out to depend on the deposition and/or growth process. This is for instance known for silicon oxide, one
10 of the most widely applied insulating materials in semiconductor processing. Silicon oxide is typically present as an amorphous layer, with inherent voids or channels or contamination resulting from the deposition process. A thermal oxide has properties different from a chemical oxide, both in terms of structural order
15 and surface smoothness. Therefore, the ability of a material for formation of an adequate diffusion barrier typically depends on the deposition process. In accordance with the invention, the diffusion barrier is chosen to act as a barrier against acid-catalysed diffusion in via formation. Suitable manners of
20 formation of a via include filling, at least partially, of through-holes with screenprinting metal paste, or electroplating. In both cases, the via formation occurs in the presence of a solvent and an acid; screenprinting of metal paste typically uses an alcohol as a solvent, such as butyl carbitol, dibutyl carbitol,
25 glycol and polyhydroxy alkphatic and aryl alcohols. Electroplating preferably uses water as a solvent. Acids are present therein; in the case of a metal paste, rosin is suitably used, which comprises abietic acid and pimaric acid. For electroplating, sulfuric acid is typically present. In order to act as a diffusion barrier in
30 acid-catalysed metal diffusion, the barrier layer is suitably grown or deposited rather than being formed wet-chemically. In view of its application after the heat treatments for diffusion of dopant, a certain temperature limitation exists. Even though some further dopant diffusion is not detrimental, a treatment above
35 1000 °C will induce major changes in an uncontrollable manner. Moreover, the complete surface area of the through-hole needs to

be covered. Suitably, the barrier layer comprises a silicon based material wherein the Si/O ratio is smaller than 0.75, preferably smaller than 0.7, more preferably smaller than 0.6 and optimally in the order of 0.5. Such material has a low-hydrogen content that is deemed suitable for its performance as a diffusion barrier.

In this example as shown, the barrier layer is a conformal barrier layer. The conformal barrier layer is applied in a structure with a high aspect ratio. Physical vapor deposition methods, such as evaporation and sputtering, have limited abilities to coat structures with high aspect ratios and thus are not suitable for the invention. Wet chemical methods are applied onto the surface. However, their resulting thickness is limited, typically to 1 or 1.5 nm. This may be suitable as a thin oxidation layer for adhesion purposes, but is insufficient as a barrier layer, particularly taking into account that wet chemical oxides are not dense. Conformal CVD reactions must have their slowest, rate-limiting steps on the surface of the growing film, rather than in the gas phase. Particularly high aspect ratios can be coated conformally by a CVD method in which two complementary reactant vapors are supplied to a surface in alternate pulses. In this way, their reactions are forced to be entirely on the surface. This method is known as Atomic Layer Deposition (ALD). The barrier layers provided with ALD turn out to be conformal, have a good thickness uniformity and a low leakage current when applying an electric field. Moreover, the silicon to oxygen ratio of ALD layers may be tuned to a ratio of nearly 0.5, for instance by application of additional oxygen/ozon or on the basis of ammonia catalysed hydrolysis of tetraethoxysilane (TEOS).

In a further embodiment, use is made of a double layer process, comprising a first layer of silicon oxide, wherein the ratio between silicon and oxide is below 0.75, preferably below 0.6 and most suitably around 0.5, and a second layer comprising a moisture barrier. A suitable moisture barrier is for instance a silicon rich layer, wherein the ratio between silicon and oxide is higher than in the first layer. Alternatively, use can be made of silicon nitride

In one embodiment, use is made of a remote plasma atomic layer deposition process using an O₂ plasma. Use is made of a FlexAL apparatus of Oxford Instruments. A constant 60 sscm O₂ flow and pressure of 15mTorr are maintained in the reactor. The silicon precursor is injected into the reactor by fast (20 ms open-close) ALD valves. A 400W inductively coupled O₂ plasma is used for oxidation. The total ALD cycle time, including pump and purge steps, is 4s. The reactor wall is kept at a constant temperature of 120°C and the precursor lines are kept at 50°C. An increase in the deposition temperature results in a reduction of layer thickness with constant number of cycles. A deposition temperature of at least 200°C appears suitable, so as to minimize the incorporation of hydrogen into the layer. This improves the quality of the barrier. Preferably, the amount of hydrogen in the layer is less than 10 at%, preferably less than 5at%. The number of ALD cycles is suitably less than 300, for instance 100-200.

In a further embodiment, use is made of a batch ALD reactor for deposition of silicon oxide and silicon nitride. A gas anneal was formed at 400°C in an inert argon atmosphere with 3% H₂. Silicon oxide was deposited using Si₂Cl₆ and O₃/O₂ as precursor gas. Deposition temperatures were varied between 300 and 400°C, leading to a growth rate in the range of 0.1-0.5 nm per cycle. Silicon nitride was deposited from SiH₂Cl₂ and NH₃ as precursor gases. Deposition temperatures in the range of 400-500°C were used, with a growth rate in the order of 0.05-0.1 nm per cycle. With both experiments, leakage currents of less than 10⁻⁸ (A/cm²) at an electric field of 3MV/cm were observed. This further holds for O-N-O multilayers.

Fig. 4 shows the substrate 10 in a fourth stage, after the provision of the doping species of a second type, in this case p+ type. The Boron diffusion source may be a vapour source or a coating source. In the oven the substrate is heated for a certain period of time and to a certain temperature so as to diffuse Boron into the front side of the substrate 10, and create selective emitter regions 30, and around those diffusion regions 31 of a lower concentration. While the present figures show the selective

emitter regions 30 and the diffusion regions 31 are separate regions, it will be understood that these are portion of a continuous emitter. Simultaneously, the phosphorous doping at the rear side 12 of the substrate 10 is diffused as well, so as to create a double-diffused field region 33. The trench 35 provided in an earlier stage is now separating the double diffused region 33 from the boron doped region 31 in the through-hole 20, thereby preventing any short-circuit between the double-diffused field region 33 and the conductor to be provided in the through-hole 20. Successful results have been obtained with a Boron vapour source for the diffusion. Two substrates are put back-to-back into the oven and heated at 900-1000°C for 30-120 minutes, for instance at 950°C for 1 hours in an atmosphere including an O₂ and boron oxide (B₂O₃) vapor. As explained above, this B₂O₃ vapor is typically in situ created from a Boron tribromide (BBr₃) vapour in the presence of oxygen. The boron oxide vapour reacts with the silicon surface to create elemental boron and silicon oxide. The elemental boron then diffuses into the silicon substrate.

The silicon oxide is typically contaminated with boron oxide, resulting in a borosilicate glass. After the termination of the diffusion treatment, the borosilicate glass is suitably removed. The removal of the borosilicate glass may be effected either with an acid such as HF that will also remove at least part of the diffusion resistance layer 22A. Alternatively, use can be made of hot water or any other known etchant which allows selective etching of the borosilicate glass. In the event that a boron-rich layer develops in the selective emitter regions 30, it will be present directly at the substrate surface, in a thickness of typically at most 20 nm. An oxidation step may then be carried out to oxidize the silicon rich layer and a thin silicon layer below it. The oxidation step will further create a new oxide on the front side 11 outside the selective emitter regions 30, if the diffusion resistance layer 22A has been removed completely. It has turned that out, when applying conductors with screenprinting techniques, these oxides need not to be removed separately.

In order to separate the emitter region 30 and the field region, a trench 35 may be applied in the through-hole 20 from the second side 12 of the substrate 10, as shown in Fig. 14. This trench is suitably provided prior to the doping with boron and the subsequent diffusion step. The extension of the field region 13B is then still most restricted, which simplifies the removal.

Fig. 5, as well as Fig. 14, shows the substrate 10 in a fifth stage, after the application of a passivation layer 32A, 32B on both the front side 11 and the rear side 12. The passivation layer suitably comprises SiN, as known to the skilled person, but alternative materials are by no means excluded. It goes without saying that the passivation layers 32A, 32B could be applied in separate steps and then do not need to have identical composition. The passivation layer 32A, 32B may be applied as well in the through-hole 20, on top of the diffusion resistance layer 22. Suitably, the process is tuned so as to achieve higher growth rates on the front side 11 and/or on the rear side 12 than in the through-hole 20. Instead of growing the passivation layer 32A, 32B into the through-hole, a separate barrier layer could be applied.

Instead of applying a nitride passivation layer, stacks of amorphous silicon layers may be deposited on the front side 11 and optionally on the rear side 12. These amorphous silicon layers are suitably deposited by Plasma enhanced chemical vapour deposition (PECVD), for instance in a parallel plate plasma deposition driven by a 13.5 MHz power source, or in an inductively coupled plasma PECVD set up. The thickness of amorphous silicon layers is suitably 20 nm or less, more preferably 10 nm or less. The stacks comprise an intrinsic layer and a p-doped layer on the front side 11, and an intrinsic layer and a n-doped layer at the rear side 12. It has turned out that such amorphous silicon layers not only act as passivation layers, but also result in silicon heterojunction solar cells.

Fig. 6 shows the resulting solar cell 100, after application of conductors 40, 41 and of terminals 51, 52. The conductors include a via 40, i.e. the filled through-silicon through-hole and the conductor 41 on the front side 11. The conductor 41 on the

front side 11 suitably comprises silver, the via 40 for instance comprises a silver/aluminum alloy or silver. Such type of conductors are typically applied using a metal paste by screenprinting in a process known in the art, as deemed most beneficial from a cost perspective. The screenprinting paste applied on the front side 11 is typically an acid-containing screenprinted paste that is able, upon heating, to etch away underlying layers, i.e. portions of the passivation layer 32A and the diffusion resistance layer 22. The screenprinting paste applied in the via 40 is suitably free of acid, so as to ensure that the diffusion resistance layer 22 and any optionally applied barrier layer is not removed. However, alternative manufacturing processes as known in the art are not excluded from the scope of the present invention. The present solar cell device 100 is provided with first terminals 51 and second terminals 52. It is observed that typically a plurality of both the first terminals 51 and the second terminals 52 are present on the rear side 12 of the substrate 10, and that both are substantially dot-shaped. Suitably, the processing is carried out such that both terminals are applied in a single process step. Therefore, most suitably, the via 40 extends to the same level as the substrate 10.

Fig. 7 and Fig. 8 show top views of the resulting solar cell 100. Fig. 8 shows herein a detail of Fig. 7. An array of conductors 41 is provided that are connected to the underlying selective emitter regions 30. The conductor 41 suitably extends by several tens of microns outside the perimeter of the via 40. The selective emitter regions 30 are in the form of straight lines at mutually equal distances. The conductors 41 extend along and over the selective emitter regions 30. This is deemed beneficial so as to have minimum resistance. It is however not excluded that the conductors 41 only partly extend or merely extend over a portion of the selective emitter regions 30.

Fig. 9-13 show consecutive steps of a second embodiment of the method of the invention in cross-sectional diagrammatical views. With respect to the choice of layers, and specific process steps, this second embodiment preferably uses the materials and

processes specified as preferred in the first embodiment, such as a typically moderately n-type doped monocrystalline silicon substrate 10, use of phosphorous doping for instance by vapour deposition, etc. These materials and processes will not be repeated in detail hereinafter.

As a first step, Fig. 9 shows a semiconductor substrate 10 with a front side 11 and a rear side 12. The semiconductor substrate 10 is provided at the rear side 12 with a region 13 of n+-doped material. In accordance with the present embodiment, the n+-doped region 13 is applied according to a predefined pattern. It is moreover merely present at the rear side 12 and not at the front side 11. The predefined pattern may be provided for instance by applying a suitable mask in advance of the doping step, or by provision of a solid phase dopant that is applied in accordance with a pattern by screenprinting or inkjetprinting, or patterned, for instance in an etching treatment, after deposition of the dopant. One suitable implementation is deposition of an oxide SiO₂ layer of typically 40-150nm by means of inkjet. This oxide will be masking the areas near the through-hole and the wafer edge.

Subsequently phosphorus is diffused into the substrate at the locations the mask is not present..Hereafter the phosphorus oxide layer is etched (PSG etch) and subsequently a stacked layer 15 of oxide and nitride is deposited on the back-side 12 of the substrate. The thickness of the oxide and nitride stack is typically between respectively 50-200nm and 5-30nm. Then an alkaline texturization etch is performed, which typically etches 5-15nm from the front side 11 of the substrate. Also the edges of the wafer are etched, removing any unwanted phosphorus doping at the edges. The oxide/nitride layer stack on the back-side blocks the texturization from etching the back-side 12. .

Fig. 10 shows the substrate 10 in a second stage in the processing, after provision of a through-hole 20 and the provision of a diffusion barrier 22. The through-hole 20 is provided into the semiconductor substrate 10, and extends from the front side 11 to the rear side 12 thereof. Typically, a plurality of through-holes 20 is applied in a single solar cell, so as to reduce a

lateral distance over which generated current has to be transported to a terminal. The diffusion barrier 22 extends in this example on the front side 11 and in the through-hole 20. It is patterned so as to define an aperture 25. A suitable etchant
5 for the diffusion barrier 22 may be applied by screenprinting, ink-jet printing. Laser etching may be used alternatively.

Fig. 11 shows the substrate 10 in a third stage, after application of p-type dopant so as to define the highly doped selective emitter 30 and the diffusion region 31. Moreover, in the
10 heat treatment for diffusion of the p-type dopant, the n-type dopant on the second side is simultaneously further diffused to constitute a field region 33. The distance between the field region 33 and the diffusion region 31 extending along a wall in the through-hole 20 is chosen in accordance with a design rule so
15 as to prevent short-circuitry. This design rule is determined by the difference between the through-hole diameter typically between 5 - 300 micron, while the oxide mask around the through hole typically has a diameter of between 1 and 7 mm.

Fig. 12 shows the application of an antireflective coating
20 layer of oxide and/or silicon nitride 32A at the front side 11.

Fig.13 shows the resulting solar cell 100, obtained by the provision of conductive material to define conductors 40, 41 and terminals 51, 52. The via metal paste composition is chosen such that it will not form a contact to the side walls of the via 40 in
25 the subsequent firing through step. Metal 41 and 52 are contacting respectively the emitter 31 and base regions 33 after firing through the anti-reflective layer 32A and back-side protection layer 15. Terminal 51 is connecting via to the emitter to the front side selective emitters 30.. The conductors include a via
30 40, i.e. the filled through-silicon through-hole and the conductor 41 on the front side 11. The first terminals 51 and second terminals 52, are defined in one screen or stencil printing step. It is observed that typically a plurality of both the first terminals 51 and the second terminals 52 are present on the rear
35 side 12 of the substrate 10, and that both are substantially dot-shaped. Suitably, the processing is carried out such that both

terminals are applied in a single process step. Therefore, most suitably, the via 40 extends to the same level as the substrate 10.

Claims

1. A method of manufacturing a solar cell, comprising the steps of:

- 5 - providing a semiconductor substrate having an opposed first and second side and comprising n-type charge carriers;
- providing through-holes into the semiconductor substrate, extending from the first side towards or to the second side;
- 10 - applying a diffusion resistance layer of electrically insulating material into the through-holes and onto the first side in accordance with a predefined pattern of selective emitter regions to be applied into the semiconductor substrate;
- 15 - providing dopant species into the semiconductor substrate to form the selective emitter regions comprising p-type charge carriers;
- creating dopant diffusion regions through controlled diffusion of further dopant species through the diffusion resistance layer, the selective emitter regions and the 20 diffusion regions jointly operating as emitter;
- applying conductive material on the selective emitter regions, so as to form conductors from said selective emitter regions into said through-holes towards the second side of the semiconductor substrate, and
- 25 - providing back contacts on the second side of the semiconductor substrate, a first group of said back contacts being coupled to said conductors, a second of said back contacts being coupled to a field region present at the second side of the semiconductor substrate.
- 30 .

2. The method as claimed in claim 1, wherein the diffusion barrier layer acts as a diffusion barrier against metal diffusion.

3. The method as claimed in Claim 1, wherein the predefined 35 pattern of selective emitter regions is completely defined on

the first side on the substrate without extending into the through-holes.

4. The method as claimed in Claim 1, wherein the diffusion resistance layer is patterned together with the provision of
5 dopant species in a single step.

5. The method as claimed in Claim 1 or 4, wherein the step of patterning the diffusion resistance layer occurs with a printing process.

6. The method as claimed in any of the previous claims, wherein
10 the thickness of the diffusion resistance layer is in the range of 1 to 30 nm, when measured on the first side of the semiconductor substrate.

7. The method as claimed in any of the previous claims, wherein the diffusion resistance layer is a high temperature oxide.

15 8. The method as claimed in claim 7, wherein the high temperature oxide is provided by low-pressure chemical vapour deposition, atomic layer deposition or a thermal oxidation in a rapid thermal anneal treatment.

9. The method as claimed in claim 5 or 6, wherein a boron rich
20 silicon layer formed in the selective emitter region is decomposed by a low temperature oxidation step.

10. The method as claimed in any of the preceding Claims, wherein the application of conductive material comprises the step of electroplating both on the first side and into the through-
25 holes.

11. A solar cell comprising a semiconductor substrate with a first side and an opposed second side, which semiconductor substrate is provided with:

- n-type dopant species in a first concentration,
- 30 - At least one selective emitter region present adjacent to the first side and comprising p-type dopant species;
- A diffusion region comprising p-type dopant species surrounding said at least one selective emitter region, said diffusion region and said at least one selective emitter
35 region jointly operating as an emitter,

- vias of conductive material through the semiconductor substrate, said vias having walls being provided with a diffusion resistance layer, and optionally a barrier layer, said conductive material extending on top of the selective emitter regions, and;

- A field region present adjacent to the second side and comprising n-type dopant species at a concentration higher than the first concentration, which emitter, substrate and field region together constituting a p-i-n diode.

12. The solar cell as claimed in Claim 11, wherein the selective emitter region has a dopant concentration of at least tenfold of dopant concentration in the diffusion region.

13. The solar cell as claimed in Claim 11 or 12, wherein the diffusion region underlies a diffusion resistance layer.

14. The solar cell as claimed in Claim 11 or 13, further comprising

15. A solar panel comprising at least one solar cell as claimed in Claim 12 and a panel carrier, in which at least some of the back contacts of the solar cell are coupled to conductors in the solar panel.

16. A method of manufacturing a solar cell, comprising the steps of:

- providing a semiconductor substrate having an opposed first and second side and comprising n-type charge carriers;

- providing dopant species into the semiconductor substrate to form the emitter regions comprising p-type charge carriers;

- providing through-holes into the semiconductor substrate, extending from the first side towards or to the second side;

- providing conductors extending from said emitter regions to the second side of the semiconductor substrate through the through-holes comprising the step of electroplating said conductors in said through-holes.

17. The method as claimed in Claim 16, wherein said emitter regions comprise selective emitter regions exposed to a first side of the substrate and acting as an initial plating base for electroplating said conductors.

18. The method as claimed in Claim 17, wherein an intermediate electrically conductive layer is applied on the selective emitters and extending laterally to said through-holes.

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19. The method as claimed in any of the Claims 16 to 18, wherein a conductive coating is applied to inner walls of said through-holes prior to the electroplating process.

10 20. The method as claimed in Claim 19, wherein the conductive coating is applied in a fluid form, for instance by printing or spraying

15 21. The method as claimed in Claim 16, further comprising the step of applying a field region adjacent to the second side of the substrate according to predefined pattern, so that a first substrate portion in which a first through-hole is to be formed is kept outside the field region, which field region is applied by providing n-type charge carriers in a concentration higher
20 that the concentration of the charge carriers in the semiconductor substrate, which first substrate portion acts as an isolation between a the field region and a conductor formed in said first through-hole and coupled to an emitter region.

25 22. A solar cell comprising a semiconductor substrate with a first side and an opposed second side, which semiconductor substrate is provided with:

- n-type dopant species in a first concentration,
- An emitter region present adjacent to the first side and
30 comprising p-type dopant species;
- A field region present adjacent to the second side and comprising n-type dopant species at a concentration higher than the first concentration, which emitter, substrate and field region together constituting a p-i-n diode;
- 35 - A via extending from the first side to the second side of the semiconductor substrate and coupled on the first side of the

substrate to the emitter region and on the second side to a back contact, and comprising electroplated metal.

23. The solar cell as claimed in Claim 22, wherein the vias are electrically insulated from the field regions through a first substrate portion adjacent to the second side thereof.

24. A method of manufacturing a solar cell, comprising the steps of:

- Providing a semiconductor substrate having a first and an opposed second side and a plurality of through-holes extending from the first side to the second side, which semiconductor substrate is provided with an emitter region and with a field region, which field region comprises charge carriers of a first conductivity type and is defined adjacent to the second side, which emitter region comprises charge carriers of a second conductivity type, opposed to the first conductivity type, and is defined adjacent to the first side;

- Applying a barrier layer onto the first side and into the through-holes;

- Applying an anti-reflective coating onto the barrier layer on the first side of the substrate;

- Applying conductive material into the through-holes so as to form vias, wherein the barrier layer prevents acid-catalysed diffusion of metal during via formation into the semiconductor substrate.

25. The method as claimed in Claim 24, wherein the barrier layer is applied with atomic layer deposition.

26. The method as claimed in Claim 24 or 25, wherein the barrier layer is applied in a thickness of at least 2 nm and at most 25 nm, preferably in the range of 3-10 nm.

27. The method as claimed in Claim 24 or 25, wherein the barrier layer comprises a first sublayer and a second sublayer.

5 28. The method as claimed in Claim 27, wherein the first sublayer has a silicon to oxygen ratio lower than the second sublayer.

29. The method as claimed in Claim 24 or 26, wherein the barrier layer is applied by oxidation of the semiconductor substrate in a rapid thermal anneal (RTA).

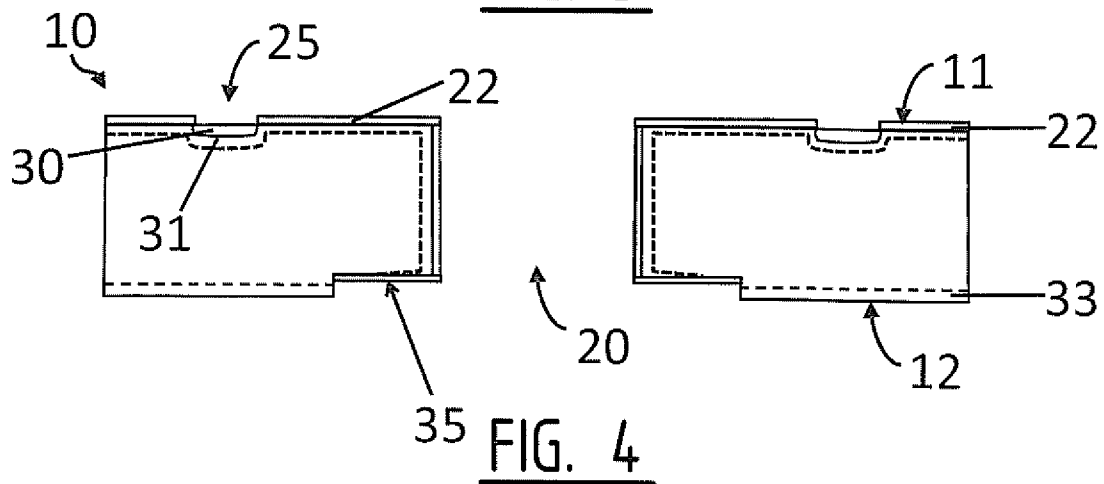
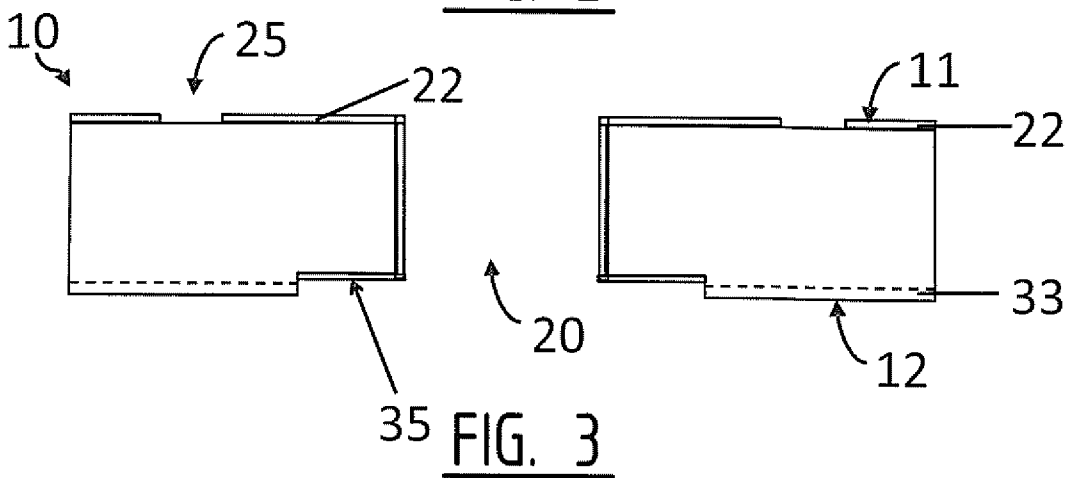
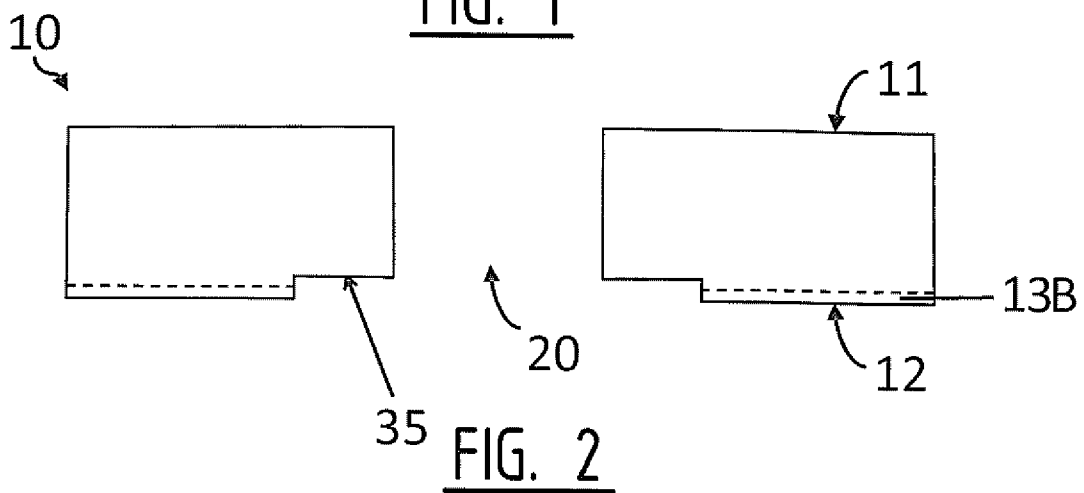
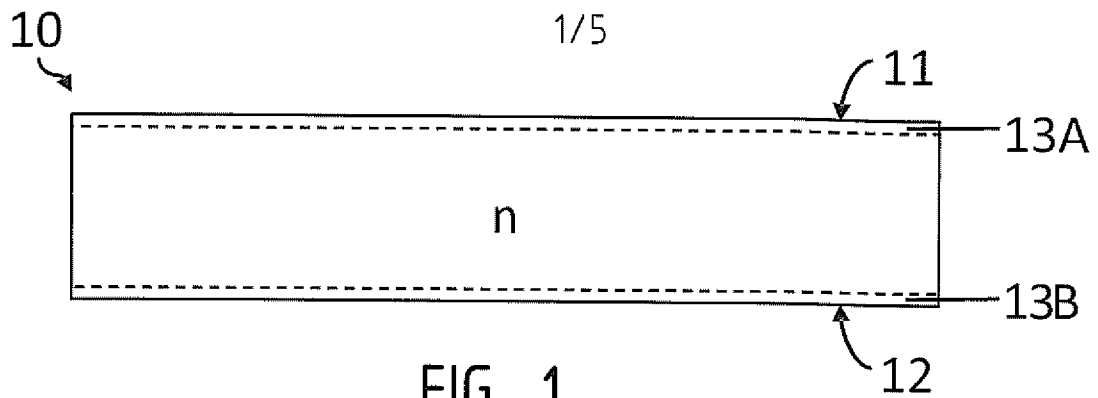
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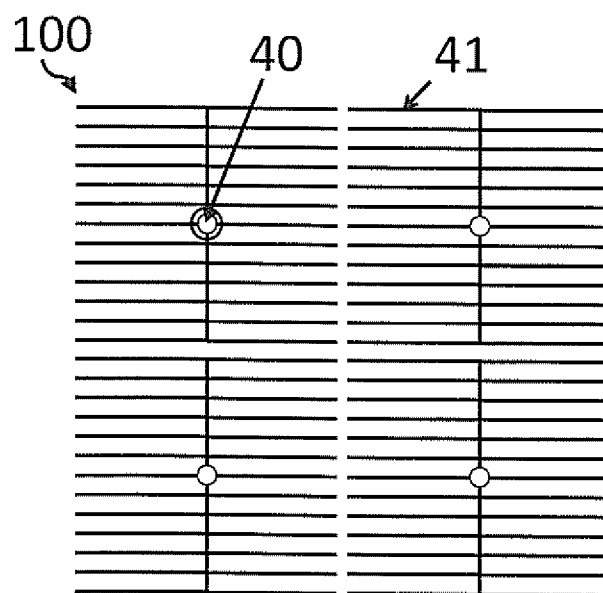
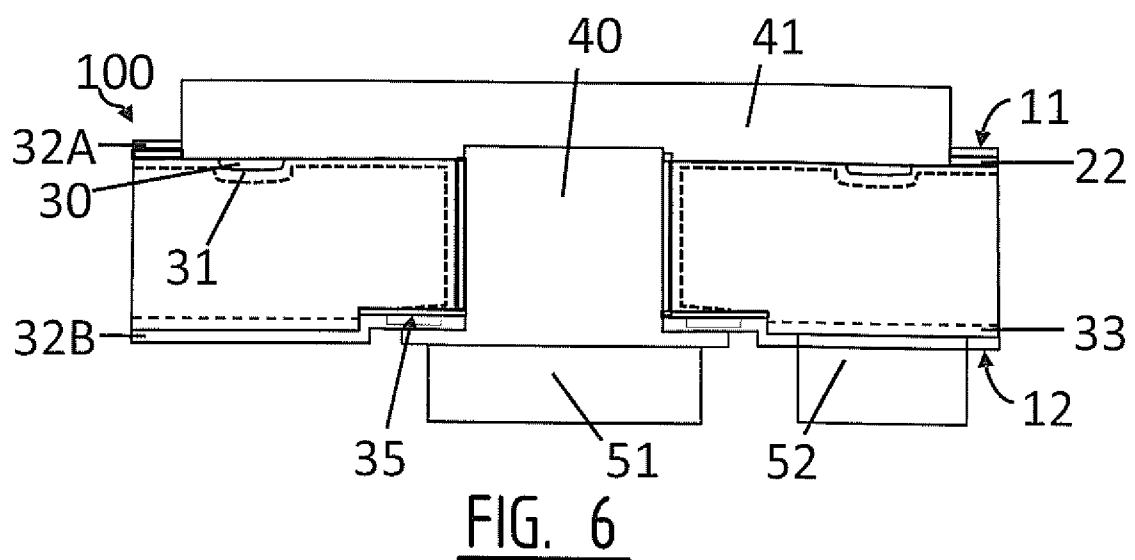
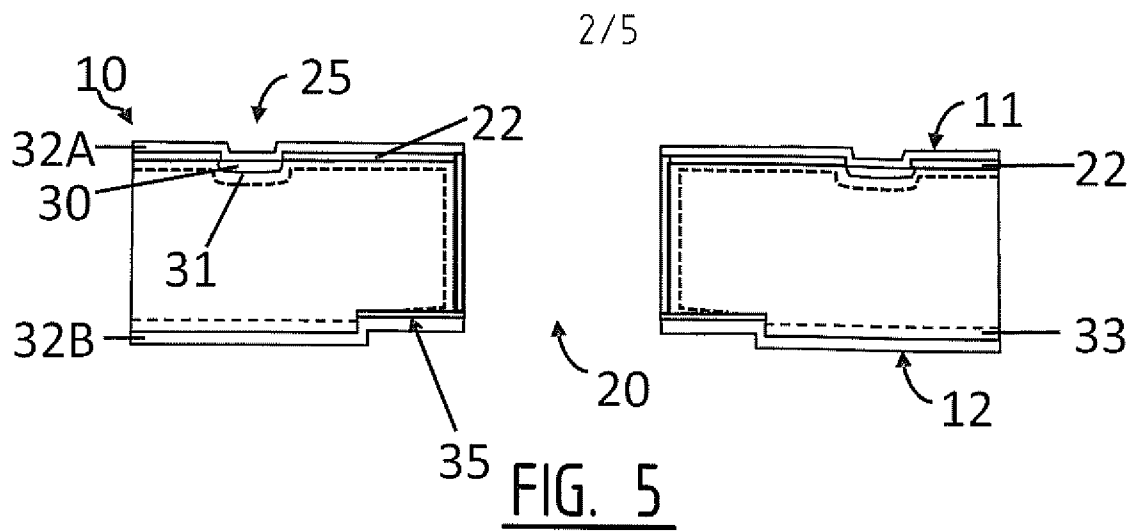
30. The method as claimed in Claim 24, wherein the conductive material is applied by electroplating.

15 31. The method as claimed in Claim 24, wherein the conductive material is applied as a metal paste, and wherein suitably a metal paste with an acid value below 130 is used for filling the through-holes.

20 32. The method as claimed in Claim 24, wherein the antireflection coating has a non-uniform composition.

33. The method as claimed in Claim 24, wherein a diameter of a through-hole at the first side of the semiconductor substrate is smaller than a diameter of the through-hole at a predefined depth.





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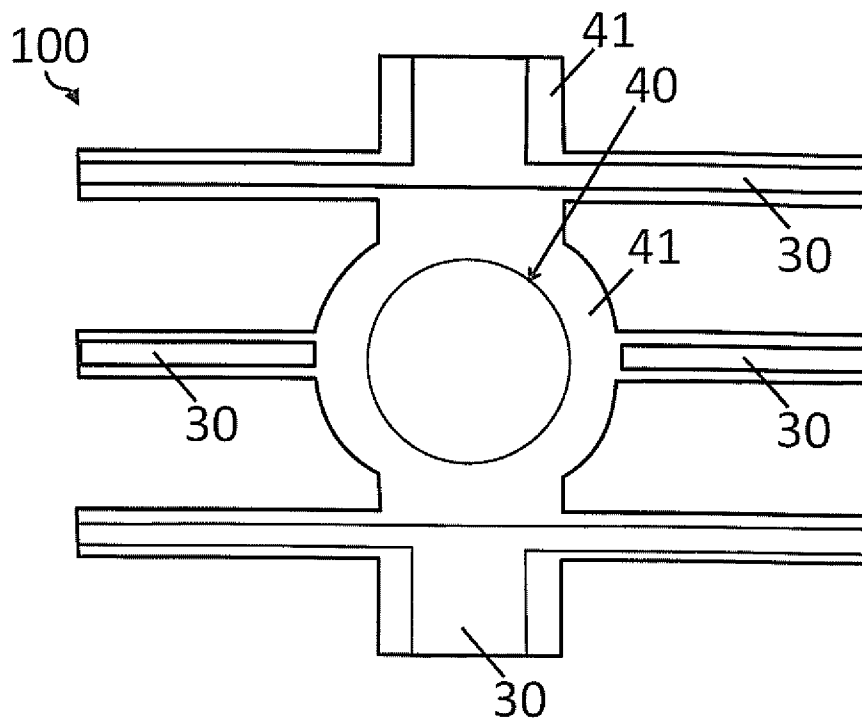


FIG. 8

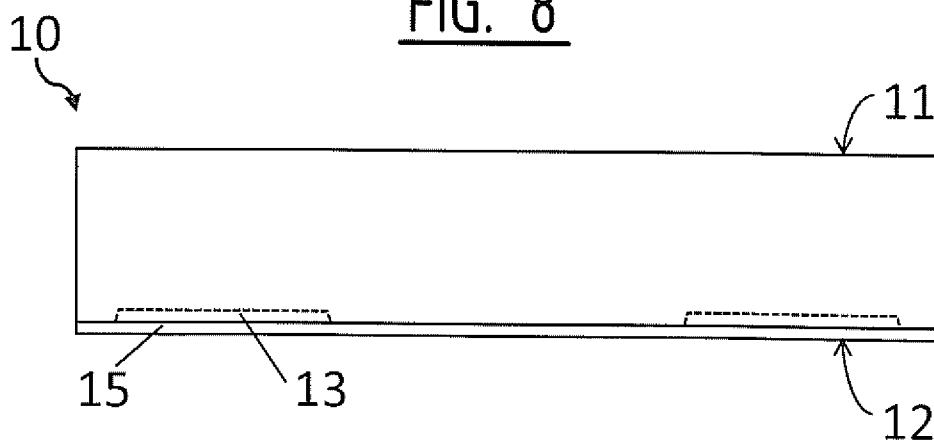
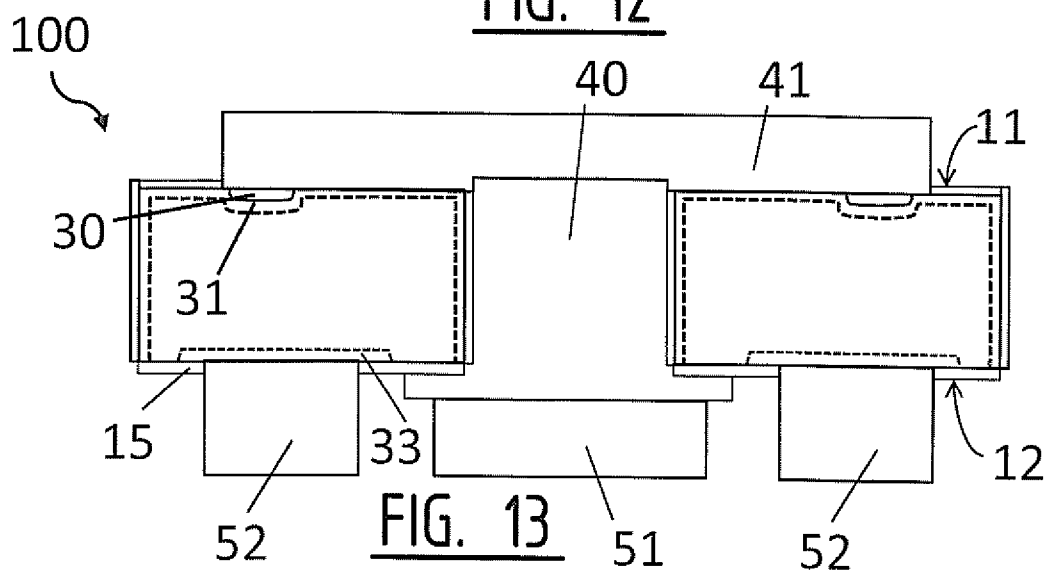
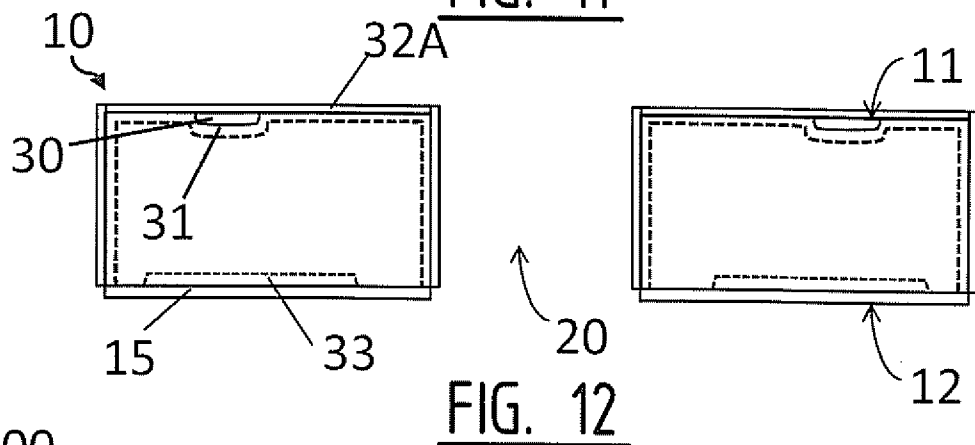
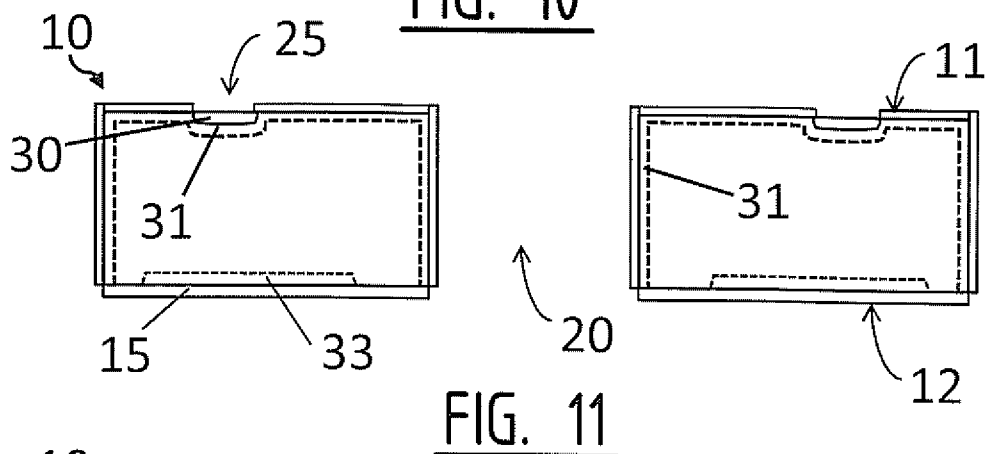
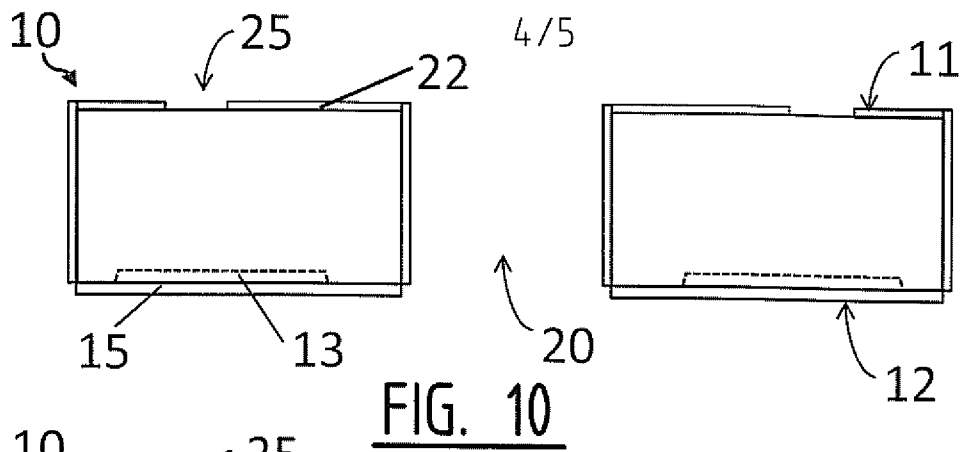


FIG. 9



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