

[54] **SOLID STATE MONETARY
ACCUMULATOR, CREDIT STORAGE, AND
SELECTOR LOGIC CIRCUIT**

[75] Inventors: **Robert W. Wheelwright,**
Tonawanda; **William V. Machanian,**
Lewiston, both of N.Y.

[73] Assignee: **The Wurlitzer Company, Chicago,**
Ill.

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[58] Field of Search..... **194/1 N, 9 R, 10, 15;**
309/215, 291

Primary Examiner—Robert B. Reeves
Assistant Examiner—Thomas E. Kocovsky
Attorney, Agent, or Firm—Olson, Trexler, Wolters,
Bushnell & Fosse

[57] **ABSTRACT**

The embodiment of the invention disclosed herein is directed to a solid state monetary accumulator, credit storage, and selector logic circuit which includes a plurality of flip-flop memory circuits for registering information corresponding to the value of coins inserted into a coin receiving mechanism, and for totaling the accumulated value of such coin accumulation to a predetermined maximum amount. Selector memory circuits are incorporated to enable a number of selections from a vending machine, such as a tape player juke box, so that selections can be made corresponding to the total value of coins inserted. Each of the flip-flop memory circuits is formed by a pair of cross-coupled logic circuits of the NOR type and have capacitors connected between the output terminals thereof and ground potential.

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3 Claims, 9 Drawing Figures

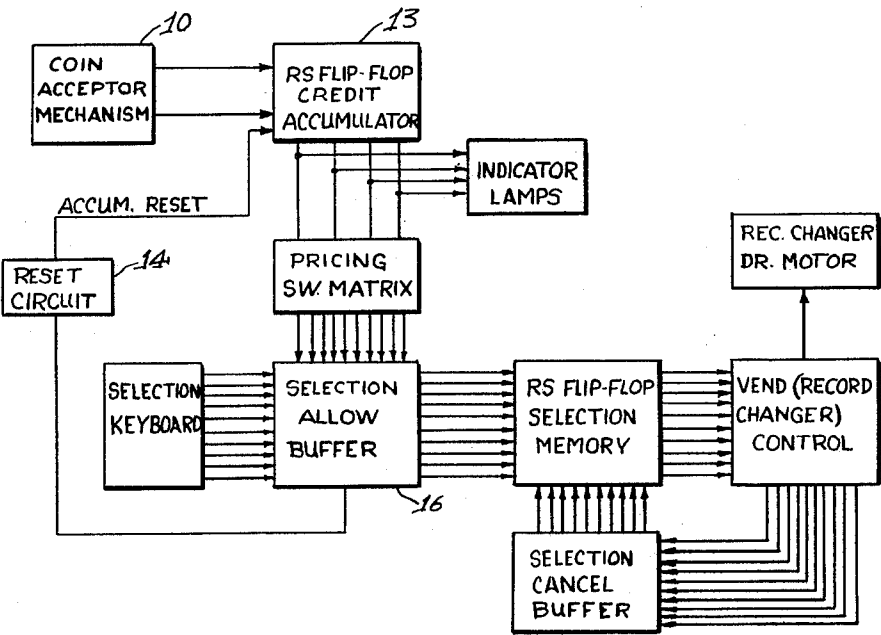


FIG. 1

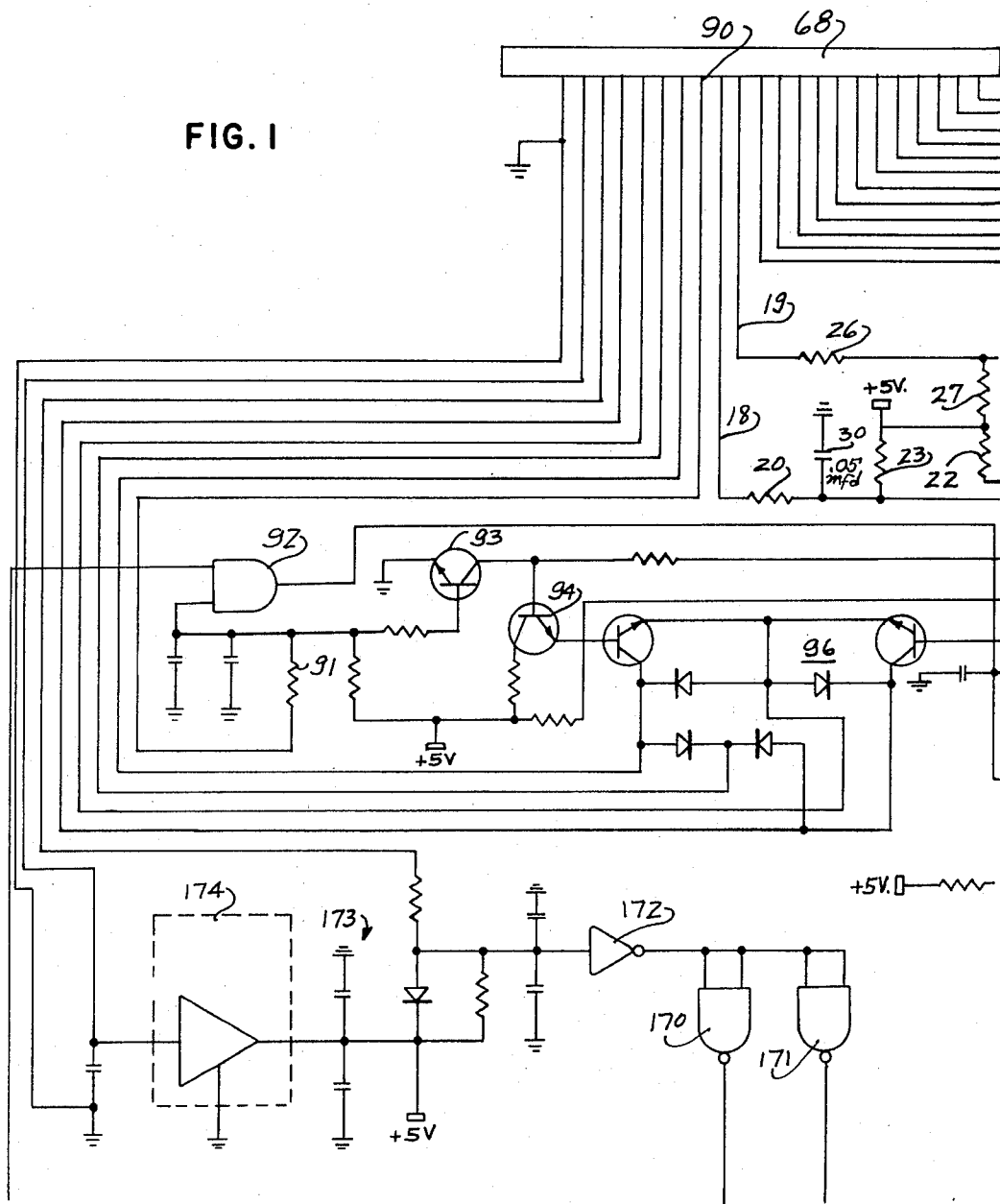


FIG. 2

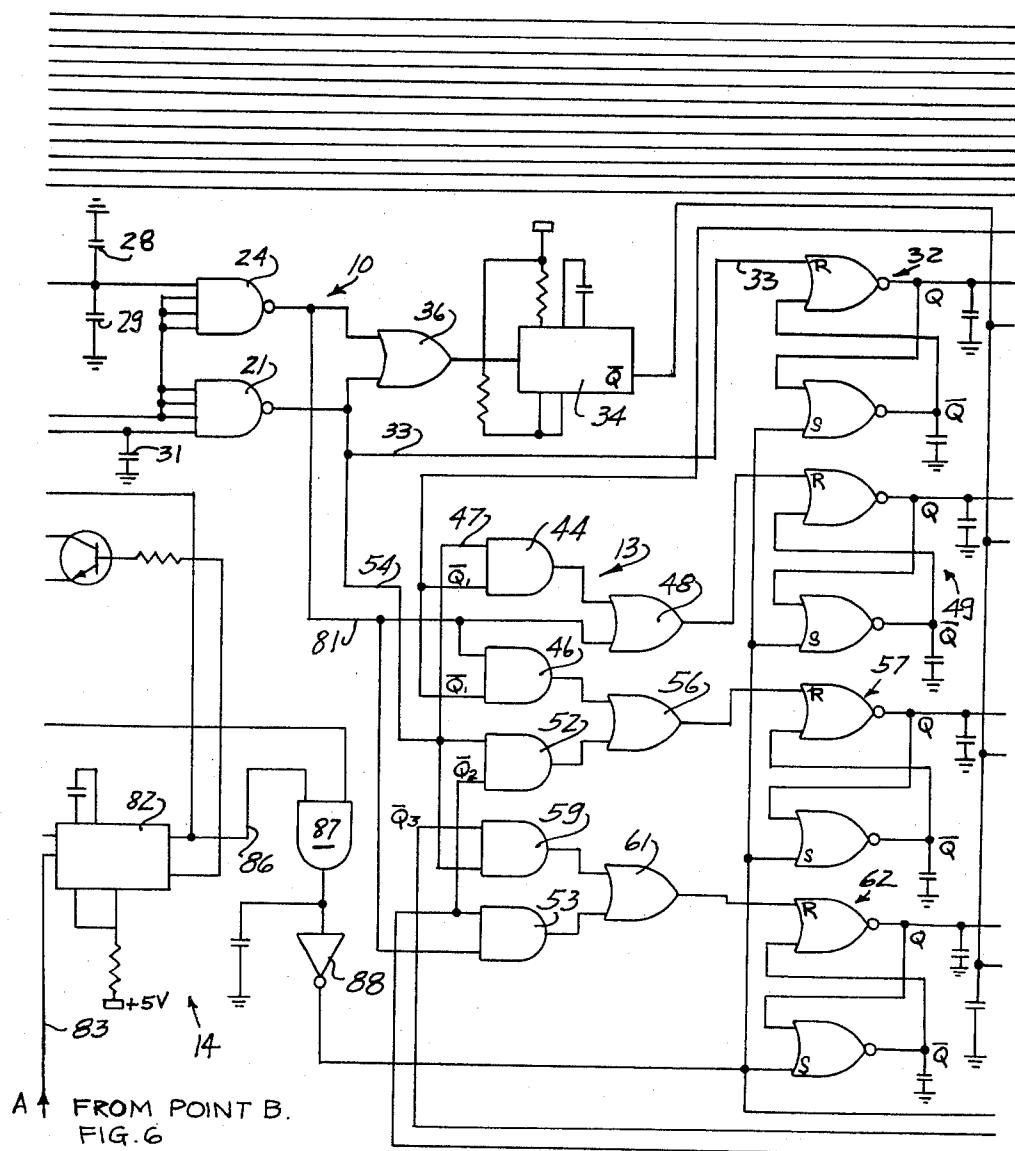


FIG. 3

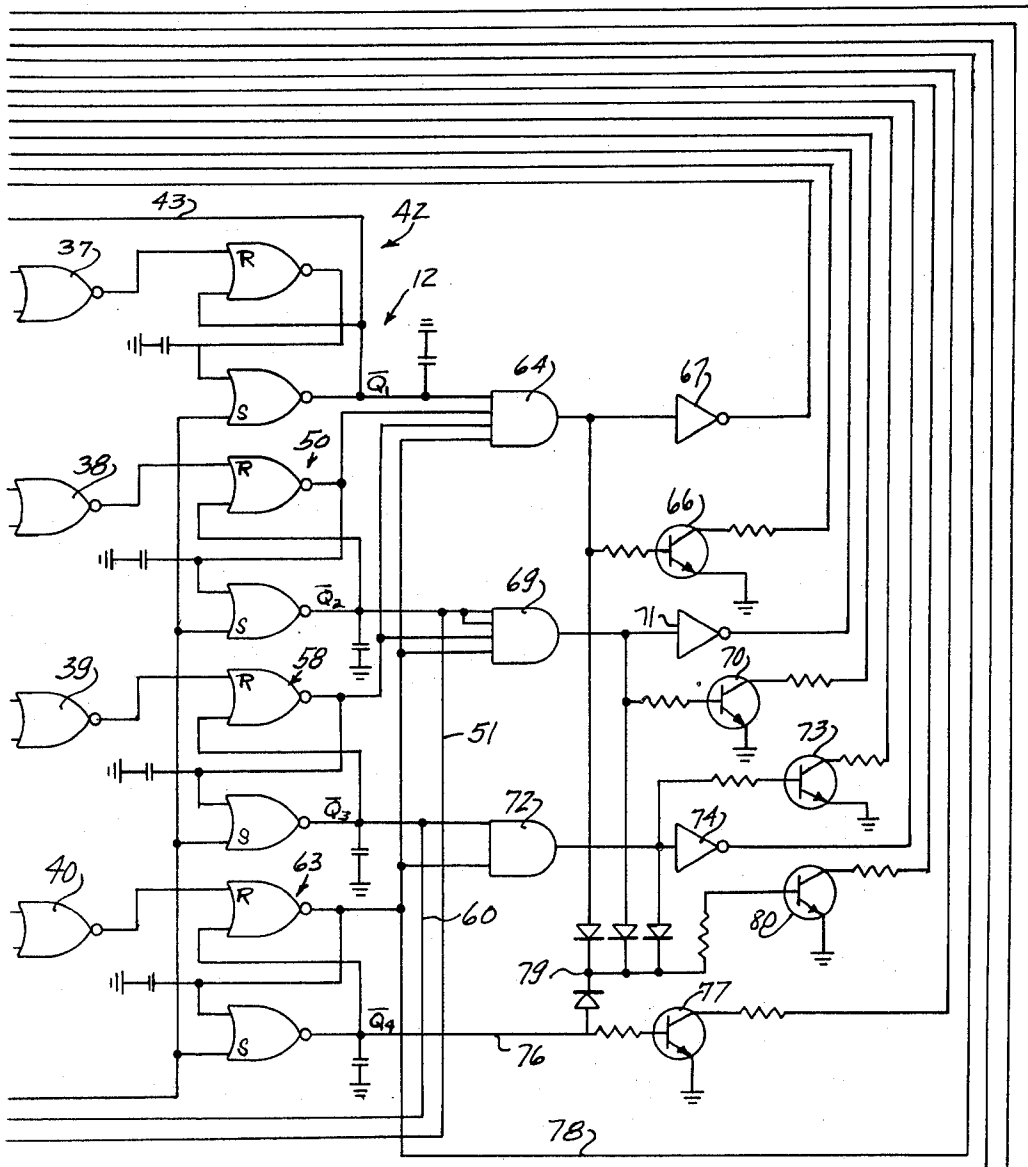


FIG. 4

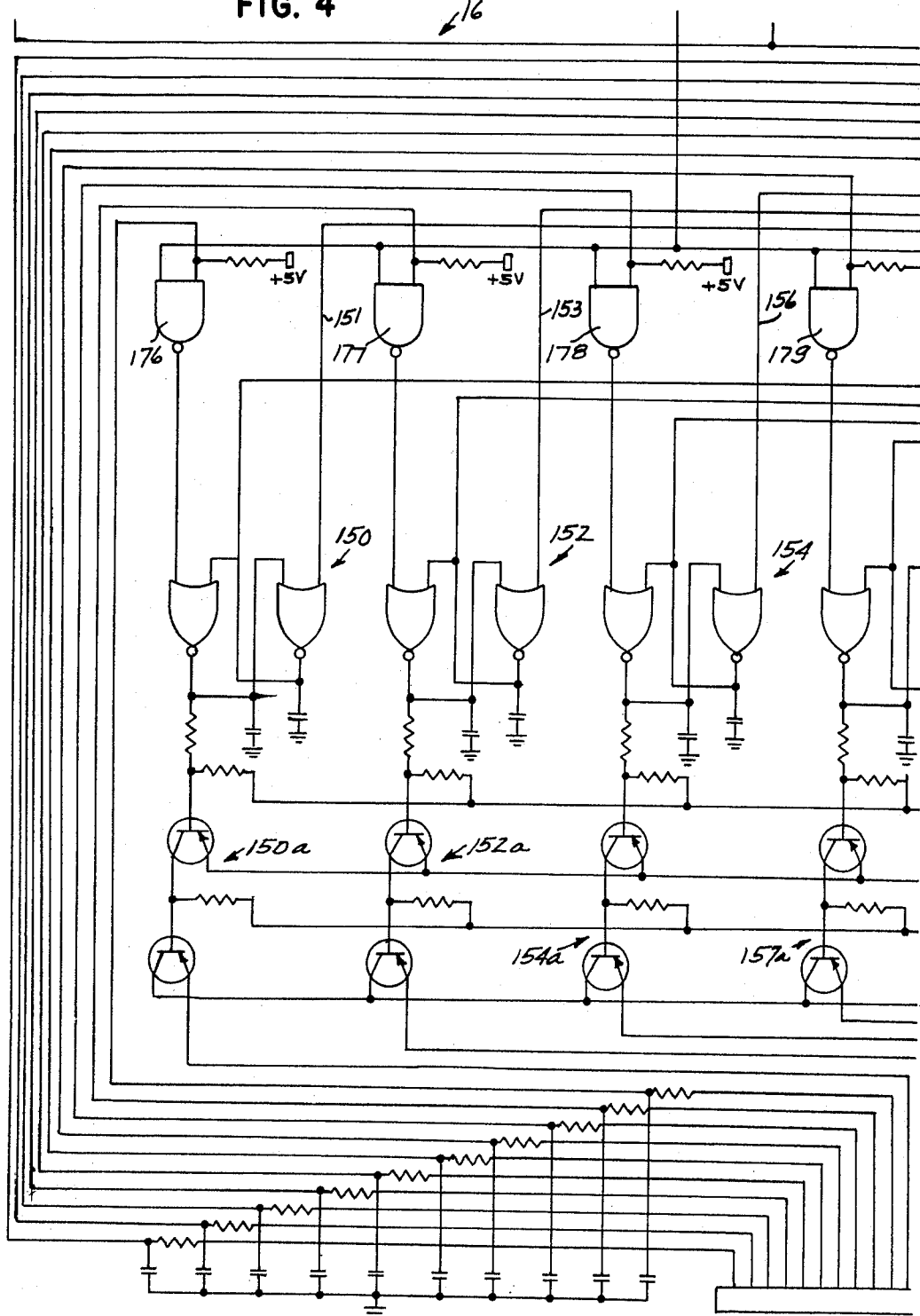


FIG. 5

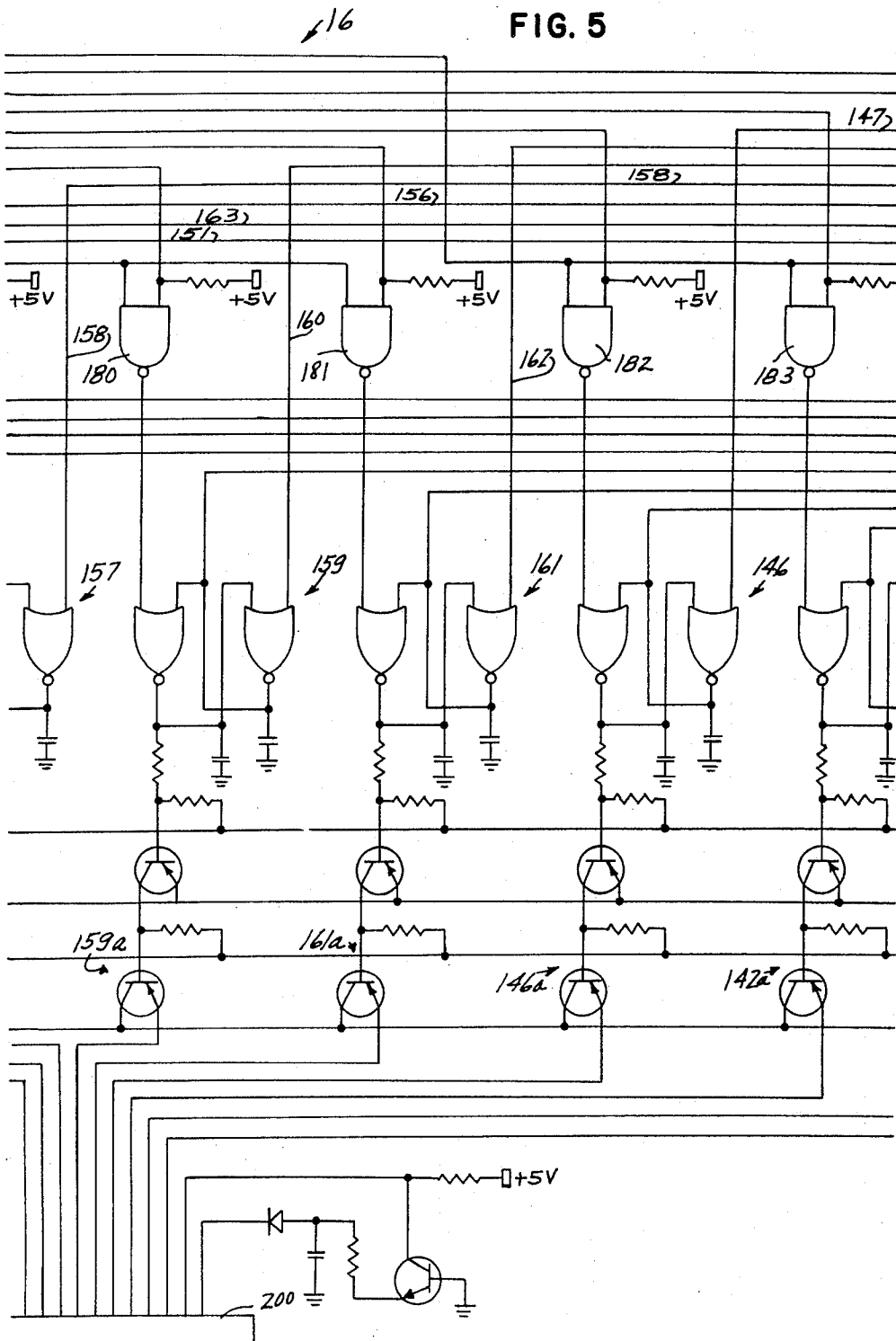


FIG. 6

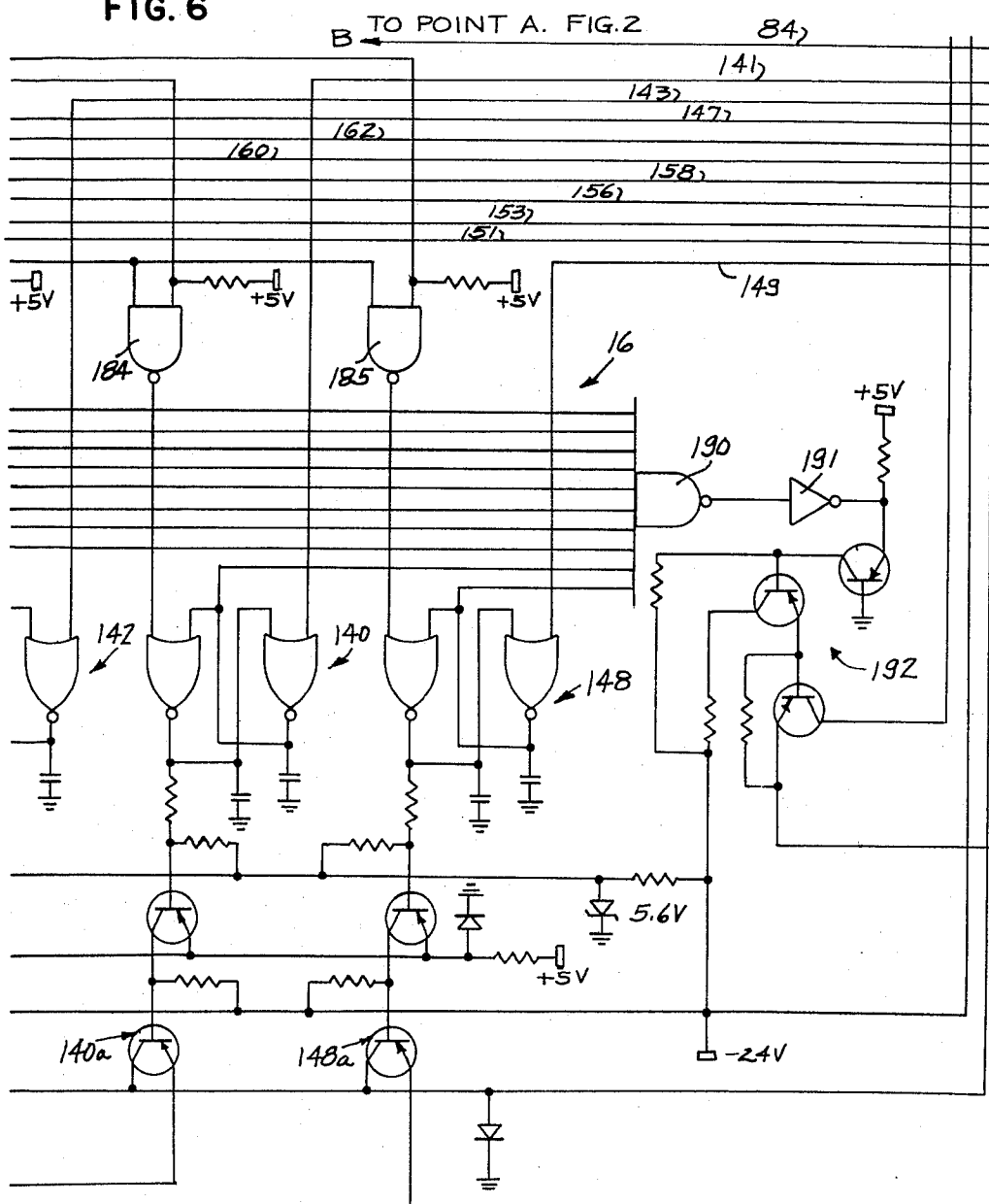
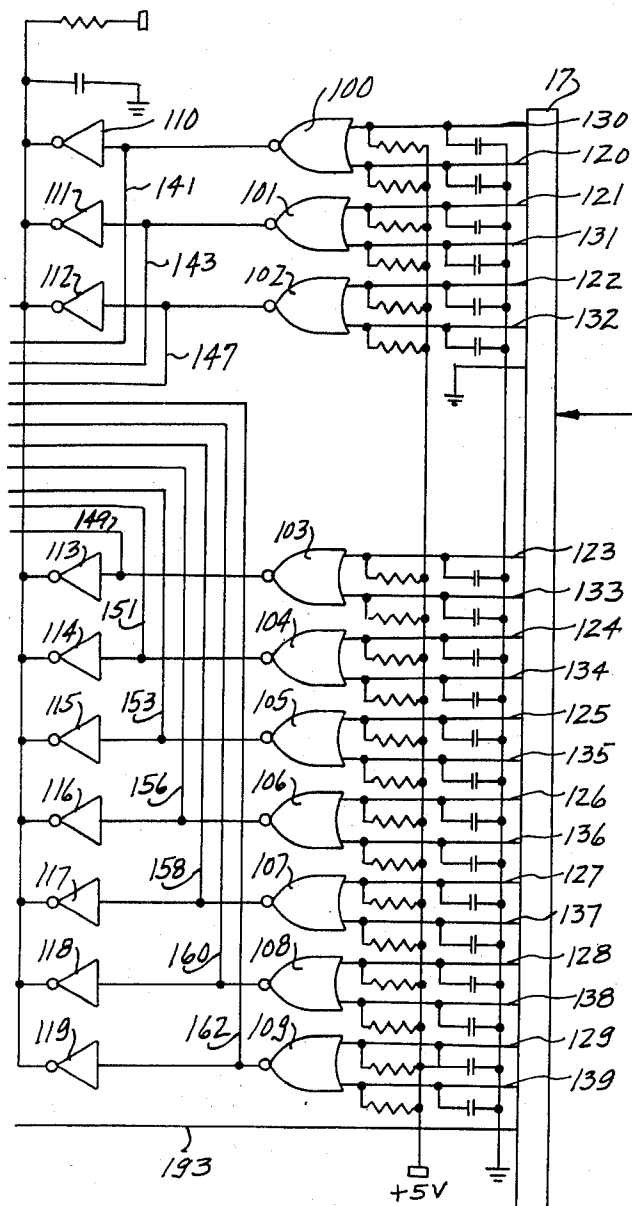


FIG. 7



FROM COIN
ACCUMULATOR &
MEMORY CKT. 12

EXTERNAL
SELECTOR
MEANS

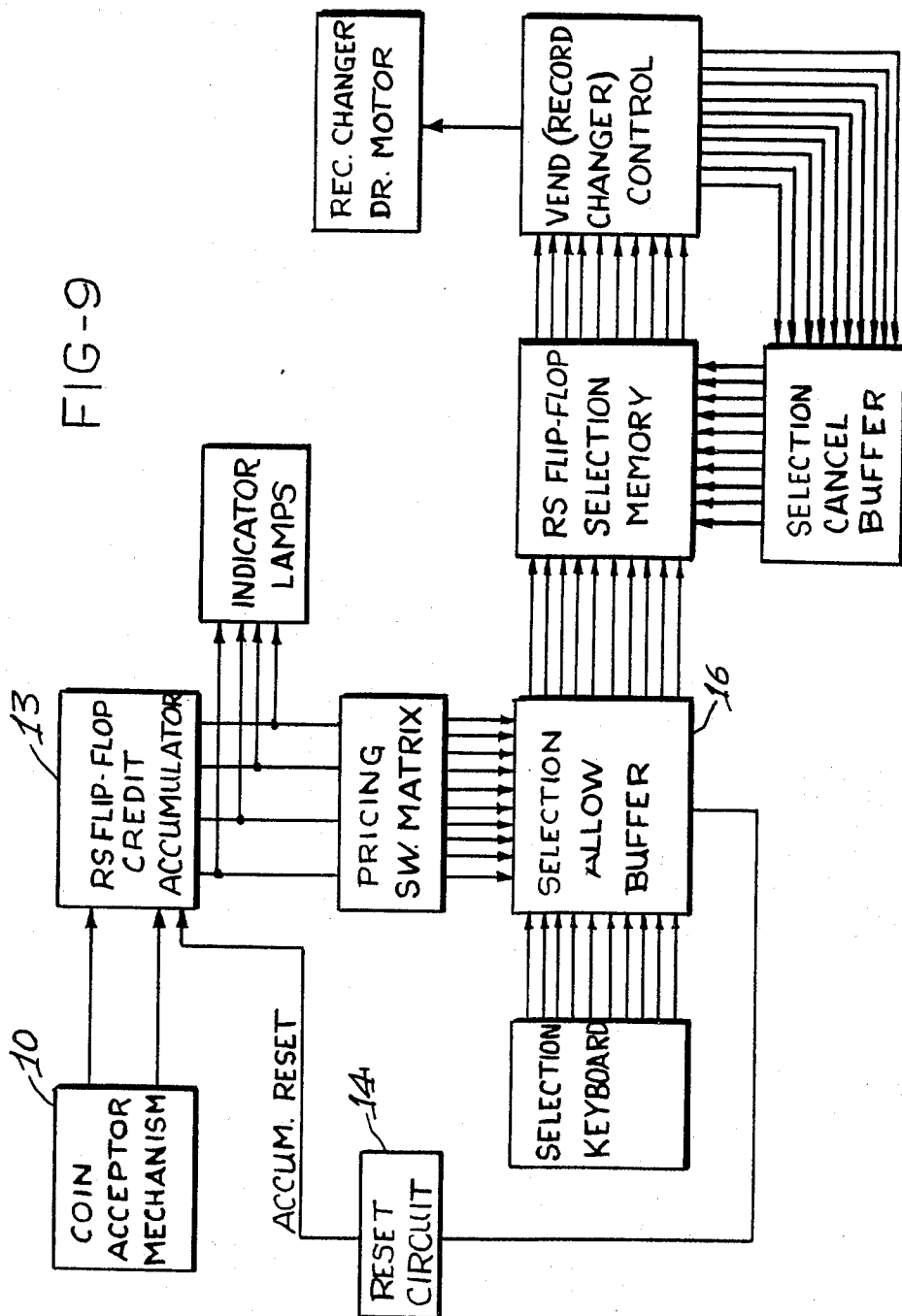
FIG. 8

FIGURE KEY

FIG. 1	FIG. 2	FIG. 3
FIG. 4	FIG. 5	FIG. 6

FIG. 7

FIG-9



SOLID STATE MONETARY ACCUMULATOR, CREDIT STORAGE, AND SELECTOR LOGIC CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates generally to a coin operated accumulator, credit storage, and selector logic circuit for use in operating a vending machine, and more particularly to a solid state logic circuit arrangement used in conjunction with juke boxes or the like which play recorded information from magnetic tape or disc records.

Coin accumulation apparatus are used in vending machines of all kinds and have found wide spread popularity for use in situations where coin accumulation is necessary because the cost of the particular items is more than the value of any particular single coin. Several coins are then necessary to actuate a release mechanism to allow selection of a particular item. While vending machines in general are anticipated for use with the present invention, it is most advantageously used in coin operated juke boxes, either of the record or tape type, wherein the number of selections obtainable by the user of the juke box is determined by the amount of coinage inserted.

The deposit of a particular value coin within a coin receiving receptacle of a juke box will allow the depositor to select a given number of plays. For example, a deposit of 25 cents may allow a single selection to be made, a deposit of 50 cents may allow two selections to be made, a deposit of 75 cents may allow three selections, and a deposit of \$1.00 may allow four selections to be made. The coin accumulation can be accomplished in any of several manners, either four quarters, one quarter, one half dollar and a second quarter, a half dollar followed by two quarters. Also a special bonus credit circuit may be incorporated to obtain bonus credit pulses in response to the energization of a 50, 75 cents, or \$1.00 accumulation. One such bonus credit arrangement which could be used in conjunction with the present invention is that disclosed in application Ser. No. 183,033, filed Sept. 23, 1971 now U.S. Pat. No. 3,222,649 and assigned to the same assignee.

One of the problems of coin accumulator circuits and mechanisms used heretofore is that they are relatively complex and use the movable contacts of relay mechanisms. Such movable contacts tend to malfunction as a result of arcing or dirt becoming lodged between the contacting surfaces thereof. Also the overall size of such electromechanical coin accumulator circuits is relatively large as well as being somewhat expensive.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide an improved coin accumulator, credit storage, and selector logic circuit which is formed of integrated circuit components of small size and which is simple and inexpensive to manufacture while maintaining a high degree of reliability and efficiency in use.

Briefly, a feature of this invention resides in the use of a plurality of flip-flop memory circuits formed by cross-coupled logic NOR gates which have capacitor elements connected between their output terminals and ground potential.

Many other objects, features, and advantages of this invention will be more fully realized and understood

from the following detailed description when taken in conjunction with the accompanying drawings wherein like reference numerals throughout the various views of the drawings are intended to designate similar elements or components.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-7 illustrate a detailed schematic logic circuit for the solid state monetary accumulator, credit storage, and selector logic circuit of this invention;

FIG. 8 is a figure key showing the arrangement of the seven figures for proper understanding; and

FIG. 9 is an overall block diagram of the circuit arrangement of this invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Throughout the specification and claims it will be understood that the terms "monetary accumulator" and "coin accumulator" are interchangeable and means the accumulation of credits for value.

Referring now to the FIGS. 1-7 of the drawings as arranged as shown in FIG. 8, a detailed circuit arrangement of a solid state coin accumulator, credit storage, and selector logic circuit is shown. The circuit arrangement of this invention includes a first circuit means for producing logic pulse signals which correspond to the value of coins inserted into a conventional coin receiving mechanism, not shown, which closes switches to indicate the relative value of the coins so inserted. The output of the first circuit is connected to a plurality of credit storage flip-flop circuits having inputs thereof coupled to the first circuit through a gating logic arrangement. The plurality of flip-flop storage circuits provide discrete output signals at a plurality of output terminals each of which corresponds to a different total accumulation of coins as inserted into a coin receptacle. Each of the output terminals of the credit storage circuits are arranged for connection to a selector mechanism usually located on the front of a vending machine, such as a juke box or the like, so that a selection can be made corresponding to the total value of coins as represented by the then energized output terminal, that is, the circuit shown allows only one selection to be made and this selection must have a value equal to the amount of accumulated credit. Either upon initial actuation of a selector switch or by actuation of a coin return switch, a second circuit means is energized to provide a reset signal to the plurality of credit storage circuits. This reset signal then reestablishes a start condition so that subsequent insertions of coins can be accumulated as before to again attain a maximum or desired value.

A plurality of selector memory circuits are connected through the selection input gating circuit shown in FIG. 7 and connector 17 to the selector buttons on the front of the vending machine. When the proper credit exists and a selection is made, the selection signal is delivered to the selector memory which, in turn, causes rotation of a turret, not shown, which turret will carry records or magnetic tape cassettes into registry with playback means. When the record or tape cassette on the turret is in the proper position, an indexing contact is actuated to cause stopping of the motor driven turret until such time as a recycling signal is obtained at the end of record play or tape play. This will cause the turret to again index to the next position

which corresponds to the previously inserted selection this being accomplished in a manner well known in the art.

For a better understanding of the details of the first circuit 10, for registering coin accumulations, attention is now directed primarily to FIGS. 1 and 2. The first circuit 10 receives pulse signal information over a pair of lines 18 and 19, which correspond to the insertion of 25 and 50 cent coins respectively. A 25 cent coin impulse supplied to line 18 will be developed across a resistor 20 and is applied to one input terminal of NAND gate 21 which forms a Schmitt Trigger. The other inputs of the NAND gate 21 are tied together to a five volt terminal point through a resistor 22. When a 25 cent coin is inserted, a ground potential is sensed across resistor 20 which, in turn, substantially reduces the voltage applied to the input of NAND gate 21 since the resistor 20 is of much smaller value than a resistor 23 which is connected between the input terminal and the supply voltage. A second NAND gate 24 which also forms a Schmitt Trigger, has one input thereof connected through the line 19 to a 50 cent coin switch and will register a pulse output upon sensing the closure of such switch. This grounded potential is sensed through a resistor 26 which reduces the voltage applied to the input terminal through a resistor 27 since resistor 26 is of lesser value. A pair of filter capacitors 28 and 29 are connected to the input terminal of NAND gate 24 to eliminate the possibility of transient pulses producing erroneous coin signal information. Similarly, a pair of capacitors 30 and 31 are connected across the input of the NAND gate 21 also to eliminate the possibility of transient pulses from causing extraneous coin input signal information.

A pulse output from either one of the NAND gates 21 or 24 will be delivered to the gate circuit arrangement 13 and therefrom to the coin accumulator memory circuit 12. The output NAND gate 21 is first delivered to an input of a flip-flop memory circuit 32 over a line 33 to change the state of the flip-flop 32. Simultaneously, the output of NAND gate 21 is delivered to a one-shot multivibrator integrated circuit component 34 through an OR gate 36. The output of the one-shot multivibrator integrated circuit 34 is applied to a gating input terminal of a plurality of NOR gates 37, 38, 39, and 40 which are interposed between two groups of coin accumulator memory flip-flop circuits. The purpose of the one-shot multi-vibrator circuit 34 is to provide a time delayed pulse to the gating circuits so that a transfer of the pulse signal information from flip-flop circuit 32 to a storage memory flip-flop circuit 42 is accomplished only after the proper coin insertion has been sensed. Once the output of the second flip-flop circuit 42 is set the output line 43 thereof is coupled back to the inputs of a pair of AND gates 44 and 46 of the gating circuit 13. This partially sets the condition for these AND gates. Therefore, upon insertion of a second quarter to develop another output pulse from NAND gate 21 the second pulse signal is delivered over the line 33 to the flip-flop 32. Since the flip-flop 32 is already set, this pulse signal is ineffective. The second output signal from NAND gate 21 is also delivered through a line 47 to a second input of the AND gate 44 to produce an output signal therefrom. This output signal is coupled through an OR gate 48 to set a second flip-flop circuit 49 of the coin accumulator and memory circuit 12. A delayed signal is again coupled

through the one-shot multivibrator 34 to the second input of the NOR gate 38, and in combination with the output of flip-flop 49 will cause a transfer signal to be delivered to a flip-flop circuit 50. This then changes the state of an output line 51 which is coupled back to the inputs of a second pair of AND gates 52 and 53 of the gating circuit 13. This sets the initial condition for these two AND gates. A third input of a quarter will again produce an output pulse at the NAND gate 21 which, in turn, is delivered over a line 54 to the input of an AND gate 52. This produces an output through an OR gate 56 to set a flip-flop circuit 57 in the same manner as mentioned above. This setting condition then is coupled through the NOR gate 39 when the time delay pulse from the one-shot multivibrator 34 is applied thereto. This then sets an associated second flip-flop circuit 58 which corresponds to a 75 cents total credit accumulation of coins. For a maximum accumulation of \$1.00 credit a fourth quarter is inserted into the coin receiving mechanism to produce a fourth output pulse from the NAND gate 21. This fourth output pulse is delivered to an AND gate 59 of the logic circuit 13. Also delivered to the AND gate 59 is an output signal from the flip-flop 58, this output signal being delivered over the line 60. This will produce an output pulse through the OR gate 61 which, in turn, will set a flip-flop circuit 62 to condition one input of the NOR gate 40. The time delay pulse from the one-shot multivibrator 34 will then allow transfer of this signal information to set a flip-flop circuit 63 which will produce a \$1.00 credit output signal.

The output of the flip-flop circuit 42 is connected to one of the inputs of a four input AND gate 64. The other three inputs of the AND gate 64 are connected to the normally high or logic one state outputs of flip-flops 50, 58, and 53, so that the output of the AND gate 54 will go high or to a logic one state upon sensing the insertion of a first quarter. This will energize a transistor circuit 66 which, in turn, will energize an indicating lamp to show that a 25 cents credit accumulation has taken place. The output of AND gate 64 is also delivered to an amplifier and inverter circuit 67 which, in turn, is coupled back to a connector terminal socket 68 so that a selector mechanism can be energized to cancel credits of up to and including 25 cents in value.

An AND gate 69 has two of its inputs coupled together and connected to the output of flip-flop 50 which registers an accumulated credit of 50 cents, either by the insertion of two quarters or by the insertion of a single 50 cent piece. The other two inputs of AND gate 69 are connected to the normally high outputs of flip-flop circuits 58 and 63 so that an output signal of a logic one state is obtained to energize a transistor circuit 70 when 50 cents accumulation is registered. The transistor circuit 70 energizes an indicating lamp to give the operator of the vending machine a visual indication that he has accumulated credits to 50 cents in value. Also connected to the output of AND gate 69 is an amplifier inverter circuit 71 which energizes selector means to increase the maximum number of selections previously obtained to allow selections which are worth exactly 50 cents in value. A third AND gate 72 has only a pair of inputs, one of which is coupled to the output line of flip-flop circuit 58 and the other of which is coupled to the normally high output of flip-flop 63. The AND gate 72 then produces a logic one state when total credit accumulation of 75 cents is obtained. This

will energize a transistor circuit 73 to light an indicating lamp giving the operator a visual indication that credits to 75 cents have been registered. Also connected to the output of AND gate 72 is an inverter amplifier circuit 74 which allows a selection worth 75 cents in value. Upon insertion of a fourth quarter, or a second 50 cent piece, the fourth flip-flop circuit 63 is energized to change its state so that the output terminal thereof will provide a logic one condition on the line 76 to energize the transistor circuit 77 which, in turn, will energize an indicating lamp showing that \$1.00 credit accumulation has taken place. The output of flip-flop circuit 63 is directly coupled to the connector plug 68 over a line 78 to energize selector means to enable the user of the vending machine to make a selection worth \$1.00 in value.

A diode steering network 79 includes four diodes coupled to the outputs of the AND gates 64, 69, 72, and to the output of the flip-flop circuit 63. This energizes a transistor circuit 80 which is connected to a credit lamp circuit so that the operator thereof knows he does have credits being accumulated during insertion of coins one after the other. If a selection is made between coins then the accumulation of credits ceases and must start over.

When a 50 cent coin is inserted into the coin receiving mechanism the output of NAND gate 24 produces a signal which is delivered to the OR gate 48 over a line 81. This then causes setting of the flip-flop circuit 49 which, in turn, changes the state at the input of NOR gate 38. A time delayed signal is then delivered to the NOR gate 38 to set the second flip-flop circuit 50 to register an accumulated credit of 50 cents. Therefore, when a 50 cent coin is used rather than two quarters, the output pulse produced at NAND gate 21 is completely bypassed and the flip-flop circuit 42 is not set.

When a second 50 cent piece is inserted into the coin receiving mechanism a second output pulse is developed at the output of the NAND gate 24 and is delivered to one of the inputs of the AND gate 53 and again to the OR gate 48. Since the flip-flop circuit 50 has been set, the high output line thereof is delivered to the AND gate 53 to condition it to produce a pulse to the one of the inputs of the OR gate 61 and set the flip-flop 62. The output from OR gate 48 has no effect since the flip-flop circuit 49 is already set. After the time delayed pulse from the one-shot multivibrator 34 has been delivered to the NOR gate 40 the flip-flop circuit 63 is set to produce a credit accumulation indication of \$1.00. It will be noted that if the second coin after the first 50 cents is a quarter an output pulse from NAND gate 21 is delivered to the input of AND gate 52 which has its input thereof set by the output of flip-flop circuit 50. This will then produce a pulse through the OR gate 56 to set the flip-flop circuit 57 which, in turn, will set flip-flop circuit 58 to give a credit indication of 75 cents. Upon insertion of a third coin, which in this case would be a quarter, the output pulse of NAND gate 21 is treated substantially in the same manner as the fourth output pulse thereof as described above with regard to using four quarters. This will produce a total accumulated credit indication of \$1.00.

The second circuit means 14, FIG. 2, includes a one-shot multivibrator 82 which has a first input terminal 83 thereof connected back to a line 84, FIG. 6, and to the output of a plurality of ganged together converter amplifiers which are responsive to actuation of any one

of a corresponding plurality of selector switches. Therefore, when a selection is made an output signal is developed at line 86 of the one-shot multivibrator 82, and this output is delivered through an AND gate 87 which has the other input thereof already in a logic one state. This will produce an output through the inverter amplifier stage 88 to apply a reset signal to all of the flip-flops within the coin accumulator memory circuit 12.

All of the flip-flops within the coin accumulator memory circuit 12 are also reset upon actuation of a coin return switch connected in circuit with a line 90 of the plug 68. This is accomplished by applying a signal over the line 90 and through a resistor 91 to the input of an AND gate 92 which, in turn, has its output connected back to the AND gate 87. A signal through resistor 91 is also applied to the base electrode of a transistor 93 to apply a signal to a second input of the one-shot multivibrator 82 and thereby produce a reset pulse through the AND gate 87 and inverter amplifier 88.

When transistor 93 is energized so also is a transistor 94 which, in turn, actuates a cash drop control circuit 96 which comprises a pair of transistors and a plurality of diodes connected in the emitter circuits thereof. When the selector system is actuated to select a particular item, or musical selection, the cash drop circuit arrangement causes the coins inserted into the coin receiver to be deposited into a receptacle for safekeeping. However, should the coin return line 90 be actuated before a selection is made the coins in the coin receiver will be dropped into a coin return trough in a manner well known in the art. The transistors and diodes of the circuit 96 also insure that all of the flip-flop circuits within the memory accumulator circuit 12 are set to the right starting condition, i.e. with no coin accumulation being registered therein when power is initially applied.

Now referring to the selector and enable circuits shown in FIG. 7, a plurality of NOR gates 100, 101, 102, 103, 104, 105, 106, 107, 108, and 109 are provided and each have their output coupled to a corresponding one of a plurality of inverter circuits 110, 111, 112, 113, 114, 115, 116, 117, 118, and 119. As mentioned above the outputs of the inverter circuits 110-119 are tied together to a common line 84 which, in turn, is connected to the input line 83 of the one-shot multivibrator 82 for energizing the same to change the logic state of the inverter upon actuation of any one of a plurality of selector switches. When the proper coinage is inserted into the coin accumulator circuit described above a plurality of allow lines are enabled. For example, the allow lines 120, 121, 122, 123, 124, 125, 126, 127, 128, and 129 are energized to apply a logic signal to one of the inputs of the plurality of NOR gates 100-109. When a logic zero condition exists on both of the inputs of any one of the NOR gates and output signal is delivered to the corresponding inverter as mentioned above. Also, an output signal is delivered across a corresponding line to one of the plurality of memory selector circuits 16. For example, the output of NOR gate 100 is delivered to a memory flip-flop circuit 140 over a line 141. The output of NOR gate 101 is delivered to a memory flip-flop circuit 142 over a line 143. The output of NOR gate 102 is delivered to a flip-flop circuit 146 over a line 147. The output of NOR gate 103 is delivered to a flip-flop memory circuit 148 over

a line 149. The output of NOR gate 104 is delivered to a memory flip-flop circuit 150, FIG. 4, over a line 151. The output of NOR gate 105 is delivered to a memory flip-flop circuit 152 over a line 153. The output of NOR gate 106 is delivered to memory flip-flop circuit 154 over a line 156. The output of NOR gate 107 is delivered to memory flip-flop circuit 157 over a line 158. The output of NOR gate 108 is delivered to a memory flip-flop circuit 159 over a line 160. Finally, the output of NOR gate 109 is delivered to a memory flip-flop circuit 161 over a line 162. Therefore, an output signal from any one of the NOR gates 100-109 as a result of actuation of a selector switch will correspondingly set one of the memory flip-flop circuits within the memory selector circuit 16. Each of the memory flip-flops within the memory selector circuit 16 is constructed by crosscoupling a pair of NOR gates in substantially the same manner as that of the flip-flops shown in the coin accumulator and credit circuit 12. Most advantageously the output terminal connections of each of the flip-flops, both those in the coin accumulator memory circuit 12 and in the selector circuit 16, have connected thereto capacitor elements. These capacitor elements have a value in the order of about 0.01 MFD. to 0.10 MFD. and preferably in the order of about 0.05 MFD.

To reset all of the flip-flop memory units of the selector memory circuit 16 a pair of NAND gates 170 and 171 have their inputs tied together to the output of an inverter amplifier 172 which, in turn, is connected to a voltage control circuit arrangement designated generally by reference numeral 173. This insures that all of the flip-flop units within the selector memory circuit 16 are set to an initial condition prior to energization of any of the coin accumulator circuits. The voltage control circuit 173 preferably includes a voltage regulator circuit 174 which maintains a regulated five volt potential at its output to insure proper operation.

The reset signal from NAND gates 170 and 171 are delivered through a corresponding one of a plurality of NAND gates 176, 177, 178, 179, 180, 181, 182, 183, 184, and 185 connected to the reset input of its associated flip-flop unit. These NAND gates are used as buffer invertors. Therefore, when the input to the NAND gates 176-185 are energized all of the flip-flop circuits are reset to an initial condition.

To operate a motorized positioning turret mechanism of a juke box, or the like, the outputs of the flip-flop circuits 140, 142, 146, 148, 150, 152, 154, 157, 159, and 161 are connected to associated cascade coupled transistor amplifier circuits 140a, 142a, 146a, 148a, 150a, 152a, 154a, 157a, 159a, and 161a. The turret mechanism is energized by a ten input NAND gate 190 which, in turn, is coupled through an inverter stage 191 to a transistorized circuit 192. The output of the transistor circuit 192 is coupled through a line 193 to start the motor and rotate the carriage or turret. When a selection is made to change the state of the flip-flop circuits within the selector memory circuit 16 the associated flip-flop circuit is actuated which, in turn, actuates its output transistors to provide a closed circuit at a particular contact point. Therefore, as the rotating turret senses this particular position as coupled through a plu-

ality of lines extending from a connector 200 the carriage will stop rotation. After completing the play of the record or cassette tape a start pulse is developed to again initiate rotation of the carriage until it comes in registry with a contact associated with a particular one of the output amplifier stages of the selector memory circuit to stop the carriage.

The circuit arrangement illustrated in FIGS. 1-7 is commonly referred to as a transistor-transistor logic (T²L). However, applying capacitors between the outputs of crosscoupled NOR gates and ground potential substantially improves stability of operation so that extremely inexpensive and simplified circuitry can be used with high reliability. FIG. 9 illustrates the overall block diagram of the specific circuit arrangement illustrated in FIGS. 1-8 and has the primary block functions designated with corresponding reference numerals. It will be understood that the NOR gates disclosed herein may be substituted with NAND gates if desired. While only a single embodiment of the present invention is disclosed herein it will be understood that numerous variations and modifications may be effected without departing from the spirit and scope of the novel concepts disclosed and claimed herein.

The invention is claimed as follows:

1. A monetary accumulator, credit storage, and selector logic circuit comprising, first circuit means for providing logic pulse signals which correspond to the value of coins sensed thereby, a plurality of memory circuits having inputs coupled to said first circuit means, said memory circuits providing discrete output terminals each corresponding to a different total accumulation of coins as registered by said first circuit means, each of the said output terminals arranged for connection to selector means to enable said selector means so that selections can be made corresponding to the total accumulation of coins as represented at the output terminal so energized, each of said plurality of memory circuit is formed by first and second cross-coupled logic circuits, each having a pair of inputs, one input of said first logic circuit being coupled to said first circuit means, one input of said second logic circuit being coupled to a second circuit means, and the output terminals of each of said first and second logic circuits being cross-coupled back to the other input of the other of said first and second logic circuits, to form an R-S flip-flop circuit, a capacitor connected between the output terminals of each of said logic circuits and ground potential, and said second circuit means being connected to said plurality of memory circuit and arranged for connection to said selector means to provide a reset signal to said plurality of memory circuits upon actuation of any one of the selector means.

2. The coin accumulator, credit storage, and selector logic circuit according to claim 1, wherein each of said capacitors has a value in the order of about 0.05 MFD.

3. The coin accumulator, credit storage, and selector logic circuit according to claim 1, further including a plurality of memory selector circuits to be selectively enabled in response to actuation of external selector means which is rendered operative in response to said plurality of memory circuits.

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