(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 March 2017 (30.03.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/053558 A1

(51) **International Patent Classification**:
H01L 21/768 (2006.01)

(21) **International Application Number**:
PCT/US2016/053099

(22) **International Filing Date**:
22 September 2016 (22.09.2016)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
62/232,027 24 September 2015 (24.09.2015) US

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,

[Continued on next page]

(54) **Title**: METHOD FOR BOTTOM-UP DEPOSITION OF A FILM IN A RECESSED FEATURE

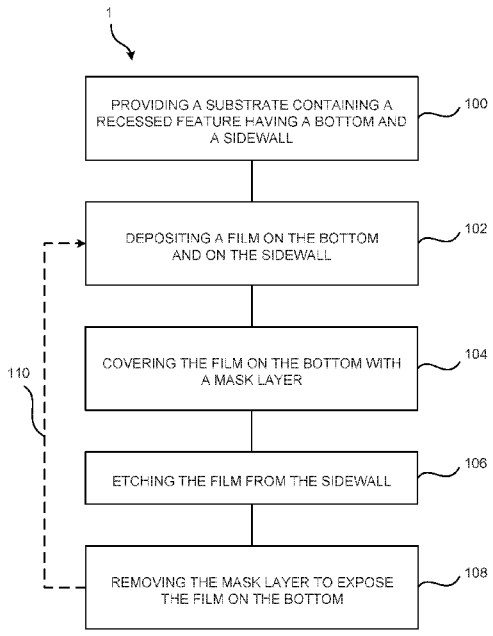

FIG. 1

(57) **Abstract**: Embodiments of the invention provide a processing method for bottom-up deposition of a film in a recessed feature. According to one embodiment, the method includes a) providing a substrate containing a recessed feature having a bottom and a sidewall, b) depositing a film on the bottom and on the sidewall of the recessed feature, and c) covering the film at the bottom of the recessed feature with a mask layer. The method further includes d) etching the film from the sidewall, and e) removing the mask layer to expose the film at the bottom of the recessed feature. Steps b) - e) may be repeated at least once until the film at the bottom of the recessed feature has a desired thickness. In one example, the recessed feature may be filled with the film.

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DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

METHOD FOR BOTTOM-UP DEPOSITION OF A FILM IN A RECESSED FEATURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority to United States Provisional Patent Application serial no. 62/232,027 filed on September 24, 2015, the entire contents of which are herein incorporated by reference.

FIELD OF INVENTION

[0002] The present invention relates to the field of semiconductor manufacturing and semiconductor devices, and more particularly, to a method for bottom-up deposition of a film in a recessed feature.

BACKGROUND OF THE INVENTION

[0003] As smaller transistors are manufactured, the critical dimension (CD) or resolution of patterned features is becoming more challenging to produce. Self-aligned patterning needs to replace overlay-driven patterning so that cost-effective scaling can continue even after EUV introduction. Patterning options that enable reduced variability, extend scaling and enhanced CD and process control are needed. Selective deposition of thin films is a key step in patterning in highly scaled technology nodes.

SUMMARY OF THE INVENTION

[0004] According to one embodiment, a processed method is disclosed. The method includes a) providing a substrate containing a recessed feature having a bottom and a sidewall, b) depositing a film on the bottom and on the sidewall of the recessed feature, and c) covering the film at the bottom of the recessed feature with a mask layer. The method further includes d) etching the film from the sidewall, and e) removing the mask layer to expose the film at the bottom of the recessed feature. Steps b) – e) may be repeated at least once until the film at the bottom of the recessed feature has a desired thickness. In one example, the recessed feature may be filled with the film.

[0005] According to another embodiment, the processing method includes a) providing a substrate containing a recessed feature having a bottom and a sidewall, b) depositing a film on the bottom and on the sidewall of the recessed feature, c) treating the film with a gas phase plasma to activate the film on the sidewall for faster etching than the film on the bottom of the recessed feature, and d) selectively etching the treated film from the sidewall. In one embodiment, the method further includes repeating steps b) – d) at least once until the film at

the bottom of the recessed feature has a desired thickness. In one example, the recessed feature may be filled with the film.

[0006] According to another embodiment, the processing method includes a) providing a substrate containing a recessed feature having a bottom and a sidewall, b) depositing a film on the bottom and on the sidewall of the recessed feature, and c) covering the film at the bottom of the recessed feature with a mask layer. The method further includes d) depositing a dopant film containing dopants in recessed feature, e) annealing the substrate to diffuse the dopants from the dopant film into the first film on the sidewall to activate the film on the sidewall for faster etching than the film on the bottom of the recessed feature, f) etching the dopant film and the film from the sidewall, and g) removing the dopant film and the mask layer from the film at the bottom of the recessed feature. In one embodiment, the method further includes repeating steps b) – f) at least once until the film at the bottom of the recessed feature has a desired thickness. In one example, the recessed feature may be filled with the film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0008] FIG. 1 is a process flow diagram for processing a substrate according to an embodiment of the invention;

[0009] FIGs. 2A-2F schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention;

[0010] FIG. 3 is process flow diagram for processing a substrate according to an embodiment of the invention;

[0011] FIGs. 4A-4E schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention;

[0012] FIG. 5 is process flow diagram for processing a substrate according to an embodiment of the invention; and

[0013] FIGs. 6A-6H schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

DETAILED DESCRIPTION OF SEVERAL EMBODIMENTS

[0014] Embodiments of the invention provide a method for bottom-up deposition of a film in a recessed feature.

[0015] FIG. 1 is a process flow diagram for processing a substrate according to an embodiment of the invention, and FIGs. 2A-2F schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

[0016] The process flow 1 includes, in 100, providing a substrate 200 containing a film 202 thereon having a recessed feature 204 with a bottom 203 and a sidewall 201. This is schematically shown in FIG. 2A. The recessed feature 204 can, for example, have a width 207 that is less than 200nm, less than 100nm, less than 50nm, less than 25nm, less than 20nm, or less than 10nm. In other examples, the recessed feature 204 can have a width 207 that is between 5nm and 10nm, between 10nm and 20nm, between 20nm and 50nm, between 50nm and 100nm, between 100nm and 200nm, between 10nm and 50nm, or between 10nm and 100nm. The width 207 can also be referred to as a critical dimension (CD). The recessed feature 204 can, for example, have a depth of 25nm, 50nm, 100nm, 200nm, or greater than 200nm.

[0017] According to one embodiment, the substrate 200 and the film 202, and therefore the bottom 203 and the sidewall 201, may contain the same material. For example, the material of the bottom 203 and the sidewall 201 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0018] According to another embodiment, the substrate 200 and the film 202, and therefore the bottom 203 and the sidewall 201, may contain different materials. The different materials may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may be selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0019] The recessed feature 204 may be formed using well-known lithography and etching processes. Although not shown in FIG. 2A, a patterned mask layer may be present on the field area 211 and defining the opening of the recessed feature 204.

[0020] The process flow 1 further includes, in 102, depositing a film 208 on the bottom 203 and on the sidewall 201. This is schematically shown in FIG. 2B. According to one embodiment, the film 208 may be deposited by atomic layer deposition (ALD). ALD can deposit very thin films with atomic level thickness control and excellent conformality over advanced raised and recessed features. In one example, the film 208 may be selected from the group consisting of a dielectric material, a metal, and a metal-containing material.

[0021] For example, the material of the film 208 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. According to another embodiment, the film 208 may be selected from the group consisting of a metal oxide film, a metal nitride film, a metal oxynitride film, a metal silicate film, and a combination thereof. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0022] In one example, the film 208 includes a metal oxide film that is deposited using ALD by a) pulsing a metal-containing precursor into a process chamber containing the substrate, b) purging the process chamber with an inert gas, c) pulsing an oxygen-containing precursor into the process chamber, d) purging the process chamber with an inert gas, and e) repeating a) – d) at least once.

[0023] In some examples, a thickness of the film 208 can be 10nm or less, 5nm or less, 4nm or less, between 1nm and 2nm, between 2nm and 4nm, between 4nm and 6nm, between 6nm and 8nm, or between 2nm and 6nm.

[0024] The process flow 1 further includes, in 104, covering the film 208 on the bottom 203 with a mask layer 206. This is schematically shown in FIG. 2C. The mask layer 206 can, for example, contain a photoresist, a hard mask, SiO_2, SiN, or a spin-on polymer. In one example, the mask layer 206 may be formed by filling or partially filling the recessed feature 204 with the material of the mask layer 206 and thereafter etching/removing the material from the recessed feature 204 until the mask layer 206 has a desired thickness on the bottom 203.

[0025] The process flow 1 further includes, in 106, etching the film 208 from the sidewall 201. As depicted in FIG. 2D, the etching removes the film 208 from the sidewall 201 but the mask layer 206 protects the film 208 under the mask layer 206 from etching. The etch gases and the etch conditions may be selected for providing efficient removal of the film 208 that is not protected by the mask layer 206.

[0026] The process flow 1 further includes, in 108, removing the mask layer 206 to expose the film 208 on the bottom 203 of the recessed feature 204. The process conditions may be selected for providing efficient removal of the mask layer 206. According to one embodiment, step 106 may be repeated following the step 108 to clean or thin the film 208.

[0027] According to one embodiment of the invention, as shown by process arrow 110, steps 102-108 may be repeated until the film 208 has a desired thickness. In one example, as depicted in FIG. 2F, steps 102-108 may be repeated until the recessed feature 204 is filled with the film 208.

[0028] FIG. 3 is process flow diagram for processing a substrate according to an embodiment of the invention, and FIGs. 4A-4D schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

[0029] The process flow 3 includes in 300, providing a substrate 400 containing a film 402 thereon having a recessed feature 404 with a bottom 403 and a sidewall 401. According to one embodiment, the substrate 400 and the film 402, and therefore the bottom 403 and the sidewall 401, may contain the same material. For example, the material of the bottom 403 and the sidewall 401 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0030] According to another embodiment, the substrate 400 and the film 402, and therefore the bottom 403 and the sidewall 401, may contain different materials. The different materials may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may be selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, or an ultra-low-k material. In one example, the high-k material may be selected from the group

consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0031] The recessed feature 404 may be formed using well-known lithography and etching processes. Although not shown in FIG. 4A, a patterned mask layer may be present on the field area 411 and defining the opening of the recessed feature 404.

[0032] The process flow 3 further includes, in 302, depositing a film 408 on the bottom 403 and on the sidewall 401. This is schematically shown in FIG. 4B. According to one embodiment, the film 408 may be deposited by ALD. In one example, the film 408 may be selected from the group consisting of a dielectric material, a metal, and a metal-containing material.

[0033] For example, the material of the film 408 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. According to another embodiment, the film 408 may be selected from the group consisting of a metal oxide film, a metal nitride film, a metal oxynitride film, a metal silicate film, and a combination thereof. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0034] In one example, the film 408 includes a metal oxide film that is deposited using ALD by a) pulsing a metal-containing precursor into a process chamber containing the substrate, b) purging the process chamber with an inert gas, c) pulsing an oxygen-containing precursor into the process chamber, d) purging the process chamber with an inert gas, and e) repeating a) – d) at least once.

[0035] In some examples, a thickness of the film 408 can be 10nm or less, 5nm or less, 4nm or less, between 1nm and 2nm, between 2nm and 4nm, between 4nm and 6nm, between 6nm and 8nm, or between 2nm and 6nm.

[0036] The process flow 3 further includes, in 304, treating the film 408 with a gas phase plasma to activate the film 408 on the field area 411 and the sidewall 401 for faster etching than the film 408 on the bottom 403 of the recessed feature 404. The treated film 413 is schematically shown in FIG. 4C. An isotropic gas phase plasma may be used to treat the film 408 and form the treated film 413. The isotropic characteristics of the gas phase plasma may be selected to preferentially activate the film 408 in the field area 411 and on the sidewall 401

for subsequent selective removal. Plasma activation of the film 408 can include disrupting the crystalline structure of the film 408 by the plasma species, thereby enabling faster etching of the treated film 413 in a subsequent selective etching process. In one example, the gas phase plasma can contain or consist of Ar gas.

[**0037**] The process flow 3 further includes, in 306, selectively etching the treated film 413 from the sidewall 401 and the field area 411. As depicted in FIG. 4D, the etching selectively removes the treated film 413 from the sidewall 401 and the field area 411 due to the higher etch rate of the treated film 413 on the sidewall 401 and the field area 411 than the film 408 on the bottom 403.

[**0038**] According some embodiments of the invention, as shown by process arrow 308, steps 302-306 may be repeated until the film 408 has a desired thickness. In one example, as depicted in FIG. 4E, steps 302-308 may be repeated until the recessed feature 404is filled with the film 412.

[**0039**] FIG. 5 is process flow diagram for processing a substrate according to an embodiment of the invention, and FIGs. 6A-6H schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

[**0040**] The process flow 5 includes, in 500, providing a substrate 600 containing a film 602 thereon having a recessed feature 604 with a bottom 603 and a sidewall 601. According to one embodiment, the substrate 600 and the film 602, and therefore the bottom 603 and the sidewall 601, may contain the same material. For example, the material of the bottom 603 and the sidewall 601 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[**0041**] According to another embodiment, the substrate 600 and the film 602, and therefore the bottom 603 and the sidewall 601, may contain different materials. The different materials may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may be selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. For example, the metal and the metal-

containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0042] The recessed feature 604 may be formed using well-known lithography and etching processes. Although not shown in FIG. 6A, a patterned mask layer may be present on the field area 211 and defining the opening of the recessed feature 604.

[0043] The process flow 5 further includes, in 502, depositing a film 608 on the bottom 603 and on the sidewall 601. This is depicted in FIG. 6B. According to one embodiment, the film 608 may be deposited by ALD. In one example, the film 608 may be selected from the group consisting of a dielectric material, a metal, and a metal-containing material.

[0044] For example, the material of the film 608 may be selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material. The dielectric material may selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material. In one example, the high-k material may be selected from the group consisting of HfO_2, ZrO_2, TiO_2, and Al_2O_3. According to another embodiment, the film 608 may be selected from the group consisting of a metal oxide film, a metal nitride film, a metal oxynitride film, a metal silicate film, and a combination thereof. For example, the metal and the metal-containing material may be selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.

[0045] In one example, the film 608 includes a metal oxide film that is deposited using ALD by a) pulsing a metal-containing precursor into a process chamber containing the substrate, b) purging the process chamber with an inert gas, c) pulsing an oxygen-containing precursor into the process chamber, d) purging the process chamber with an inert gas, and e) repeating a) – d) at least once.

[0046] In some examples, a thickness of the film 608 can be 10nm or less, 5nm or less, 4nm or less, between 1nm and 2nm, between 2nm and 4nm, between 4nm and 6nm, between 6nm and 8nm, or between 2nm and 6nm.

[0047] The process flow 5 further includes, in 504, covering the film 608 at the bottom 603 of the recessed feature 604 with a mask layer 606. This is depicted in FIG. 6C. The mask layer 606 can, for example, contain a photoresist, a hard mask, SiO_2, or SiN.

[0048] The process flow 5 further includes, in 506, depositing a dopant film 609 in the recessed feature 604. This is depicted in FIG. 6D. The dopant film 609 can include an oxide layer (e.g., SiO_2), a nitride layer (e.g., SiN), an oxynitride layer (e.g., SiON), or a combination of two or more thereof. The dopant film 609 can include one or more dopants

from Group IIIA of the Periodic Table of the Elements: boron (B), aluminum (Al), gallium (Ga), indium (In), and thallium (Tl); and Group VA: nitrogen (N), phosphorous (P), arsenic (As), antimony (Sb), and bismuth (Bi). According to some embodiments, the dopant film 609 can contain low dopant levels, for example between about 0.5 and about 5 atomic % dopant. According to other embodiments, the dopant film 609 can contain medium dopant levels, for example between about 5 and about 20 atomic % dopant. According to yet other embodiments, the dopant film 609 can contain high dopant levels, for example greater than 20 atomic percent dopant.

[0049] The process flow 5 further includes, in 508, annealing the substrate to diffuse a dopant from the dopant film 609 into the film 608 on the sidewall 601 to activate the film 608 on the sidewall 601 for faster etching than the film 608 on the bottom 603 of the recessed feature 604. It is contemplated that the dopants disrupt the crystalline structure of the film 608, thereby enabling fast etching of the film 608 in a subsequent selective etching process.

[0050] The process flow 5 further includes, in 510, etching the dopant film 609 and the film 608 from the sidewall 601 and the field area 611. As depicted in FIG. 6E, the etching removes the dopant film 609 and the field area 611from the sidewall 601 but the mask layer 606 protects the film 608 under the mask layer 606 from etching. The etch gases and the etch conditions may be selected for providing efficient removal of the dopant film 609 and the film 608 that is not protected by the mask layer 606. Step 510 may be performed in one or more etching steps using one or more etching recipes.

[0051] The process flow 5 further includes, in 512, removing the mask layer 606 from the film 608 on the bottom 603 of the recessed feature 604. This is depicted in FIG. 6G.

[0052] According to one embodiment of the invention, as shown by process arrow 514, steps 502-512 may be repeated until the film 608 has a desired thickness. In one example, as depicted in FIG. 6H, the recessed feature 604 may be filled with film 608.

[0053] A plurality of embodiments for bottom-up deposition of a film in a recessed feature have been described. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms that are used for descriptive purposes only and are not to be construed as limiting. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. It is therefore

intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A processing method, comprising:
   a) providing a substrate containing a recessed feature having a bottom and a sidewall;
   b) depositing a film on the bottom and on the sidewall;
   c) covering the film at the bottom with a mask layer;
   d) etching the film from the sidewall; and
   e) removing the mask layer to expose the film at the bottom.
2. The method of claim 1, further comprising
   repeating steps b) – e) until the film has a desired thickness in the recessed feature.
3. The method of claim 1, further comprising
   repeating steps b) – e) until the recessed feature is filled with the film.
4. The method of claim 1, wherein the bottom and the sidewall contain the same material.
5. The method of claim 4, wherein the material is selected from the group consisting of silicon, germanium, silicon germanium, a dielectric material, a metal, and a metal-containing material.
6. The method of claim 5, wherein the dielectric material is selected from the group consisting of SiO_2, SiON, SiN, a high-k material, a low-k material, and an ultra-low-k material.
7. The method of claim 5, wherein the metal and metal-containing material are selected from the group consisting of Cu, Al, Ta, Ru, TaN, TaC, and TaCN.
8. The method of claim 1, wherein the bottom and the sidewall contain different materials.
9. A processing method, comprising:
   a) providing a substrate containing a recessed feature having a bottom and a sidewall;
   b) depositing a film on the bottom and on the sidewall of the recessed feature;
   c) treating the film with a gas phase plasma to activate the film on the sidewall for faster etching than the film on the bottom; and
   d) etching the treated film from the sidewall.
10. The method of claim 9, further comprising
    repeating steps b) – d) at least once until the film has a desired thickness in the recessed feature.

11. The method of claim 9, further comprising

repeating steps b) – d) until the recessed feature is filled with the film.

12. The method of claim 9, wherein the bottom and the sidewall contain the same material.

13. The method of claim 9, wherein the bottom and the sidewall contain different materials.

14. A processing method, comprising:

a) providing a substrate containing a recessed feature having a bottom and a sidewall;

b) depositing a film on the bottom and on the sidewall;

c) covering the film at the bottom with a mask layer;

d) depositing a dopant film in recessed feature;

e) annealing the substrate to diffuse a dopant from the dopant film into the film on the sidewall to activate the film on the sidewall for faster etching than the film on the bottom;

f) etching the dopant film and the film from the sidewall; and

g) removing the mask layer from the film on the bottom.

15. The method of claim 14, further comprising

repeating steps b) – g) at least once until the film has a desired thickness in the recessed feature.

16. The method of claim 14, further comprising

repeating steps b) – g) until the recessed feature is filled with the film.

17. The method of claim 14, wherein the bottom and the sidewall contain the same material.

18. The method of claim 14, wherein the bottom and the sidewall contain different materials.

19. The method of claim 14, wherein the dopant is selected from the group consisting of boron (B), aluminum (Al), gallium (Ga), indium (In), thallium (Tl), nitrogen (N), phosphorous (P), arsenic (As), antimony (Sb), and bismuth (Bi).

20. The method of claim 14, wherein the dopant film includes an oxide layer, a nitride layer, an oxynitride layer, or a combination thereof.

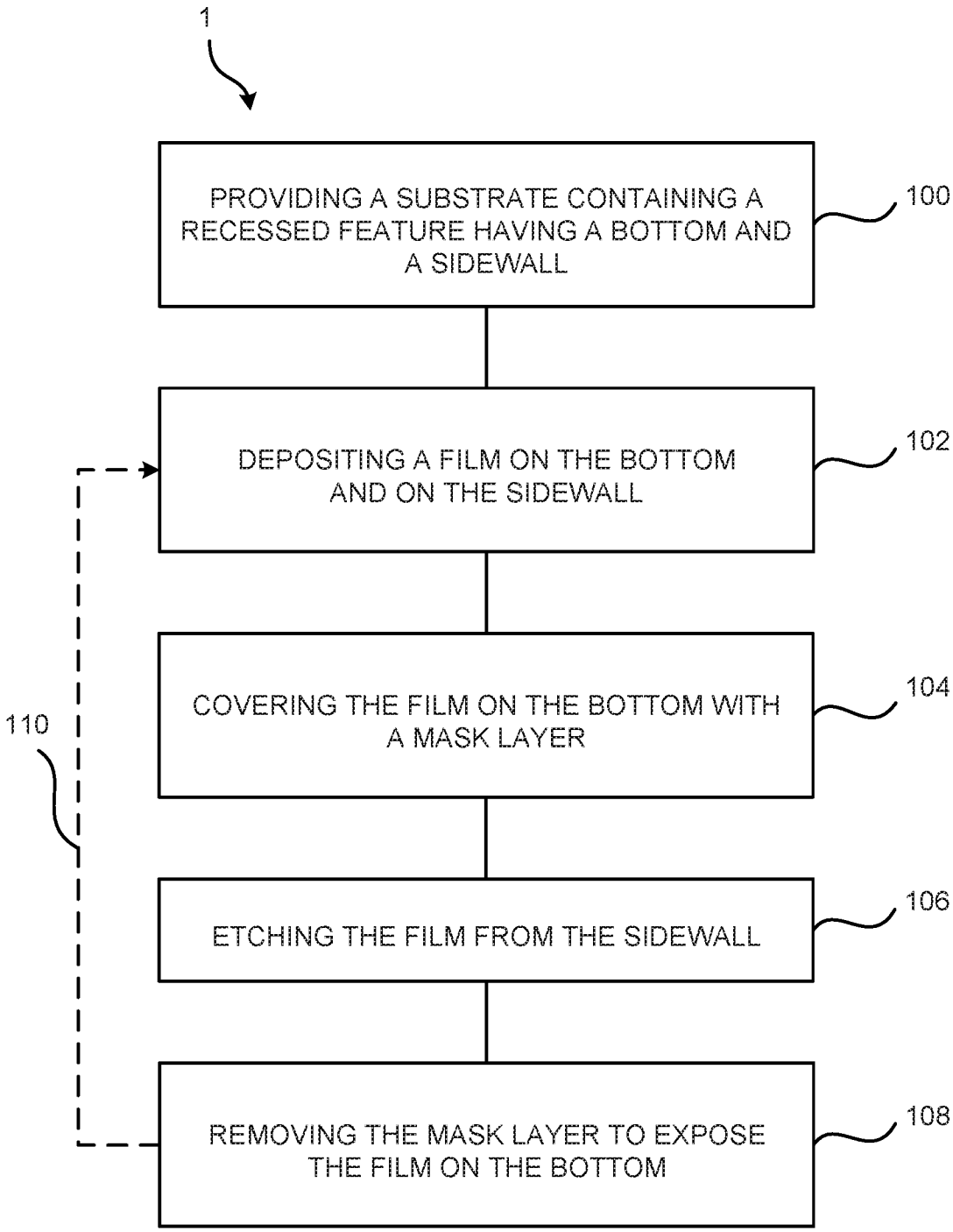

1
PROVIDING A SUBSTRATE CONTAINING A RECESSED FEATURE HAVING A BOTTOM AND A SIDEWALL
100
DEPOSITING A FILM ON THE BOTTOM AND ON THE SIDEWALL
102
COVERING THE FILM ON THE BOTTOM WITH A MASK LAYER
104
110
ETCHING THE FILM FROM THE SIDEWALL
106
REMOVING THE MASK LAYER TO EXPOSE THE FILM ON THE BOTTOM
108

FIG. 1

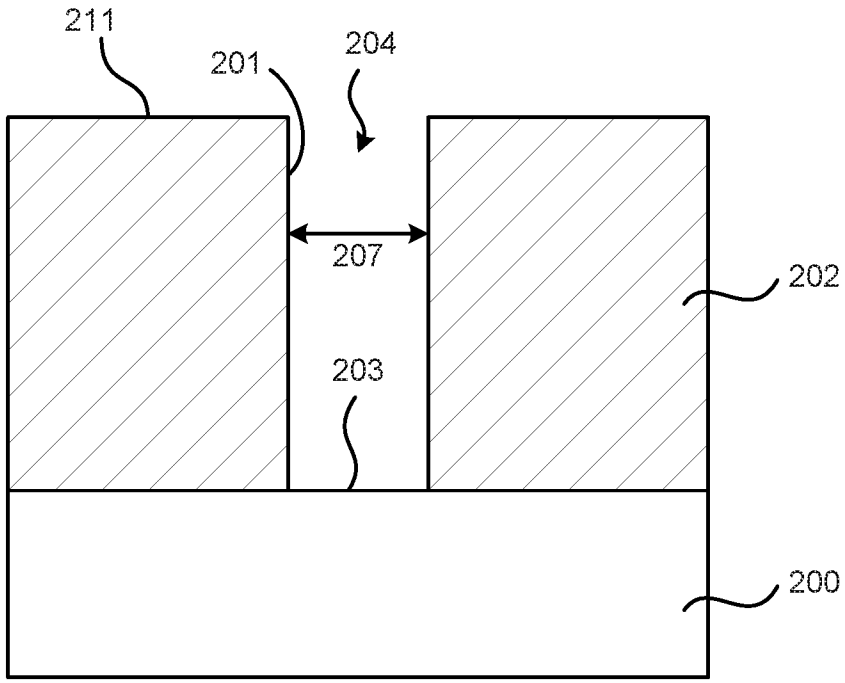


FIG. 2A

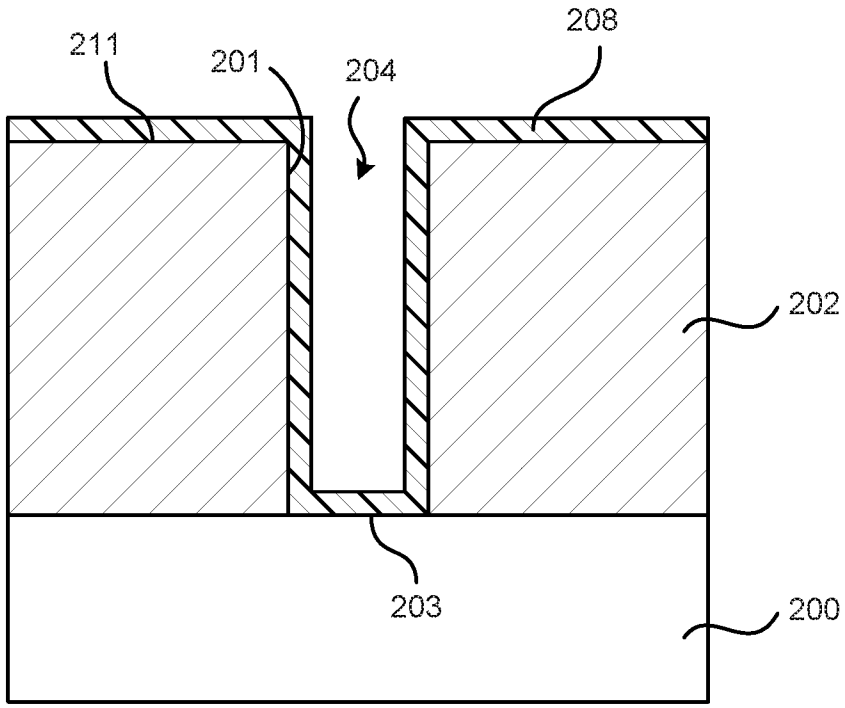


FIG. 2B

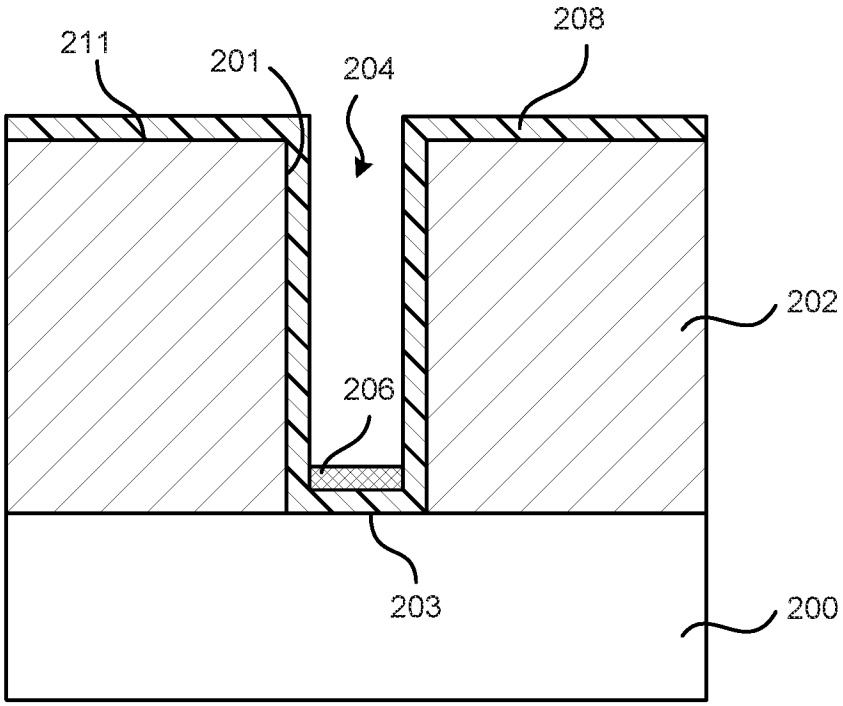


FIG. 2C

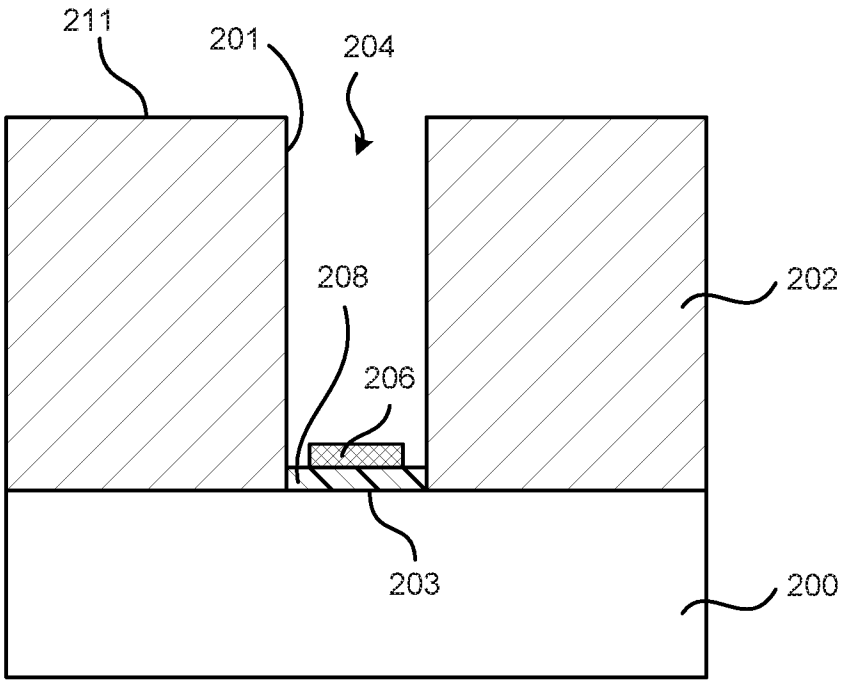


FIG. 2D

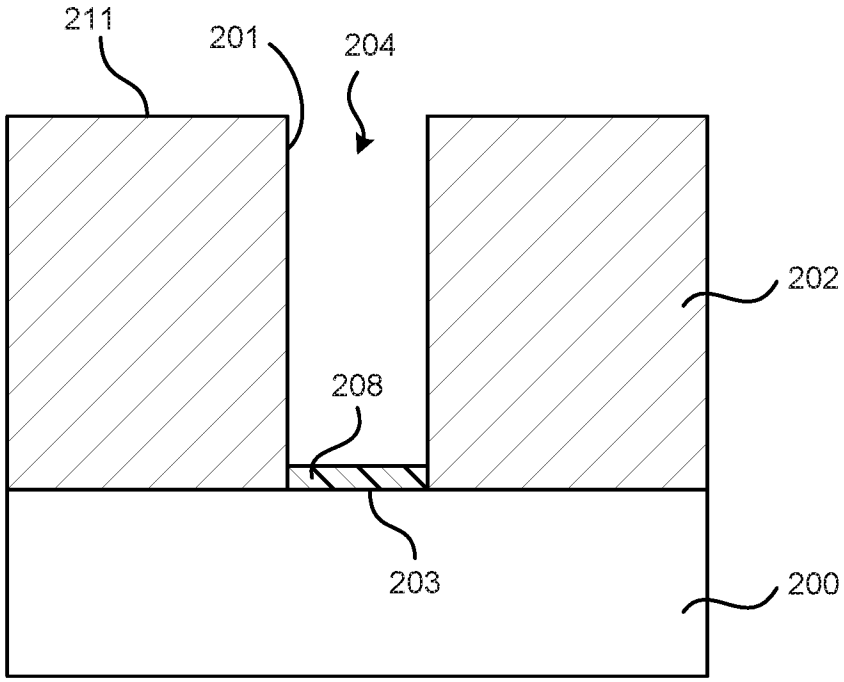


FIG. 2E

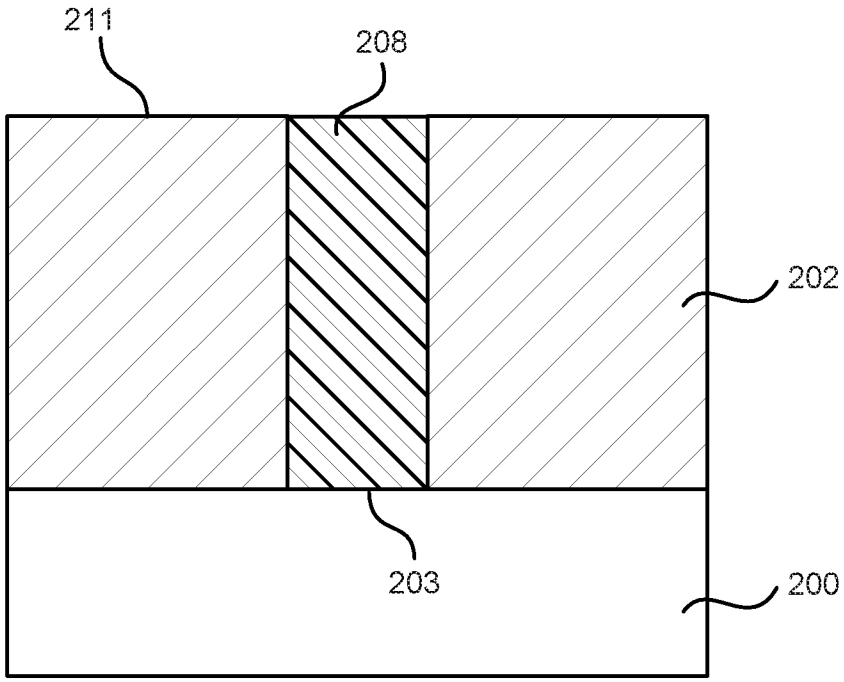


FIG. 2F

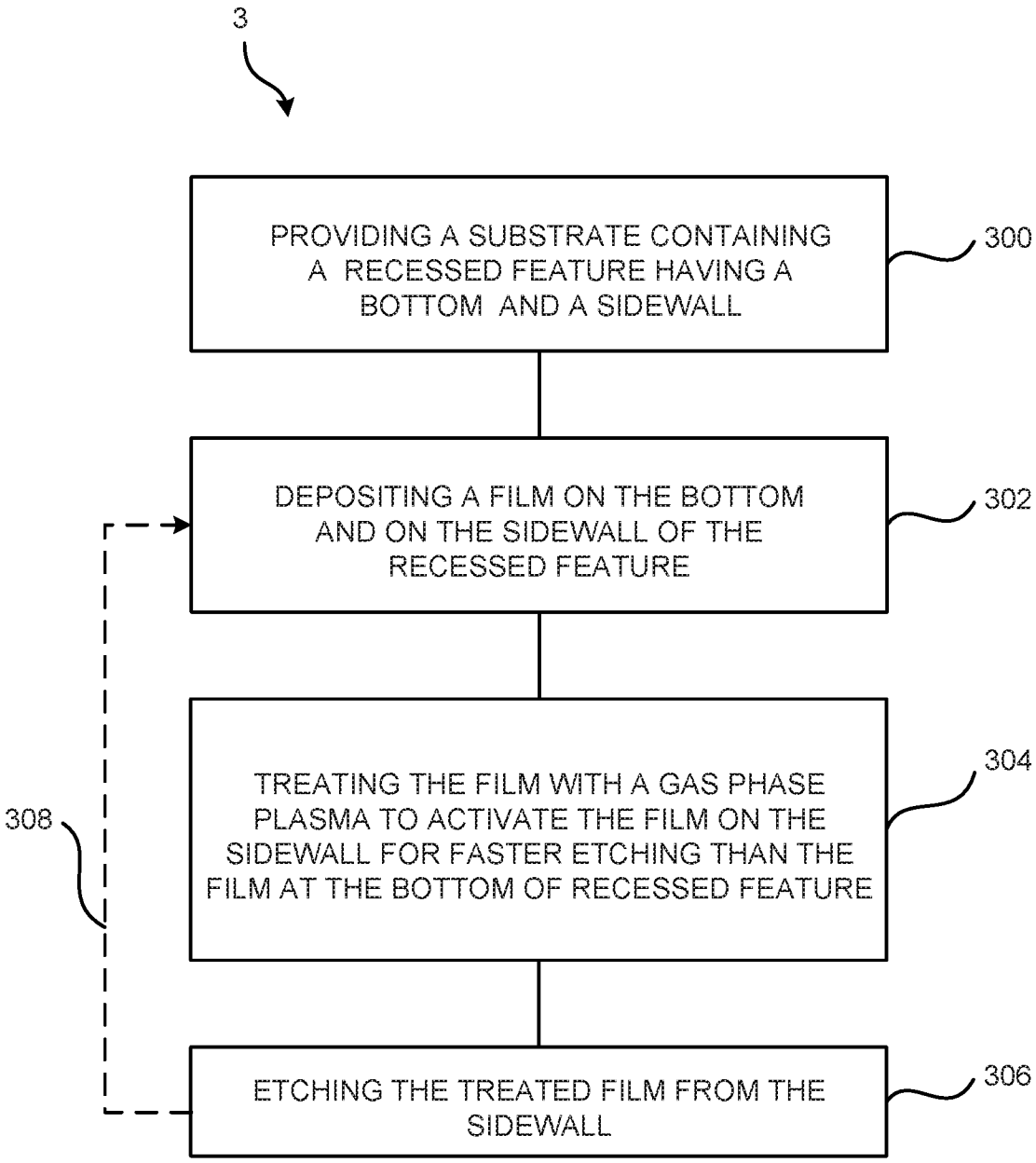

3
PROVIDING A SUBSTRATE CONTAINING A RECESSED FEATURE HAVING A BOTTOM AND A SIDEWALL
300
DEPOSITING A FILM ON THE BOTTOM AND ON THE SIDEWALL OF THE RECESSED FEATURE
302
TREATING THE FILM WITH A GAS PHASE PLASMA TO ACTIVATE THE FILM ON THE SIDEWALL FOR FASTER ETCHING THAN THE FILM AT THE BOTTOM OF RECESSED FEATURE
304
308
ETCHING THE TREATED FILM FROM THE SIDEWALL
306

FIG. 3

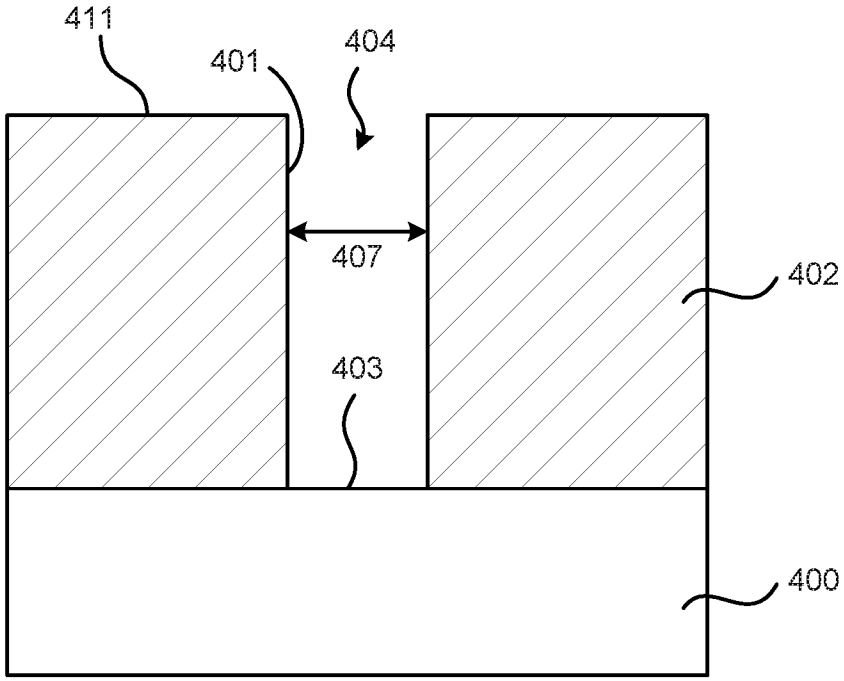


FIG. 4A

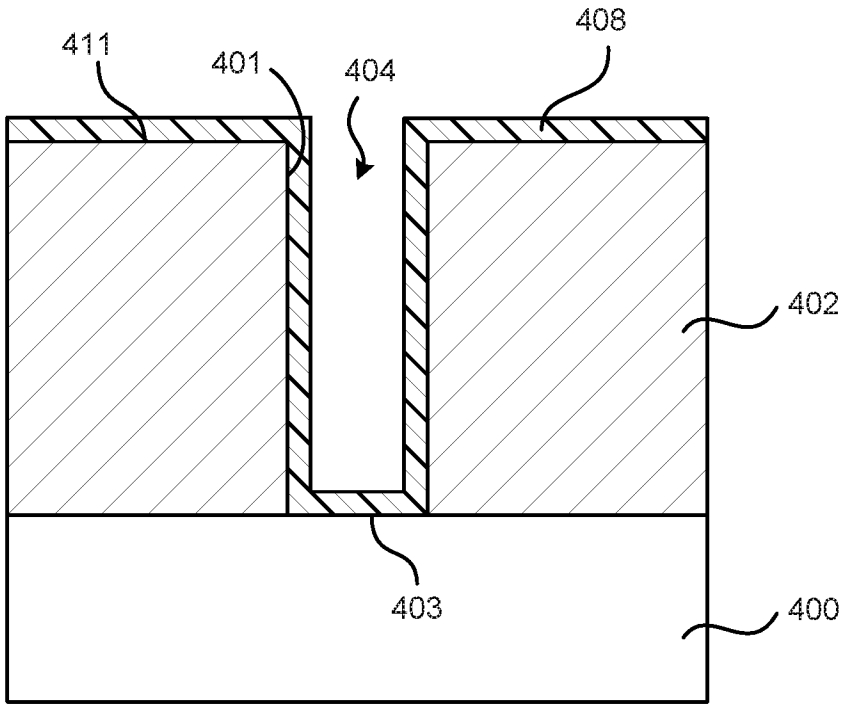


FIG. 4B

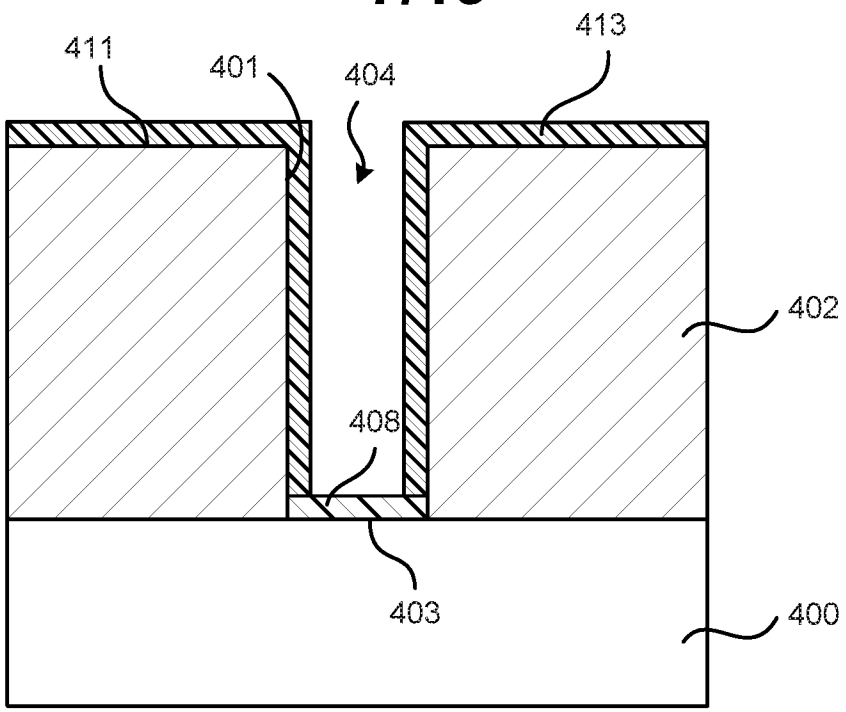


FIG. 4C

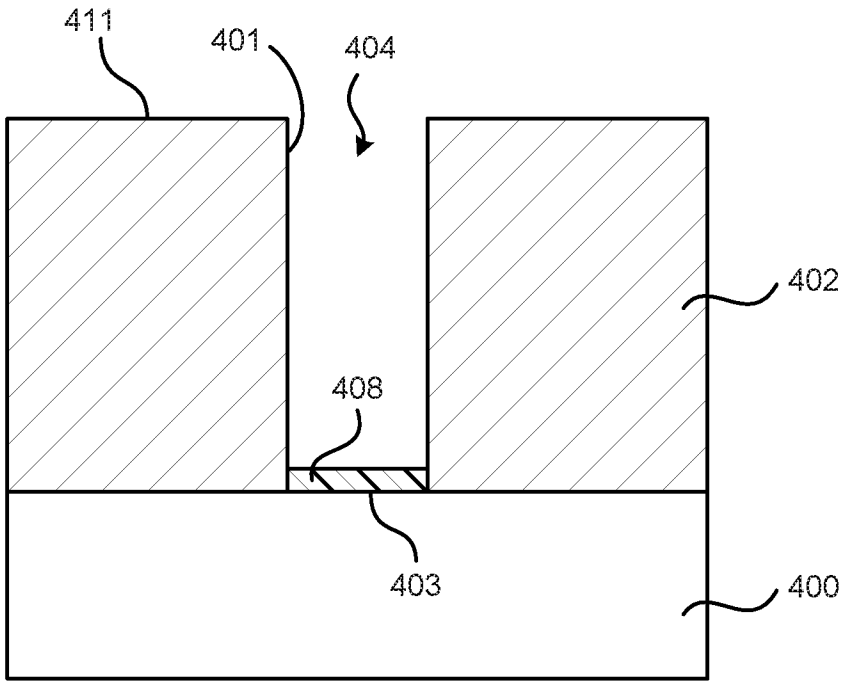


FIG. 4D

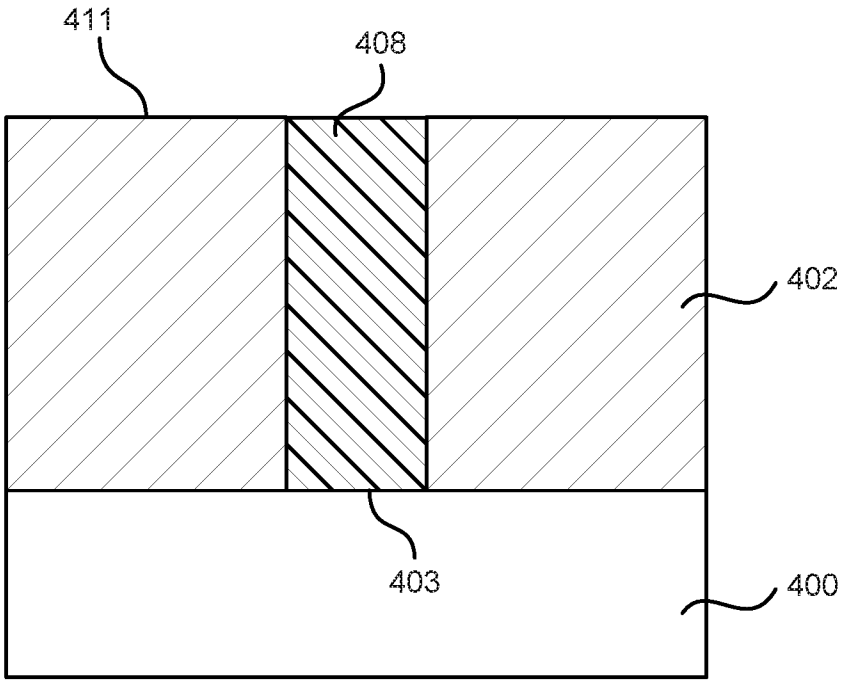
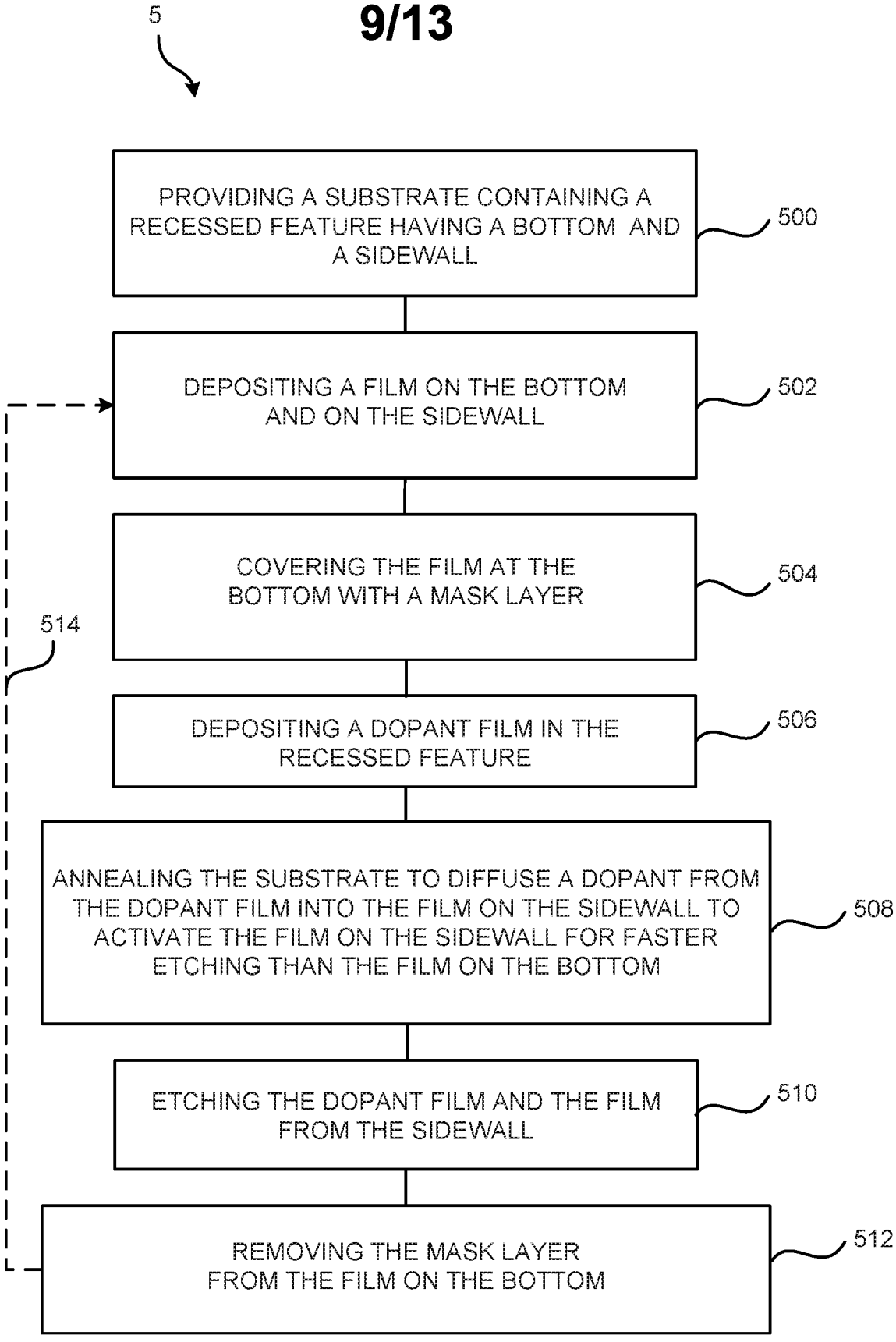


FIG. 4E

FIG. 8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PROVIDING A SUBSTRATE CONTAINING A RECESSED FEATURE HAVING A BOTTOM AND A SIDEWALL
500
DEPOSITING A FILM ON THE BOTTOM AND ON THE SIDEWALL
502
COVERING THE FILM AT THE BOTTOM WITH A MASK LAYER
504
514
DEPOSITING A DOPANT FILM IN THE RECESSED FEATURE
506
ANNEALING THE SUBSTRATE TO DIFFUSE A DOPANT FROM THE DOPANT FILM INTO THE FILM ON THE SIDEWALL TO ACTIVATE THE FILM ON THE SIDEWALL FOR FASTER ETCHING THAN THE FILM ON THE BOTTOM
508
ETCHING THE DOPANT FILM AND THE FILM FROM THE SIDEWALL
510
REMOVING THE MASK LAYER FROM THE FILM ON THE BOTTOM
512

FIG. 5

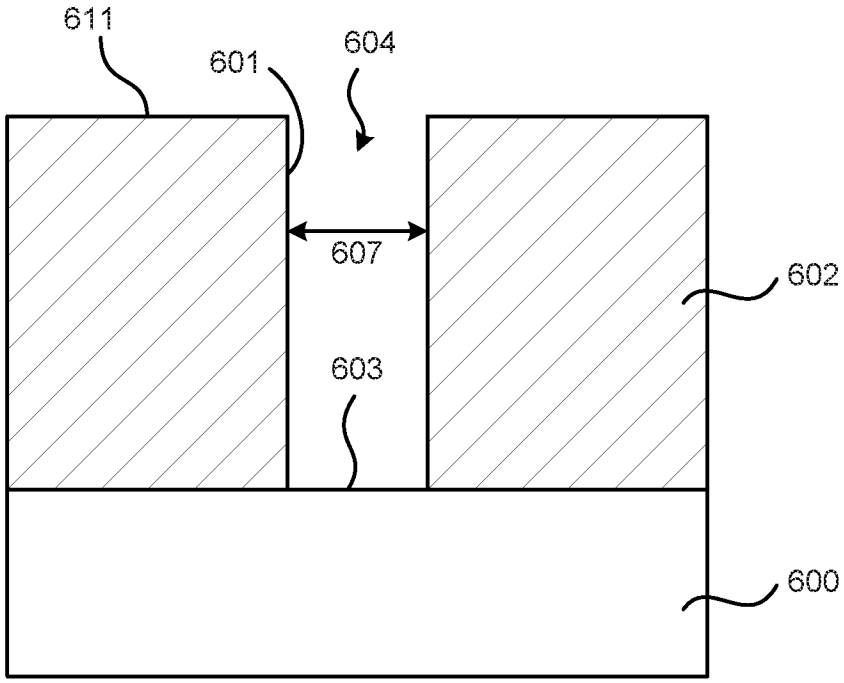

FIG. 6A

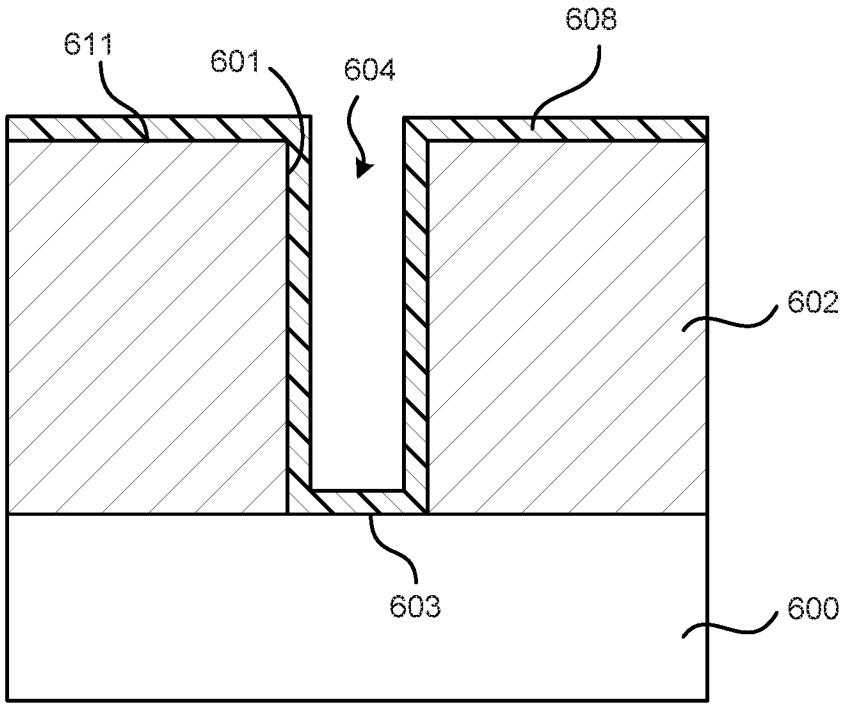

FIG. 6B

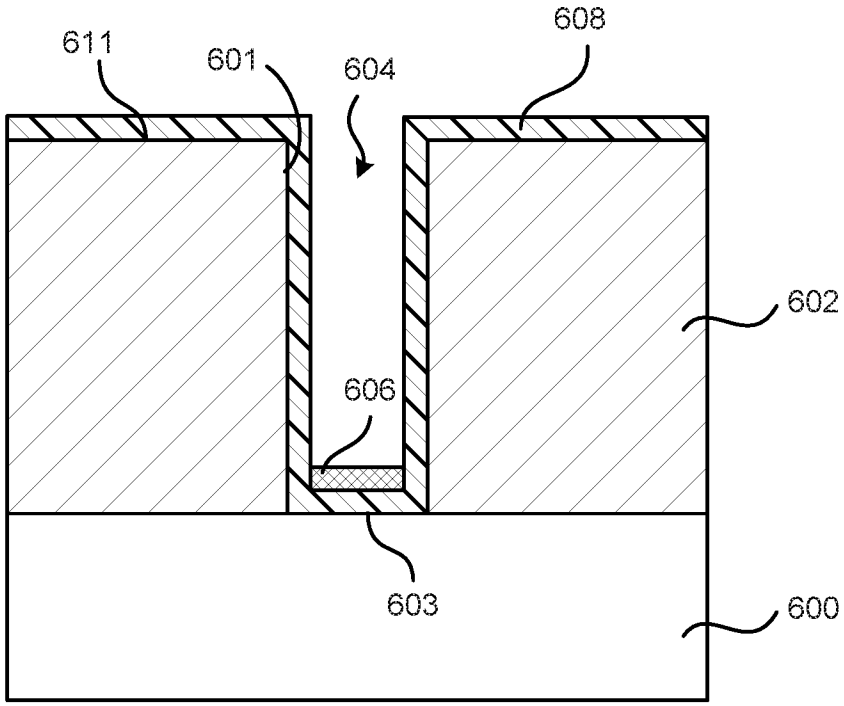
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FIG. 6C

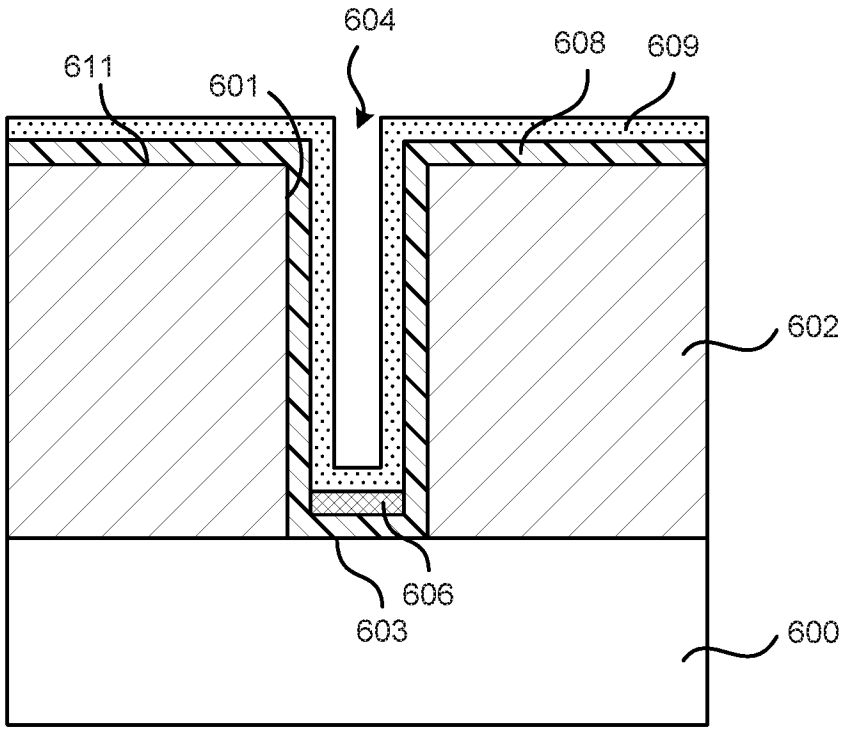
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FIG. 6D

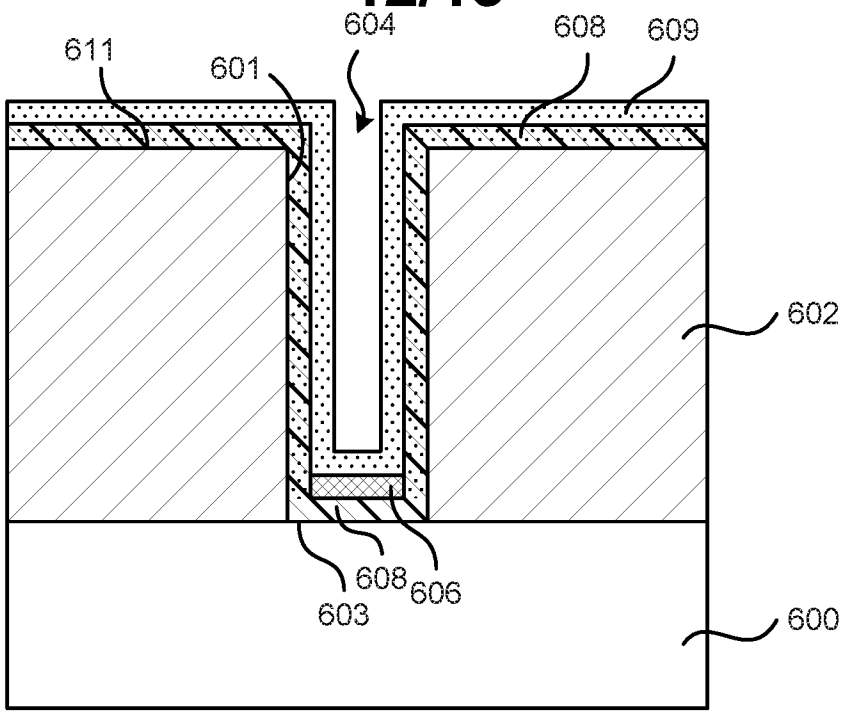
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FIG. 6E

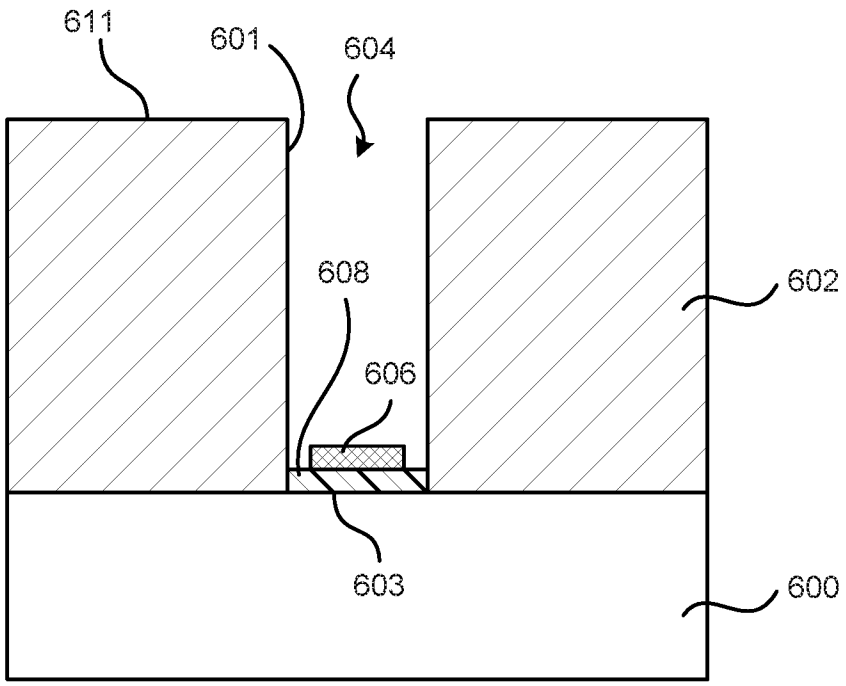
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FIG. 6F

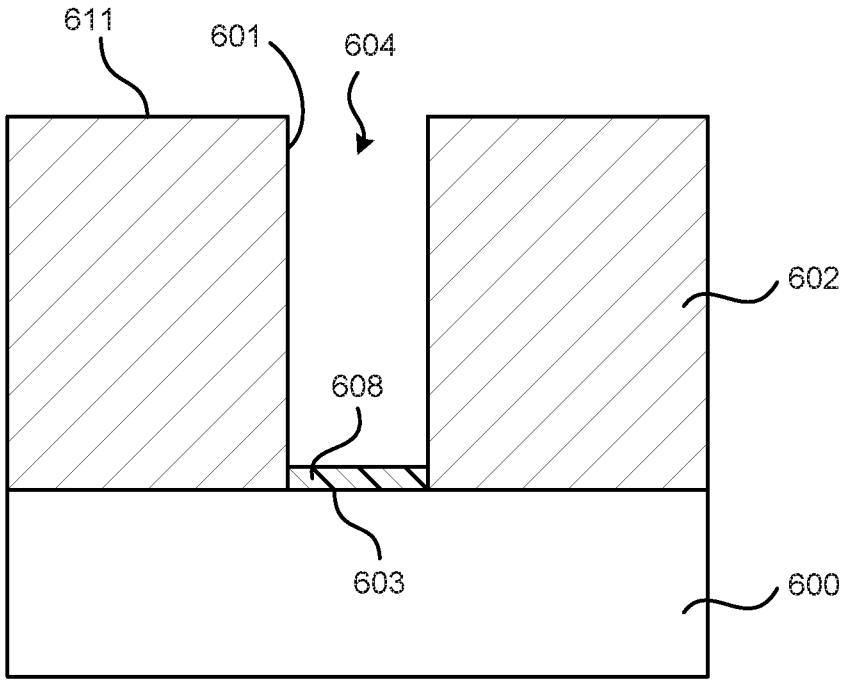

FIG. 6G

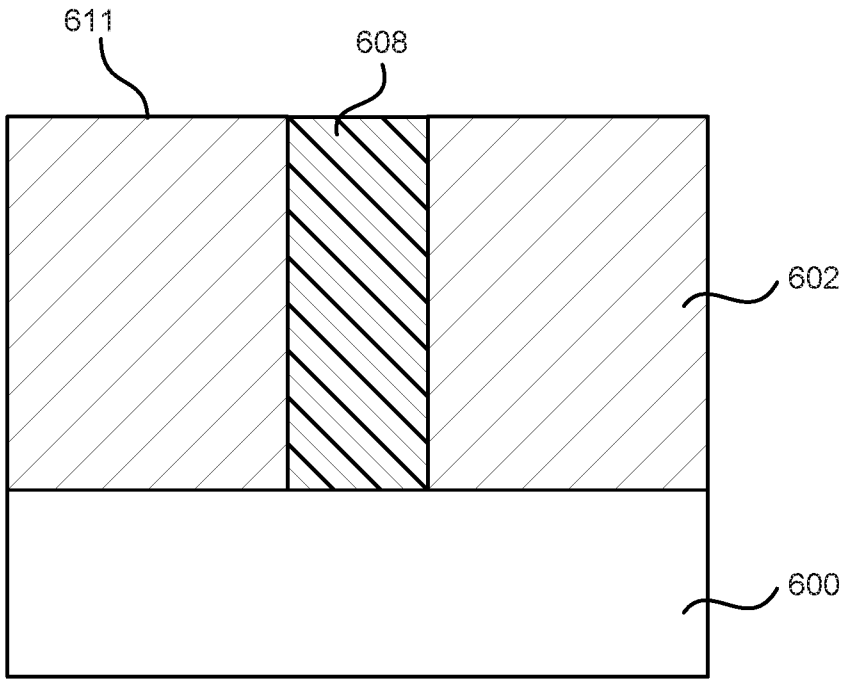

FIG. 6H

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053099

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/268; H01L 21/20; H01L 21/469; H01L 21/336; H01L 21/8242; H01L 21/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: deposition, film, recess, sidewall, mask layer, etching, plasma, doping

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005-0112839 A1 (YUNG-HSIEN WU) 26 May 2005 See abstract, paragraphs [0021]-[0025], claims 1-7 and figures 2A-2H.	1-20
A	US 2005-0272201 A1 (CHENG KANGGUO et al.) 08 December 2005 See abstract, paragraphs [0015]-[0024], claims 1-16 and figures 4-12.	1-20
A	US 2013-0230987 A1 (NERISSA DRAEGER et al.) 05 September 2013 See abstract, paragraphs [0032]-[0037], claims 1-10 and figure 1.	1-20
A	KR 10-0744071 B1 (HYNIX SEMICONDUCTOR INC.) 30 July 2007 See abstract, paragraphs [0021]-[0037], claims 1, 2, 8 and figures 3a-3f.	1-20
A	US 7148155 B1 (RAIHAN M. TARAFDAR et al.) 12 December 2006 See abstract, column 5, line 43 - column 7, line 2, claim 1 and figures 2-3B.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 January 2017 (05.01.2017)	**05 January 2017 (05.01.2017)**

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Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/053099

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		TW I320208 A	01/02/2010
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		US 7790633 B1	07/09/2010