

Jan. 4, 1966

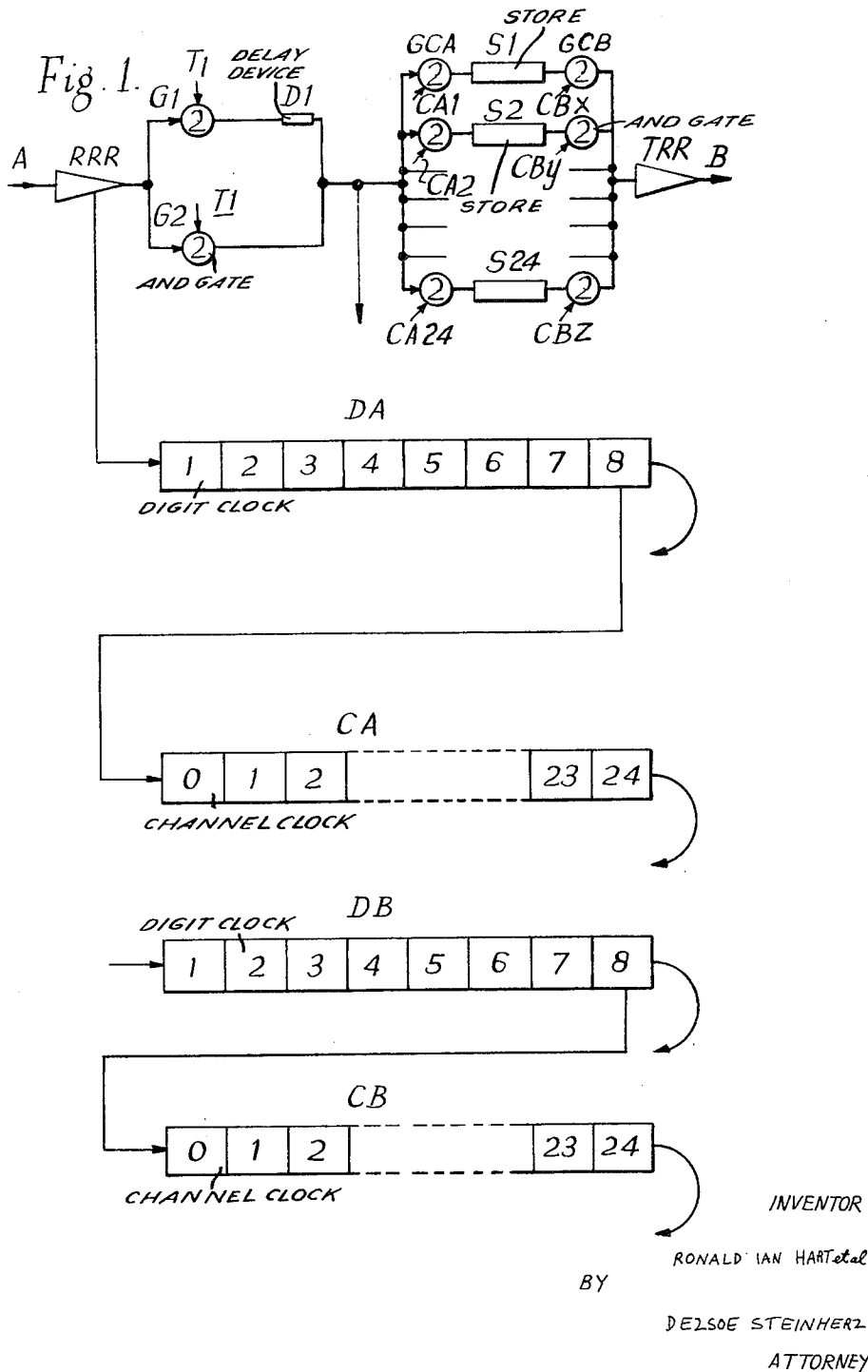
R. I. HART ETAL

3,227,811

INTERCONNECTING ARRANGEMENT FOR TIME DIVISION MULTIPLEX
ELECTRICAL SIGNALLING SYSTEMS OF THE SAME
NOMINAL FREQUENCY

Filed Feb. 23, 1962

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Fig. 2.

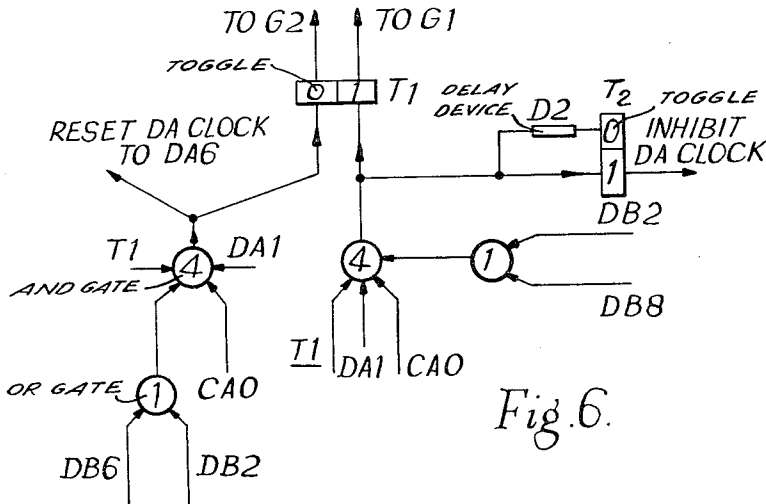
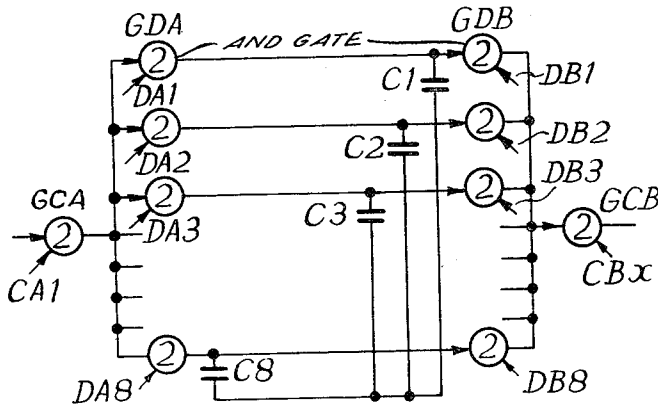


Fig. 6.

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Fig. 3.

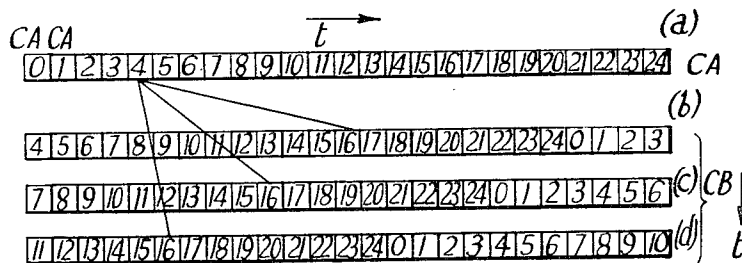


Fig. 4.

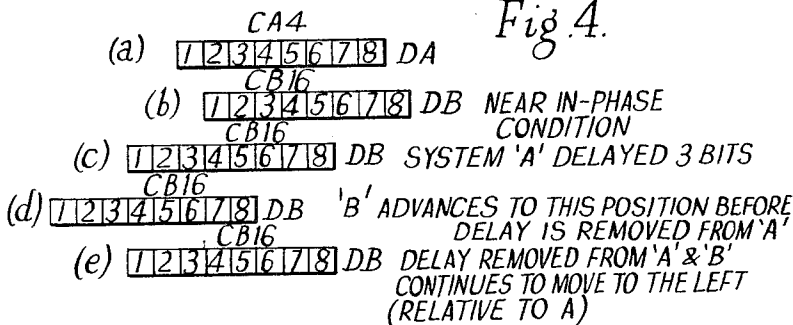
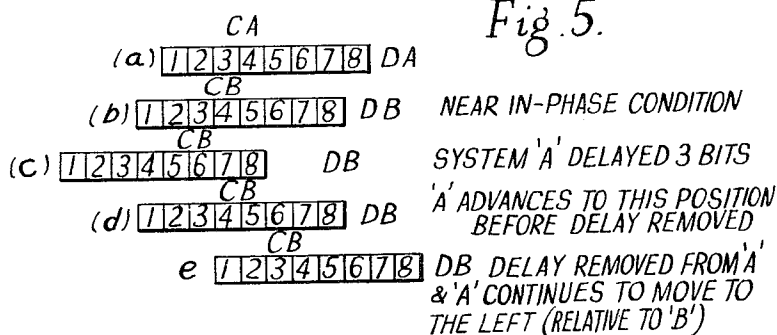


Fig. 5.



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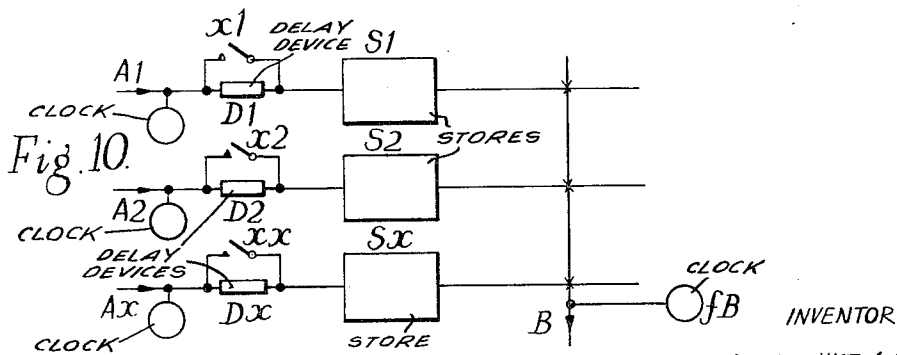
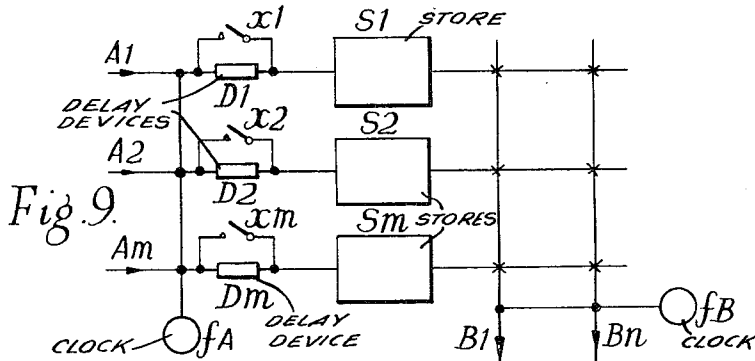
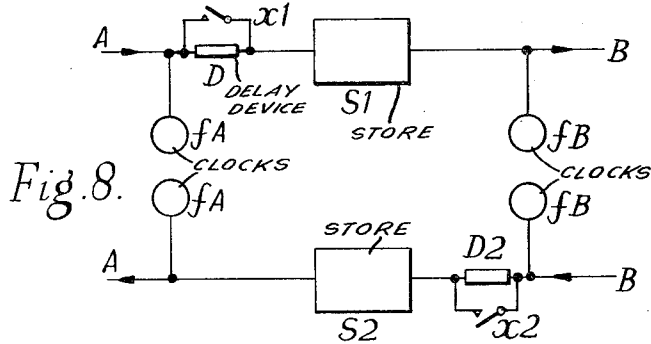
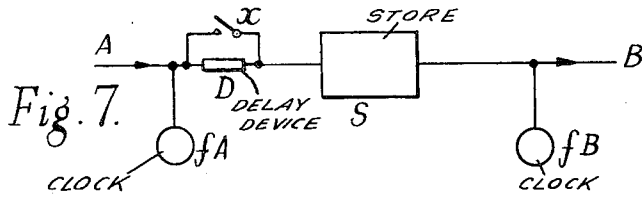
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4 Sheets-Sheet 4



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3,227,811

INTERCONNECTING ARRANGEMENT FOR TIME DIVISION MULTIPLEX ELECTRICAL SIGNALING SYSTEMS OF THE SAME NOMINAL FREQUENCY

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Claims priority, application Great Britain, Feb. 23, 1961, 6,706/61

6 Claims. (Cl. 179-15)

The present invention relates to electrical signalling systems and is more particularly concerned with pulse communication systems operating on a time division multiplex basis, for instance of the type known as pulse code modulation. For satisfactory operation of such systems, it is found necessary in practice to employ one of the channels for synchronisation purposes and this operates in conjunction with the frequency control or so-called clock system.

In any large scale application of such pulse systems, the need will certainly arise for interconnecting different systems which accordingly have their own individual clock systems. Though the accuracy and stability of the timing may be quite high, it is inevitable that long term drift will occur and this will clearly produce difficulties when a number of systems are interconnected, since the various clock systems must necessarily be independent.

One possible method of overcoming the difficulty would be to demodulate the channels of each system, interconnect the channels at audio frequency and then re-code the channels on to the multiplex system. This involves a good deal of additional equipment and also is objectionable from the technical point of view in that it adds to the quantising noise, and hence it is generally preferable to interconnect the pulse systems directly without demodulation.

It is also likely to occur in practice that channels in a certain time position in one system will need to be connected to channels in a different time position in another system and this makes the use of some form of storage essential. Since, as has already been stated, it is impossible in practice to maintain two systems in exact synchronism over a long period, it will follow that in due course of time one system will gain on the other and this will mean that the interval between the instant at which the information is fed into the store and the instant at which it is withdrawn for re-transmission will gradually decrease to zero and it is clear that as long as the two systems are practically in phase, there is a danger of information being lost. If the difference between the two clocks is comparatively large, the in-phase condition will occur comparatively frequently but will not last for very long on each occasion. If the systems are very close to synchronism, the difficulty will only arise at much longer intervals but will persist for much longer before it clears itself. In either case, the danger of information being lost is so great as to be intolerable in practice and it is highly important to prevent it as far as possible. The chief object of the invention is to provide arrangements for dealing with the conditions outlined above so that two or more independent multiplex systems having slightly different frequencies may be arranged to work together satisfactorily without any appreciable loss of information.

According to the invention, this is achieved by arranging for a sudden change to be made in the length of the storage period when the storage time approaches zero. Conveniently a delay is introduced into one system

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when the near in-phase condition is about to occur whereby the imminent conflict is avoided and then subsequently when the two systems have in effect moved clear of the dangerous in-phase condition, the delay is removed so that the previous relationship is restored.

The invention will be better understood from the following description of one method of carrying it into effect which should be taken in conjunction with the accompanying drawings comprising FIGURES 1-10. FIGURE 1 shows schematically the equipment provided for the interconnection of two systems A and B, FIGURE 2 shows one of the stores with its associated gates, FIGURE 3 shows possible time relationships between the two systems at different instants, FIGURE 4 shows the manner of application of the invention when system B is running slightly faster than system A, FIGURE 5 shows similarly how the invention operates when A is running faster than B, FIGURE 6 shows the logical circuits employed for introducing and removing the delay, and FIGURES 7-10 show schematically various interconnecting arrangements for the systems which are readily possible.

Referring now particularly to FIGURE 1, it is assumed that each system caters for 25 channels, of which channel 25 is the synchronising channel and that each appearance of a channel involves 8 digits; consequently a complete cycle or frame will represent 200 elements or bits. The A system is controlled by the digit clock DA producing the pulses DA1-DA8 corresponding to the digits for each channel, and also by the channel clock CA operated therefrom and producing pulses CA0-CA24 of which CA0 relates to the synchronising channel. It will be appreciated that if the sampling frequency is 8,000 c./s., which is a convenient value in practice, particularly if the information being transmitted is speech, the bit frequency will be 1.6 mc./s.

The incoming signals from system A are fed to the receive regenerative repeater RRR and then pass to the gates G1 and G2 which are controlled by the toggle or flip-flop T1 as will be explained more fully shortly. It will be understood that in these circumstances either gate G1 or gate G2 is always open and it will be seen that the circuit over gate G1 includes the delay device D1 which conveniently introduces a delay of three bits. This figure is arbitrary and the choice of the most satisfactory value depends upon the number of digits per channel and the minimum allowable storage time. The signals then pass to the gates GCA which are controlled respectively from the channel clock by the pulses CA1-CA24 and information is thus passed to the stores S1, S2 . . . S24. No store is provided for the synchronising channel since the synchronising information is re-inserted for system B.

FIGURE 2 shows one form of channel store which makes use of capacitors C1, C2, C3 . . . C8 as shown and the digits are routed into the appropriate stores by way of the gates GDA operated by the digit clock pulses DA1-DA8. The clock DA is kept in frequency synchronism with the incoming information by means of 1.6 mc./s. strobe pulses derived from the regenerative repeater and the strobe pulses are also used in known manner to control the toggles. Clock DA drives clock CA and both clocks are kept in phase synchronism with the incoming information by means of the so-called synchronism searching circuit for instance of the type disclosed in the application of Geoffrey F. Croft, Serial No. 156,235, filed December 1, 1961.

The clocks are shown conventionally as comprising ring counters driven by the strobe pulses but any suitable source of clock pulses may be employed. The stored information is read out by way of the gates GDB and

GCB corresponding to digits and channels respectively when required for transmission over system B by way of the transmit regenerative repeater TRR. The gates GCB, although under the control of clock CB, are in fact operated in a variable sequence indicated by the references *x*, *y* and *z* in order to achieve the required cross-connection of channels. The method of producing this result is well understood by those skilled in the art and forms no part of the present invention. In essence it involves suitable choice of the connection to the gates GCB. It will be appreciated that means may be provided for varying the channels which are interconnected so as to permit a selective connection to be made for instance under the control of a dial at a telephone subscriber's instrument.

Referring now to FIG. 3, the top line *a* shows a frame of channels belonging to system A which are connected in the manner described above to system B. The succeeding lines *b*, *c*, *d* show frames of the B system as they occur for various time intervals. The horizontal time scale is 125 μ s for each frame and the time interval between the different series of B frames may be of the order of 2 minutes. It will be assumed that channel 4A is communicating with channel 16B as indicated by the arrows and that the B system is gaining on the A system. Initially there is quite an appreciable time interval between information being presented to the store by system A and being read out for transmission over system B. It will be seen that when the conditions of frame *d* arise, the in-phase condition has practically been reached and some action must be taken if loss of an appreciable amount of the information is to be avoided.

This is shown in greater detail in FIGURE 4 in which the channels concerned have been divided up into their individual bits which are drawn so as to have significant time relationships. *a* represents channel 4 of system A and *b* represents channel 16 of system B, and the position has been reached in which digit DB1 coincides with digit DA2. The three-bit delay which is assumed to be provided is then switched into system A which may be regarded as advancing system B by three bits so that the relative positions are represented by *a* and *c*. System B continues to gain on system A until the position of *d* is reached in which DB6 coincides with DA1. Thereupon a further switching operation is produced to cut out the three-bit delay and the position of DB is then as in *e*. The difficulty arising from the near in-phase condition has now been passed and the two systems can run straightforwardly until the next occasion on which phase coincidence approaches. It will be understood that when the three-bit delay is introduced, the A clock must be altered accordingly and similarly the previous clock conditions must be restored when the delay is subsequently cut out.

FIGURE 5 shows similar conditions in the case where system A is running faster than system B. This case could obviously be dealt with on precisely similar lines by arranging for a three-bit delay to be introduced into system B. It is readily possible however, as is in fact shown in FIGURE 5, to deal with this case also by introducing a three-bit delay into system A. As before, *a* and *b* represent the conditions of systems A and B respectively at the time when switching needs to take place because of the imminence of the in-phase condition. Thus when DA1 coincides with DB2, a three-bit delay is introduced into the A system which has the effect of advancing the B system as shown in *c*. The A system now continues to advance until the position of *d* is reached in which DA1 again coincides with DB2. When this occurs, the delay is cut out of system A, with the result that the B system is in effect advanced to the position of *e* which means that the in-phase condition has been passed without any loss of information. Again the A clock needs to be altered correspondingly when the delay is introduced and when it is cut out.

It may be noted that with the conditions of FIGURE 4 the in-phase condition is avoided by the delay operation so that it is not strictly necessary to cut out the delay subsequently though it is probably simpler to do so. With the conditions of FIGURE 5 however, the in-phase condition is not satisfactorily dealt with until the delay has been introduced and subsequently cut out.

The system as explained so far suggests that it might be necessary to make use of coincidence detection for each established connection, that is to say for each channel. However it is possible to secure considerable economy of components without appreciably prejudicing the operation by arranging for the inspection and delay switching operation to be confined to the synchronising channel CA0 of system A in association with any channel in the B system.

The detailed circuits are indicated diagrammatically in FIGURE 6 and as in FIGURES 1 and 2, the various gates are indicated by circles with a plurality of inputs represented by arrows and a single output. Where the figure in the circle is a 1, this indicates an OR gate and any one of the different inputs will produce an output. Where the figure in the circle is greater than 1, this represents an AND gate and an output will only be obtained if the number of inputs corresponding to the figure are all available at the same time. Toggles such as T1 and T2 are represented by rectangles divided into two, one half being labelled 0 and the other 1. The convention is adopted that the toggle is in the reset or unoperated condition when an output is obtained from the 0 side and in the set or operated condition when an output is obtained from the 1 side. The setting of the toggle, i.e., the change from the 0 to the 1 position, is effected by a suitable input applied to the 0 side and similarly the resetting operation, i.e., the change from the 1 to the 0 position, is effected by an input applied to the 1 side.

The notation commonly employed for indicating logic circuits is that designations of the various inputs which need to be present simultaneously to produce a switching operation are separated by dots and are followed by a dash and then an indication of the effect which is produced, for instance the setting or resetting of a toggle. As regards the toggles, the existence of the set condition or a change thereto is indicated by the reference numeral for the toggle and similarly the existence of the reset condition or a change thereto is indicated by this reference underlined. Where the same circuit produces the operation of two or more toggles, this is indicated by the use of the plus sign.

In the present instance use is made of two toggles T1 and T2, both of which are arranged to be set when the delay is to be introduced. Using the above mentioned notation for such circuits, in the case of FIGURE 4 where system B is running faster than system A this may be expressed as:

$$DA1.CA0.DB8.T1 - T1 + T2$$

The output from T1 then opens the gate G1, FIGURE 1, in the path involving the three-bit delay D1 while at the same time gate G2 is closed. Toggle T2 when operated has the effect of inhibiting the DA clock. T2 however is reset from its set input in a circuit including a three-bit delay D2 so that on the resetting of T2, the clock DA will resume its normal counting. When the conditions are reached for cutting out the delay, toggle T1 is restored in the circuit:

$$DA1.CA0.DB6.T1 - T1$$

thereupon gate G1 is closed and G2 is opened so that the signals pass to the stores without any delay. The same circuit which resets T1 also has the effect of advancing the DA clock to the DA6 position.

Similar circuits are used to cover the case in which the A system is faster than the B system but in this instance

DB2 is used in each case instead of DB8 and DB6 so that the circuits become:

$$\begin{aligned} &DA1.CA0.DB2.T1-T1+T2 \\ &DA1.CA0.DB2.T1-T1 \end{aligned}$$

The explanation so far given has been in terms of connecting one incoming system to one outgoing system, the two systems having nominally the same but actually slightly different clock frequencies and this is shown in FIGURE 7, which is a somewhat more diagrammatic form of FIGURE 1. In this case the delay unit D is shown as capable of being shunted by contacts x when the delay is not to be operative.

The arrangement of FIGURE 7 can clearly be duplicated to give two-directional 4-wire communication as indicated in FIGURE 8. Here the stores for signals incoming over the A and B systems respectively are shown at S1 and S2 and the delay units D1 and D2 are arranged to be shunted by contacts $x1$ and $x2$ when necessary.

A further possibility, illustrated in FIGURE 9, is to provide that channels from one or more of a set of m synchronous systems may be connected to any one of n systems which are themselves synchronous but have a slightly different clock rate from that of the set m . In FIGURE 9 which shows only one direction of transmission, the delay units D1, D2 and D m associated with systems A1, A2 and A m may be shunted by contacts $x1$, $x2$ and xm respectively and control the supply of the signals to the stores S1, S2 and S m . The systems B1-B n are all subject to the same clock or frequency control fB .

Still another possibility which comes within the scope of the invention is that several unidirectional systems all having independent clock rates, are concentrated on to a single system having the same nominal frequency as the others but actually asynchronous with them. This arrangement is shown diagrammatically in FIGURE 10 and it will be readily followed that the systems A1, A2 and A x have respectively associated with them the delay units D1, D2 and D x , shunting contacts $x1$, $x2$ and xx and stores S1, S2 and S x .

The invention accordingly provides a means of interconnecting a plurality of multiplex systems which substantially overcomes in a simple manner the danger of loss of information at intervals due to unavoidable differences in the basic frequencies of the different systems.

We claim:

1. In a time division multiplex pulse communication arrangement, a first system over which signals are transmitted to a receiving point, a first frequency control arrangement for controlling the multiplexing operation of said first system, a second system over which signals are transmitted from said receiving point, a second frequency control arrangement for controlling the multiplexing operation of said second system, the frequencies of said first and second frequency control arrangements being nominally the same but mutually independent, means at said receiving point for storing signals incoming over said first system under the control of said first frequency control arrangement, means for retransmitting said stored signals over said second system under the control of said second frequency control arrangement, and switching means for effecting a sudden change in the length of the storage period, said switching means being operated when owing to progressive slight changes in the frequencies defined by at least one of said first and second frequency control arrangements the time relationship between the storage and retransmitting operations of said storage means is such that the time between completion of storage and commencement of retransmission approaches zero and also when the time relationship is such that the time between completion of retransmission and commencement of storage approaches zero, whereby the prospective interfering phase relationship between said first and second frequency control arrangements is avoided.

2. In a time division multiplex pulse communication arrangement, a first system over which signals are transmitted to a receiving point, a first frequency control arrangement for controlling the multiplexing operation of said first system, a second system over which signals are transmitted from said receiving point, a second frequency control arrangement for controlling the multiplexing operation of said second system, the frequencies of said first and second frequency control arrangements being nominally the same but mutually independent, means at said receiving point for storing signals incoming over said first system under the control of said first frequency control arrangement, means for retransmitting said stored signals over said second system under the control of said second frequency control arrangement, and switching means for effecting a sudden increase in the length of the storage period, said switching means being operated when owing to progressive slight changes in the frequencies defined by at least one of said first and second frequency control arrangements the time relationship between the storage and retransmitting operations of said storage means is such that the time between completion of storage and commencement of retransmission approaches zero, whereby the prospective interfering phase relationship between said first and second frequency control arrangements is avoided.

3. In a time division multiplex pulse communication arrangement, a first system over which signals are transmitted to a receiving point, a first frequency control arrangement for controlling the multiplexing operation of said first system, a second system over which signals are transmitted from said receiving point, a second frequency control arrangement for controlling the multiplexing operation of said second system, the frequencies of said first and second frequency control arrangements being nominally the same but mutually independent, means at said receiving point for storing signals incoming over said first system under the control of said first frequency control arrangement, means for retransmitting said stored signals over said second system under the control of said second frequency control arrangement, and switching means for effecting a sudden increase in the length of the storage period and subsequently a corresponding decrease in the length of said period, said switching means being operated when owing to progressive slight changes in the frequencies defined by at least one of said first and second frequency control arrangements the time relationship between the storage and retransmitting operations of said storage means is such that the time between completion of storage and commencement of retransmission approaches zero and also when the time relationship is such that the time between completion of retransmission and commencement of storage approaches zero, whereby the prospective interfering phase relationship between said first and second frequency control arrangements is avoided.

4. In a time division multiplex pulse communication arrangement, a first system over which signals are transmitted to a receiving point, a first frequency control arrangement for controlling the multiplexing operation of said first system, a second system over which signals are transmitted from said receiving point, a second frequency control arrangement for controlling the multiplexing operation of said second system, the frequencies of said first and second frequency control arrangements being nominally the same but mutually independent, means at said receiving point for storing signals incoming over said first system under the control of said first frequency control arrangement, means for retransmitting said stored signals over said second system under the control of said second frequency control arrangement, a delay device, and switching means for introducing said delay device into the circuit over which said incoming signals are supplied to said storage means and subsequently removing said delay device from said circuit, said switching means being

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operated when owing to progressive slight changes in the frequencies defined by at least one of said first and second frequency control arrangements the time relationship between the storage and retransmitting operations of said storage means is such that the time between completion of storage and commencement of retransmission approaches zero and also when the time relationship is such that the time between completion of retransmission and commencement of storage approaches zero, whereby the prospective interfering phase relationship between said first and second frequency control arrangement is avoided.

5. A time division multiplex pulse communication arrangement as claimed in claim 1 in which said first and second system serve for the transmission of pulse code modulation signals, each complete frame including a plu-

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rality of information channels and a synchronizing channel.

6. An arrangement as claimed in claim 5 in which said switching means are controlled so as to be operated during said synchronising channel.

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