A method of using a laser (16) to etch patterns in a thin layer of amorphous silicon (14) which is used as a mask for the etching of a layer of silicon dioxide (12) in integrated circuit fabrication. The laser is used to etch the amorphous silicon in the presence of halogen ions. Subsequently, the amorphous silicon is used as a mask to plasma etch the silicon dioxide. Alternate embodiments of the method etch a metal region on a substrate, or a silicon dioxide layer on a metal region, both using an etched amorphous silicon mask. An alternate embodiment uses a double masking technique to etch an amorphous silicon mask, which is used to etch a silicon dioxide hard mask, which is used to etch a metal region.
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METHOD OF LASER ETCHING OF SILICON DIOXIDE

This invention relates to a method of patterning oxide for the fabrication of integrated circuits using laser pantography.

The patterning of oxide is one of the most basic and repeated steps in the fabrication of integrated circuit devices particularly in silicon microelectronics. Silicon dioxide (SiO₂) is often used as a mask against ion implantation or diffusion. It is also used as an isolation layer to define transistor geometries. Conventionally, this oxide patterning is done using photolithography techniques. Photolithography employs wet chemical processes for coating and developing a photoresist layer. The photolithography process required for each oxide delineation comprises a series of several steps. The photolithography process is a source of contamination and defect generation and often produces a loss of circuit yields. Also inherent in the photolithography process is the need to have proper exposure and focus on a photoresist layer on the surface of the semiconductor element to be patterned. Focusing and exposure becomes difficult as the topology of the integrated circuit varies and is particularly difficult over reflective metal regions of the integrated circuit device.

Accordingly, there is a need in the art for an improved method for etching silicon dioxide layers on an integrated circuit or other semiconductor element.

SHORT STATEMENT OF THE INVENTION

The present invention relates to a method of using a laser to provide a method of etching openings in a silicon dioxide (SiO₂) pattern on an integrated circuit or other semiconductor element. In accordance with the invention, a thin layer, for example, 2,000 Å, of amorphous silicon is blanket deposited over the surface area of an integrated circuit or other semiconductor element upon which an oxide pattern is to be delineated. Using a focused laser beam with sufficient power having a wavelength of, for example, 5,145 Å as a point heat source and placing the integrated circuit

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or semiconductor element in a gaseous environment such as Cl₂ or HCl or other halogen ion, the desired pattern is etched in the amorphous silicon. After laser etching the amorphous silicon, the semiconductor substrate is then placed in a plasma etcher or reactive ion etcher (RIE). In a plasma etcher using a gas, such as CHF₃, which has a selectivity ratio of SiO₂:Si equal to 10:1, the laser etched pattern in the amorphous silicon can be transferred to the silicon dioxide. After the etching of the SiO₂, the amorphous silicon layer can be removed, if desired.

One advantage of the present invention is that all wet chemical steps may be eliminated during etching of the oxide when fabricating integrated circuits. The use of the present invention is easily adapted to automation where standard machine interface ("SMIF") boxes for transferring substrates between machines are used. Therefore, clean room requirements are reduced or eliminated, providing for a truly all dry process for the fabrication of integrated circuits.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Other improvements, advantages and features of the present invention will become more fully apparent from the following detailed description of the preferred embodiments, the appended claims and the accompanying drawings in which:

Figure 1 illustrates a first step in accordance with a preferred embodiment of the present invention;

Figure 2 shows the second step in accordance with a preferred embodiment of the present invention;

Figure 3 illustrates the third step in accordance with a preferred embodiment;

Figure 4 shows the resulting step in accordance with a preferred embodiment of the present invention.

Figures 5, 6, 7 and 8 show various steps of etching using the invention to etch a metallic layer with an amorphous silicon mask.

Figures 9, 10, 11, 12 and 13 show an alternative preferred embodiment of the invention which etches a metallic layer using both an amorphous silicon mask and a silicon dioxide etched hard mask in a double masking technique.
DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The Figures, by way of example, illustrate a preferred embodiment of the present invention. It should be appreciated that the oxide patterning process of the present invention may be used in connection with any type of patterning of silicon dioxide on an integrated circuit or other semiconductor element. By way of example, the invention may be used in forming the implant mask openings on an integrated circuit.

The semiconductor substrate 10 has a thin film of SiO$_2$ 12 which has been either grown or deposited on the substrate. A blanket deposition of amorphous silicon 14 is made over the thin film of SiO$_2$ 12. It is preferable that the amorphous silicon layer 14 be less than about 2,000 Å in thickness.

A focused laser beam illustrated by the arrows 16 in Figure 2 and having a wavelength of, for example, 5,145 Å, is used as a point heat source. The semiconductor substrate 10 having the thin film layer of SiO$_2$ 12 and amorphous silicon layer 14 is placed in a chamber having a gaseous environment of Cl$_2$ or HCl or other halogen containing gas. The laser beam 16 is focused on the amorphous silicon 14 and traversed along the surface of the amorphous silicon 14 in the form of the desired SiO$_2$ pattern openings, and by doing so, the thin amorphous silicon layer 14 is etched away. The laser’s light and heat interact with the halogen gas environment to loosen the gas’s ionic covalent bond. The resulting etchant gas turns the amorphous silicon layer 14 into a gas at the point of contact of the laser beam on the amorphous silicon. The gaseous compounds are then pumped out of the pantography chamber. Because the reaction chamber remains at room temperature, process-gas contamination of the chamber or the workplace is virtually eliminated.

After laser etching the amorphous silicon, the integrated circuit device is then placed in plasma etcher or reactive ion etcher (RIE) to transfer (by conventional integrated circuit fabrication means) the pattern existing on the amorphous silicon to the SiO$_2$ layer. In a plasma etcher using a gas such as CHF$_3$, a selectivity ratio of silicon
dioxide to silicon equal to 10:1 can be achieved. After suitable etch time, the pattern delineated in the amorphous silicon is transferred into the SiO$_2$ layer 10 as shown in Figure 3. The use of a plasma etcher or RIE allows for the bulk etching of the SiO$_2$ rather than an area-by-area etch limited by the area of a laser scan.

After the etching of the SiO$_2$, the amorphous silicon 14 can be plasma stripped to remove the amorphous silicon layer 14. This is shown in Figure 4. Alternatively, it may not be necessary to remove the amorphous silicon layer 14 and it may, in fact, be desirable to have it remain for use in later integrated circuit processing.

The invention as described eliminates the need for wet chemistry in all processes and particularly in the use of photolithography. The yield loss during photolithography due to particles, contamination, over and under cutting, and bad exposure are all eliminated.

The process can be used to pattern oxides even over metal regions and is not subject to topology or reflectivity variations existing on the integrated circuit substrate. This also permits etching metal layers or regions on integrated circuit substrates.

Figure 5 shows this embodiment of the invention. The amorphous silicon layer 14 is deposited over the metallic layer 21 on the substrate 10. In Figure 6 the laser 16 etches the amorphous silicon 14 in the manner of the previous embodiments. In Figure 7 the etched amorphous silicon 14 is then used as a mask to etch the metallic layer 21 by placing it in a blank environment.

Then in Figure 8 the amorphous silicon layer may be removed if required or it may be left in place as shown in Figure 7.

The heat flow into the metal layer 21 of this embodiment, arising from the laser etch of the amorphous silicon layer 14, may cause a loss of the subsequent lasography effect required. This might be avoided by the use of excimer lasers to etch, or other means. Currently, to prevent this heat flow, the preferred embodiment is to
deposit a layer of silicon dioxide between the metal layer 21 and the amorphous silicon 14, as shown in Figure 9. As shown in Figure 10, laser 16 then will etch a mask in the amorphous silicon 14. The silicon dioxide layer 12 will then be etched through the amorphous silicon mask 14, as shown in Figure 11. Then as shown in Figure 12, the metal layer 21 may be etched through the hard mask provided by the silicon dioxide 12. This is a double masking technique. The etching of the silicon 12 and the metal layer 21 might, in theory, be done in the same chamber with a two-step process, however, it is preferable to etch the SiO2 in a separate step from the metal in order to split the etch chemistry and for cleanliness reasons.

After the etching, the amorphous silicon layer 14 may be plasma stripped if required, as shown in Figure 13. Also, the silicon dioxide layer 12 may be removed as shown in Figure 14, if required.

Because the laser can be accurately controlled during the etching of the amorphous silicon, undercutting can be minimized or can be controllably reproduced.

While the present invention has been disclosed in connection with the preferred embodiment thereof, it should be appreciated that other embodiments may be used in keeping with the spirit and scope of the present invention as defined by the appended claims. Examples of variations include the use of the invention to etch various materials and their oxides or nitrides.
We Claim:

1. A method of laser etching an oxide or nitride coated substrate comprising the steps of:
   (a) depositing an amorphous silicon layer on the substrate;
   (b) forming a pattern in the amorphous silicon layer by exposing selected regions of the amorphous silicon layer to laser light in the presence of reactive ions; and
   (c) etching the substrate in a plasma environment or reactive ion environment using the amorphous silicon as a mask over the oxide or nitride.

2. A method of laser etching a silicon dioxide layer on an integrated circuit device comprising the steps of:
   (a) depositing an amorphous silicon layer over the silicon dioxide layer on the integrated circuit device;
   (b) forming a pattern in the amorphous silicon layer by exposing selected regions of the amorphous silicon layer to laser light in the presence of reactive ions; and
   (c) etching the silicon dioxide layer on the integrated circuit device in a plasma environment or reactive ion environment using the amorphous silicon as a mask over the silicon dioxide.

3. The method of claim 2 wherein the amorphous silicon layer is less than about 2,000 Å in thickness.

4. The method of claim 2 wherein the laser used to expose selective regions of the amorphous silicon has a wavelength of 5,145 Å.

5. The method of claim 2 wherein the reactive ions are halogen ions.

6. The method of claim 5 wherein the reactive ions are chlorine ions.

7. The method of claim 2 wherein the silicon dioxide is etched in a plasma etchant containing CHF₃.
8. A method of laser etching a metallic layer region in an integrated circuit device comprising the steps of:
   (a) depositing an amorphous silicon layer over the metallic layer region on the integrated circuit device;
   (b) forming a pattern in the amorphous silicon layer by exposing selected regions of the amorphous silicon layer to laser light in the presence of reactive ions, and
   (c) etching the metallic layer region on the integrated circuit device in a plasma environment or a reactive ion environment using the amorphous silicon as a mask over the metallic layer.

9. A method of laser etching a silicon dioxide layer over a metallic layer region in an integrated circuit device comprising the steps of:
   (a) depositing a layer of silicon dioxide over the metallic layer region on the integrated circuit device;
   (b) depositing a layer of amorphous silicon over the layer of silicon dioxide that was deposited over the metallic layer region.
   (c) forming a pattern in the amorphous silicon layer by exposing selected regions of the amorphous silicon layer to laser light in the presence of reactive ions, and
   (d) etching the layer of silicon dioxide that was deposited over the metallic layer region, in a plasma environment or a reactive ion environment using the amorphous silicon as a mask to the layer of silicon dioxide.

10. The method in claim 9, further comprising the step of:
   (a) etching the metallic layer region on the integrated circuit device in a plasma environment or a reactive ion environment
using the etched layer of silicon dioxide as a hard mask over the metallic layer region.
### INTERNATIONAL SEARCH REPORT

**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

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According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

| U.S. | 437/101, 357/2, 148/DIG. 1 |

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<td>JP 0,173,502 (YAMADA) 06 September 1983, See abstract.</td>
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<td>X</td>
<td>EP 0,272,799 (JANAI) 29 June 1988, See column 1, lines 17-46.</td>
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Relevant to claim No.

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| 7         |
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Further documents are listed in the continuation of Box C. See patent family annex.

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  - document published prior to the international filing date but later than the priority date claimed

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**Date of the actual completion of the international search**

21 JULY 1992

**Date of mailing of the international search report**

SEP 1992

**Name and mailing address of the ISA/Commissioner of Patents and Trademarks**

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Washington, D.C. 20231

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