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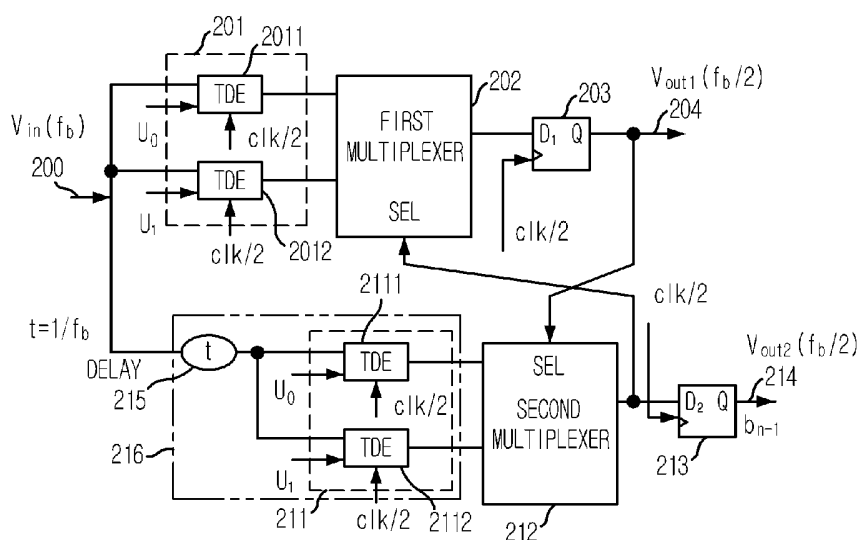
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(54) Title: PARALLEL DECISION FEEDBACK EQUALIZER FOR STABLE EQUALIZATION OF HIGH SPEED DATA



(57) Abstract: A parallel decision feedback equalizer for stable equalization of high speed data is provided. The parallel decision feedback equalizer includes: a first parallel threshold decision element having at least two parallel threshold decision elements each having a different threshold value; a first multiplexer for multiplexing data from the first parallel threshold decision element based on a second output from a second multiplexer; a first D flip-flop for delaying a first output from the first multiplexer by a unit data clock pulse; a second parallel threshold decision element having a third delay unit and at least two parallel threshold decision elements each having a different threshold value; the second multiplexer for multiplexing data from the second parallel threshold decision element based on a delayed output from the first D flip-flop; and a second D flip-flop for delaying the second output from the second multiplexer by the unit data clock pulse.

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Description

PARALLEL DECISION FEEDBACK EQUALIZER FOR STABLE EQUALIZATION OF HIGH SPEED DATA

Technical Field

- [1] The present invention relates to a parallel decision feedback equalizer; and, more particularly, to a parallel decision feedback equalizer for equalizing high speed data in stable based on data synchronization.

[2]

Background Art

- [3] Fig. 1 is a circuit diagram of a conventional parallel decision feedback equalizer.

- [4] First, f_b is a bit rate of input data, U_0 is a first threshold of a present bit when a previous bit is '0', U_1 is a second threshold of the present bit when the previous bit is '1', $clk/2$ is a clock signal having a half of a clock rate of the input data.

- [5] As shown in Fig. 1, the conventional parallel decision feedback equalizer includes two parallel channels 101, 110 which are parallel. Two parallel channels are used to reduce a bit rate of decisions in each channel by a factor of two. Since a bit outputted from one parallel channel should be used to select decision of the other parallel channel' next bit, both parallel channels have to be coupled crosswise.

- [6] The first channel 101 includes two parallel threshold decision elements 102 and 104 having different thresholds U_0 and U_1 respectively and transmitting their outputs to a multiplexer 103, the multiplexer 103 transmitting output data to a first D flip-flop 105, and the D flip-flop 105 outputting the delayed output data.

- [7] The second channel 110 includes two parallel threshold decision elements 112 and 114 having different thresholds U_0 and U_1 respectively and transmitting their outputs to a multiplexer 113, the multiplexer 113 transmitting output data to a second D flip-flop 115, and the second D flip-flop 115 outputting the delayed output data.

- [8] The first channel 101 is operated in response to the clock signal $clk/2$ and the second channel 110 is operated in response to an out-of-phase of the clock signal

$\overline{clk/2}$

. Thus, the two parallel channels demultiplex the input data 1:2.

- [9] A threshold of the next bit is decided based on output data from the multiplexer of one parallel channel which controls selection of the multiplexer of the other parallel channel. As a result, demultiplexed and equalized data is outputted from the each parallel channel.

- [10] As describe above, the conventional parallel decision feedback equalizer has parallel structure for doubling processing rate. The conventional parallel decision

feedback equalizer has characteristics that a first output of the multiplexer of one parallel channel controls selection of the multiplexer of the other parallel channel and a second output of the multiplexer of the other parallel channel controls selection of the multiplexer of the one parallel channel. Therefore, there is problem that unstable operations can occur because the input data are processed asynchronously.

[11]

Disclosure of Invention

Technical Problem

[12] It is, therefore, an object of the present invention to provide a parallel decision feedback equalizer for equalizing high speed data in stable base on data synchronization.

[13]

Technical Solution

[14] In accordance with one aspect of the present invention, there is provided a parallel decision feedback equalizer for stable equalization of high speed data, including: a first parallel threshold decision element having at least two parallel threshold decision elements each having a different threshold value; a first multiplexer for multiplexing data from the first parallel threshold decision element based on a second output from a second multiplexer, to thereby generate a first multiplexed signal; a first D flip-flop for delaying a first output from the first multiplexer by a unit data clock pulse; a second parallel threshold decision element having a third delay unit and at least two parallel threshold decision elements each having a different threshold value; the second multiplexer for multiplexing data from the second parallel threshold decision element based on a delayed output from the first D flip-flop; and a second D flip-flop for delaying the second output from the second multiplexer by the unit data clock pulse.

[15]

Advantageous Effects

[16] According to the present invention, stable operation can be performed through including a flip-flop in feedback loop synchronized at clock signal.

[17] In the present invention, a signal distortion of high speed data can be compensated using the parallel decision feedback equalizer. That is, the high speed data can be equalized stably based on data synchronization.

[18]

Brief Description of the Drawings

[19] The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

[20] Fig. 1 is a circuit diagram of a conventional parallel decision feedback equalizer;

[21] Fig. 2 is a circuit diagram illustrating a parallel decision feedback equalizer in accordance with a first embodiment of the present invention;

[22] Fig. 3 shows a timing diagram of the parallel decision feedback equalizer in accordance with the present invention; and

[23] Fig. 4 is a circuit diagram illustrating a parallel decision feedback equalizer in accordance with a second embodiment of the present invention.

[24]

Best Mode for Carrying Out the Invention

[25] Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, which is set forth hereinafter.

[26] The present invention relates to a decision feedback equalizer to compensate distortion for high speed data in an optical fiber. The present invention can improve instability of the conventional parallel decision feedback equalizer.

[27] Fig. 2 shows a circuit diagram illustrating a parallel decision feedback equalizer for equalizing high speed data in stable in accordance with a first embodiment of the present invention.

[28] As shown in Fig. 2, the parallel decision feedback equalizer includes a first parallel threshold decision element 201, a first multiplexer 202, a first D flip-flop 203, a second parallel threshold decision element 216, a second multiplexer 212 and a second D flip-flop 213.

[29] The first parallel threshold decision element 201 having parallel two threshold decision elements (TDE) 2011, 2012, receives input data 200 and transmits output to the first multiplexer 202.

[30] The first multiplexer 202 receives data transmitted from the first parallel threshold decision element 201 to generate a first multiplexed signal and transmits the first multiplexed signal to the first D flip-flop 203 based on a control signal (SEL).

[31] The first D flip-flop 203 outputs a first output signal 204 which controls selection of the second multiplexer 212.

[32] The second parallel threshold decision element 216 includes a delay unit 215 which delays the input data by one bit and outputs the delayed input data to two threshold decision elements (TDE) 2111 and 2112, and the threshold decision elements (TDE) 2111 and 2112 receive the delayed input data 200 and transmit output to the second multiplexer 212.

[33] The second multiplexer 212 receives the delayed data transmitted from the second parallel threshold decision element 211 to generate a second multiplexed signal and

transmits the second multiplexed signal to the second D flip-flop 213. The output from the second multiplexer 212 controls selection of the first multiplexer 202.

[34] The second D flip-flop 213 outputs a second output signal 214.

[35] In addition, the first parallel threshold decision element 201 and the second parallel threshold decision element 211 are operated based on the same in-phase clock signal $\text{clk}/2$.

[36] Fig. 3 shows a timing diagram of the parallel decision feedback equalizer in accordance with the present invention.

[37] Referring to Fig. 3, the second parallel threshold decision element 216 outputs the delayed data which is delayed by one bit from the input data of the first parallel threshold decision element 201. Since the parallel threshold decision elements 201, 211 are operated based on the same clock signal which is half rate of the input data, the input data are demultiplexed by 1:2.

[38] In addition, since the output of the first flip-flop 203 is one bit delayed data compared with the second parallel threshold decision element 216, the first flip-flop 203 decides one bit later data based on selection control of the second multiplexer 212.

[39] Moreover, since the output of the second multiplexer 212 is one bit delayed data compared with the first parallel threshold decision element 201, the second multiplexer 212 decides one bit later data based on selection control of the first multiplexer 202.

[40] Therefore, since output of the first flip-flop 203 controls selection of the second multiplexer 212 synchronously, outputs of the first multiplexer 202 and the second multiplexer 212 are synchronized to the clock signal. Thus, stable parallel decision feedback equalizing performed.

[41] Fig. 4 is a circuit diagram illustrating parallel decision feedback equalizer for equalizing high speed data in stable in accordance with a second embodiment of the present invention.

[42] As shown in Fig. 4, the parallel decision feedback equalizer includes a first parallel threshold decision element 401, a first multiplexer 402, a first D flip-flop 403, a second parallel threshold decision element 416, a second multiplexer 412 and a second D flip-flop 413.

[43] The first parallel threshold decision element 401 having parallel two threshold decision elements (TDE) 4011 and 4012, receives input data 400 and transmits output to the first multiplexer 402.

[44] The first multiplexer 402 receives data transmitted from the first parallel threshold decision element 401 to generate a first multiplexed signal and transmits the multiplexed signal to the first D flip-flop 403 based on a control signal.

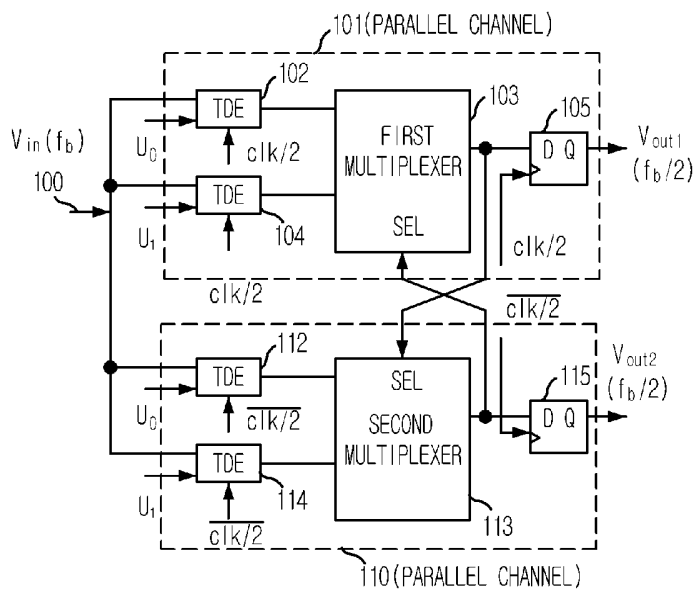
[45] The first D flip-flop 403 outputs a first output signal 404 which controls selection of a second multiplexer 412.

- [46] The second parallel threshold decision element 416 includes two parallel threshold decision elements (TDE) 4111 and 4112 which receives the input data 400 and transmits output to each delay unit 417 and 418, and the two delay units 417 and 418 delay outputs from the two threshold decision elements TDE 4111 and 4112 by one bit and outputs the delayed data to the second multiplexer 412.
- [47] The second multiplexer 412 receives the delayed data to generate a second multiplexed signal and transmits the second multiplexed signal to the second D flip-flop 413. The output of the second multiplexer 412 controls selection of the first multiplexer 402.
- [48] Then, the second D flip-flop 413 outputs a second output signal 414.
- [49] In addition, the first parallel threshold decision elements 401 is operated based on a half of the clock signal $clk/2$ and the parallel two threshold decision elements 4111, 4112 are operated based on out-of-phase clock signal $\overline{clk/2}$.
- [50] The present application contains subject matter related to Korean patent application No. 2004-0107264, filed with the Korean Intellectual property Office on December 16, 2004, the entire contents of which is incorporated herein by reference.
- [51] While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

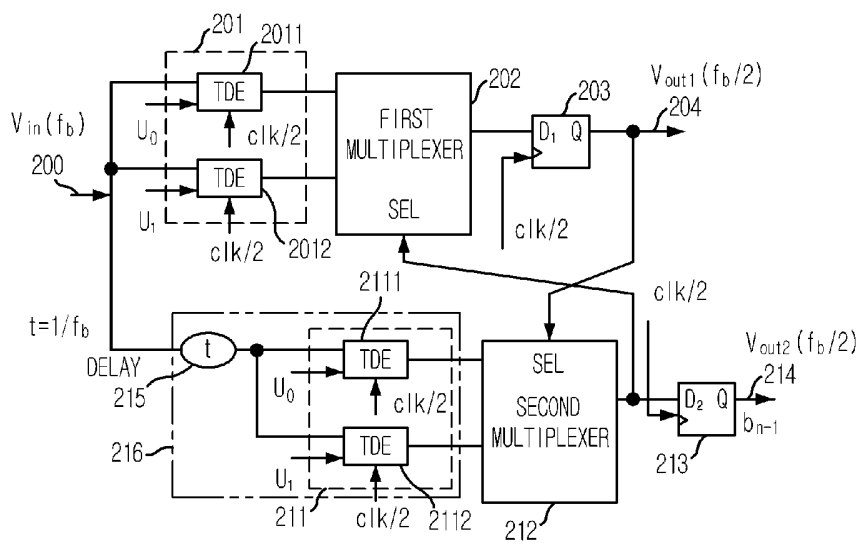
Claims

- [1] Parallel decision feedback equalizer for stable equalization of high speed data, comprising:
a first parallel threshold decision means having at least two parallel threshold decision elements each having a different threshold value;
a first multiplexing means for multiplexing data from the first parallel threshold decision means based on a second output from a second multiplexing means, to thereby generate a first multiplexed signal;
a first delaying means for delaying a first output from the first multiplexing means by a unit data clock pulse;
a second parallel threshold decision means having a third delaying means and at least two parallel threshold decision elements each having a different threshold value;
the second multiplexing means for multiplexing data from the second parallel threshold decision means based on a delayed output from the first data delaying means; and
a second data delaying means for delaying the second output from the second multiplexing means by the unit data clock pulse.
- [2] The parallel decision feedback equalizer as recited in claim 1, wherein the third delaying means located in front of the two threshold decision elements, and outputs the delayed input data to each of the threshold decision elements.
- [3] The parallel decision feedback equalizer as recited in claim 2, wherein the second parallel threshold decision means receives an in-phase clock signal as the same as the first parallel threshold decision means.
- [4] The parallel decision feedback equalizer as recited in claim 2, wherein the third delaying means delays the input data by one bit of the input data.
- [5] The parallel decision feedback equalizer as recited in claim 1, wherein the third delaying means located at output ports of each threshold decision element.
- [6] The parallel decision feedback equalizer as recited in claim 4, wherein the second parallel threshold decision means receives an out-of-phase clock signal of the first parallel threshold decision means.

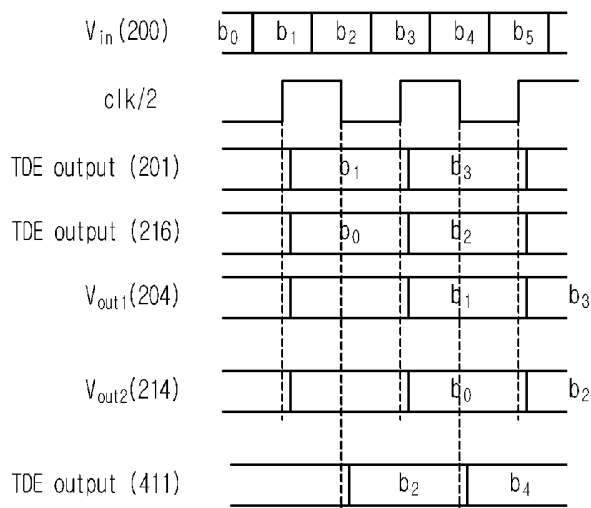
[Fig. 1]



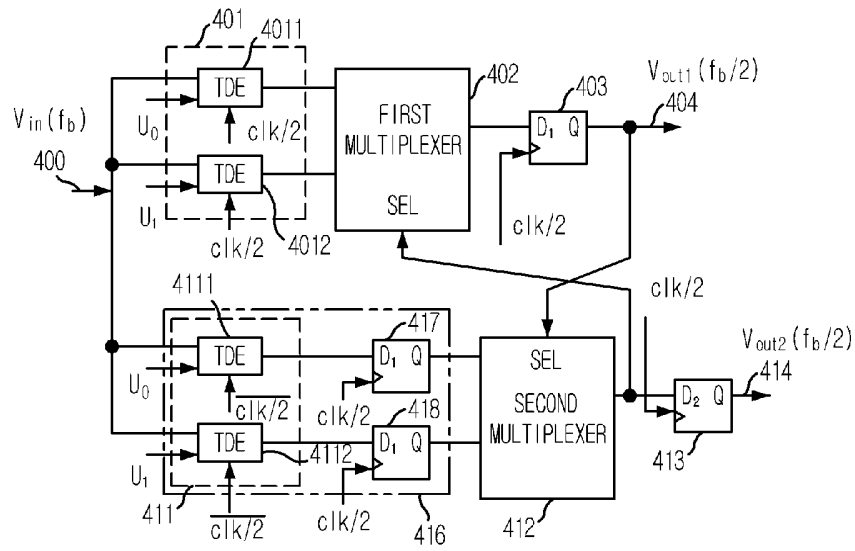
[Fig. 2]



[Fig. 3]



[Fig. 4]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/004327

A. CLASSIFICATION OF SUBJECT MATTER**H04L 27/01(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8: H04J H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KOREAN PATENTS AND APPLICATIONS FOR INVENTIONS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PAJ, FPD, USPAT, eKIPASS, IEEE "EQUALIZER""SYNCHRONIZATION""CLOCK""DELAY"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Moller, L.; Zheng Gu; Thiede, A.; Chandrasekhar, S.; Stulz, L.; "20 Gbit/s electrical data recovery using decision feedback equaliser supported receiver", Electronics Letters Volume 39, Issue 1, 9 Jan 2003 Page(s):78 - 79 see the whole document, FIGURE 1	1-6
Y	Ginosar, R.; Kol, R.; "Adaptive synchronization" Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on 5-7 Oct. 1998 Page(s):188 - 189 see the whole document, FIGURE 2 AND 3	1-6

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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Date of the actual completion of the international search

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