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(54) **INTEGRATED CIRCUIT AND METHOD OF MAKING**

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(52) **U.S. Cl.**

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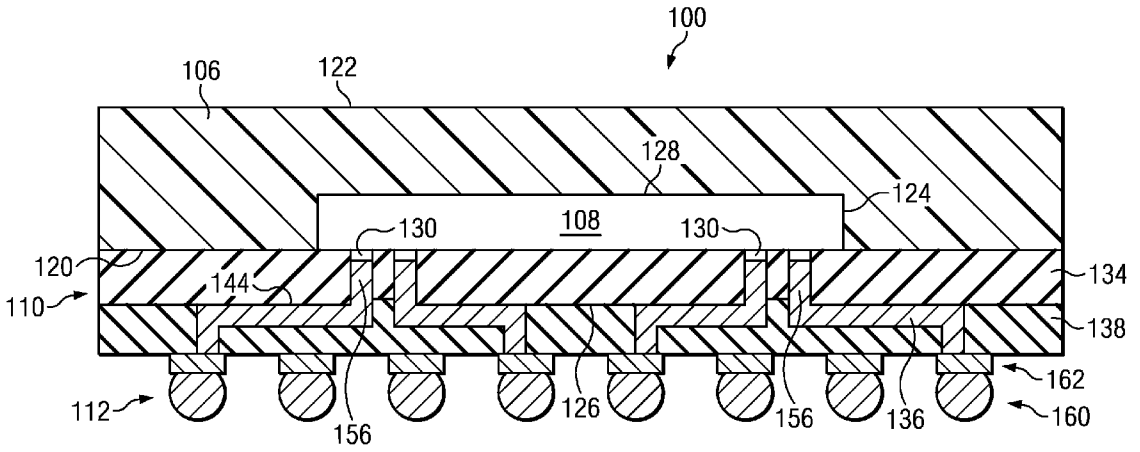
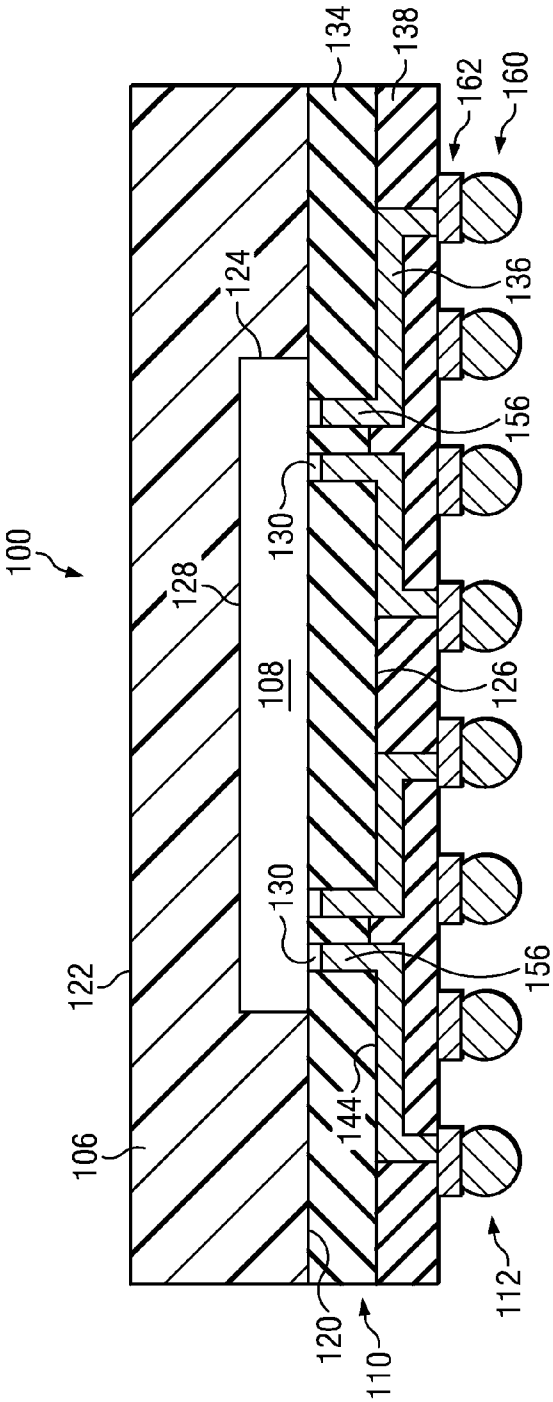
(57) **ABSTRACT**

Circuits and methods of fabricating circuits are disclosed herein. An embodiment of the circuit includes a die having a side, wherein a connection point is located on the side. A dielectric layer having a first side, a second side, and at least one via extending between the first side and the second side, is located proximate the side of the die. The via is electrically connected to the connection point. A conductive layer is located adjacent the second side of the first dielectric layer, wherein at least a portion of the conductive layer is electrically connected to the via.




100
106
108
110
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122
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144
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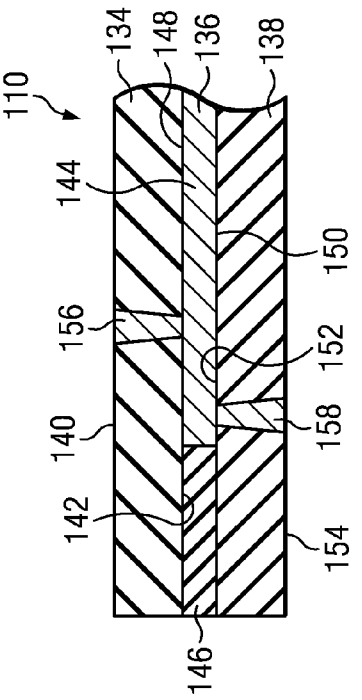
156
160
162

FIG. 1


110
134
136
138
140
142
144
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148
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152
154
156
158

FIG. 2

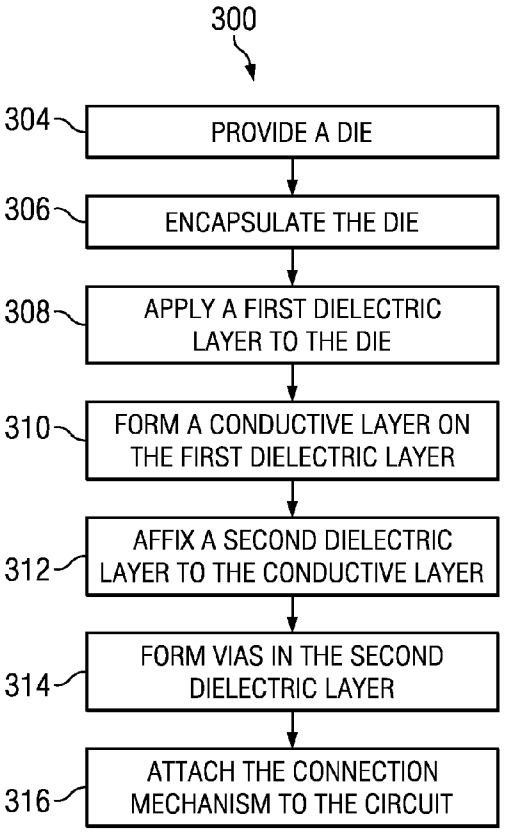

300
304
PROVIDE A DIE
306
ENCAPSULATE THE DIE
308
APPLY A FIRST DIELECTRIC LAYER TO THE DIE
310
FORM A CONDUCTIVE LAYER ON THE FIRST DIELECTRIC LAYER
312
AFFIX A SECOND DIELECTRIC LAYER TO THE CONDUCTIVE LAYER
314
FORM VIAS IN THE SECOND DIELECTRIC LAYER
316
ATTACH THE CONNECTION MECHANISM TO THE CIRCUIT

FIG. 3

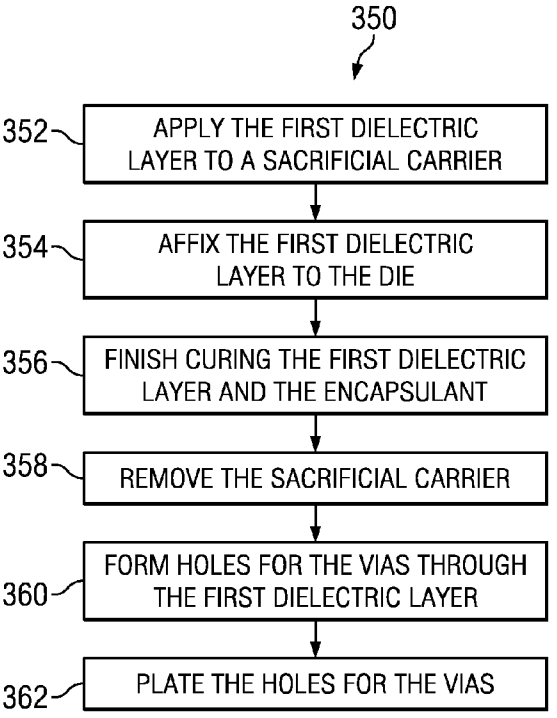

350
352
APPLY THE FIRST DIELECTRIC LAYER TO A SACRIFICIAL CARRIER
354
AFFIX THE FIRST DIELECTRIC LAYER TO THE DIE
356
FINISH CURING THE FIRST DIELECTRIC LAYER AND THE ENCAPSULANT
358
REMOVE THE SACRIFICIAL CARRIER
360
FORM HOLES FOR THE VIAS THROUGH THE FIRST DIELECTRIC LAYER
362
PLATE THE HOLES FOR THE VIAS

FIG. 6

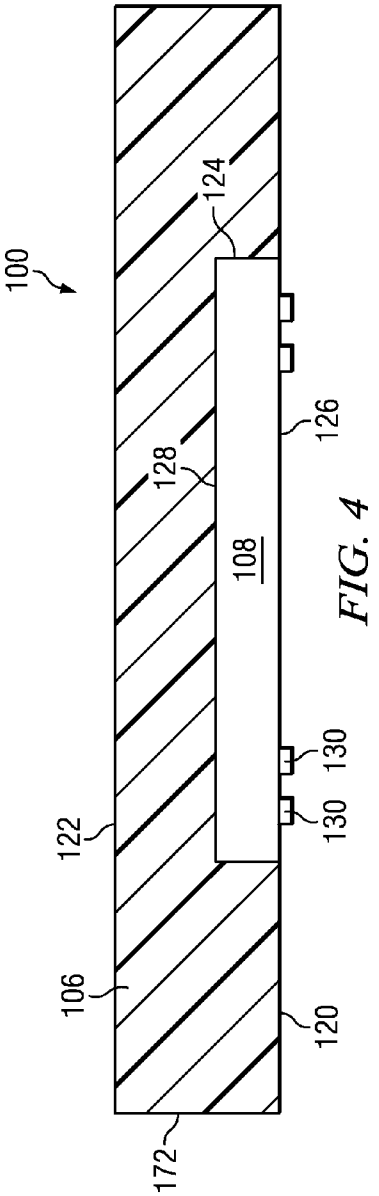

100
124
126
128
108
130
130
122
106
120
172

FIG. 4

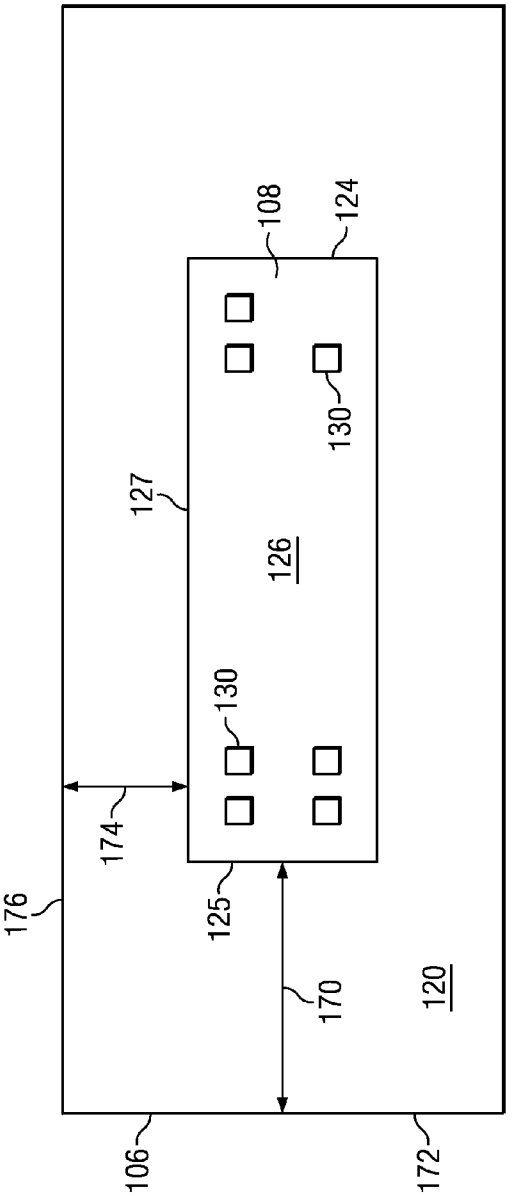

108
124
130
127
126
130
174
176
125
170
120
106
172

FIG. 5

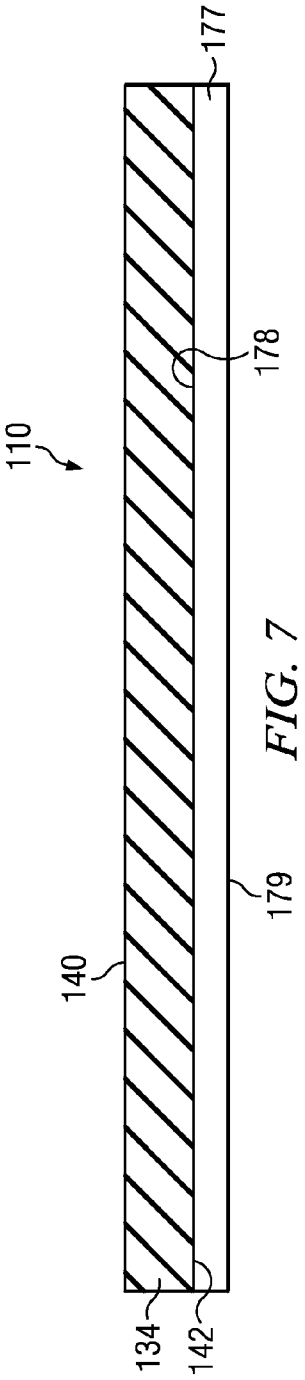
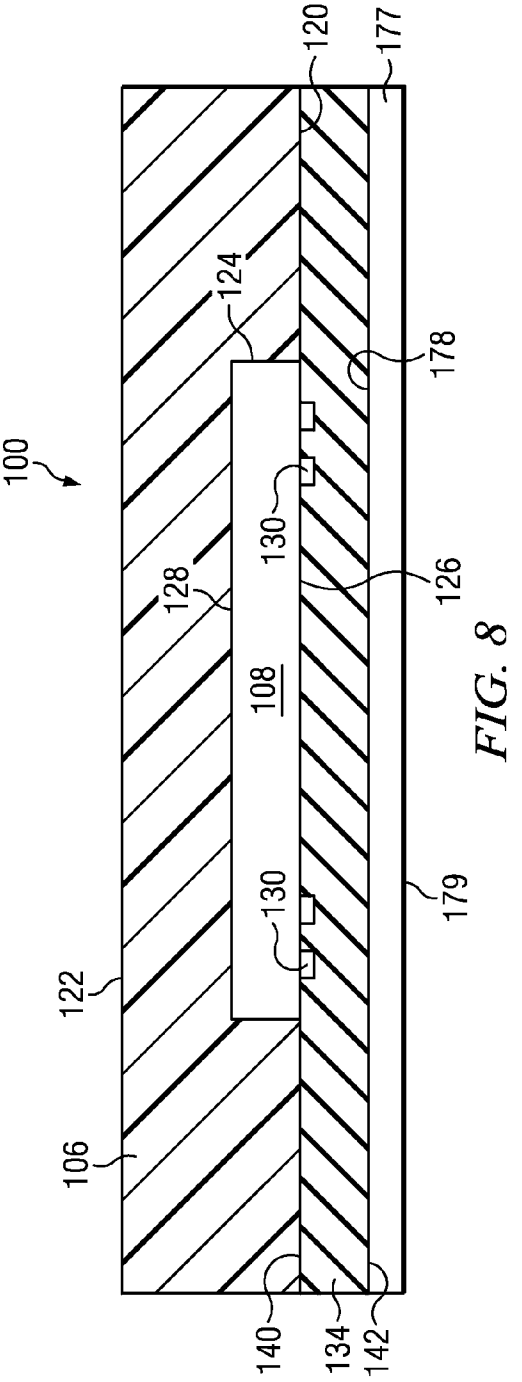

110
177
178
179
140
134
142

FIG. 7


100
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177
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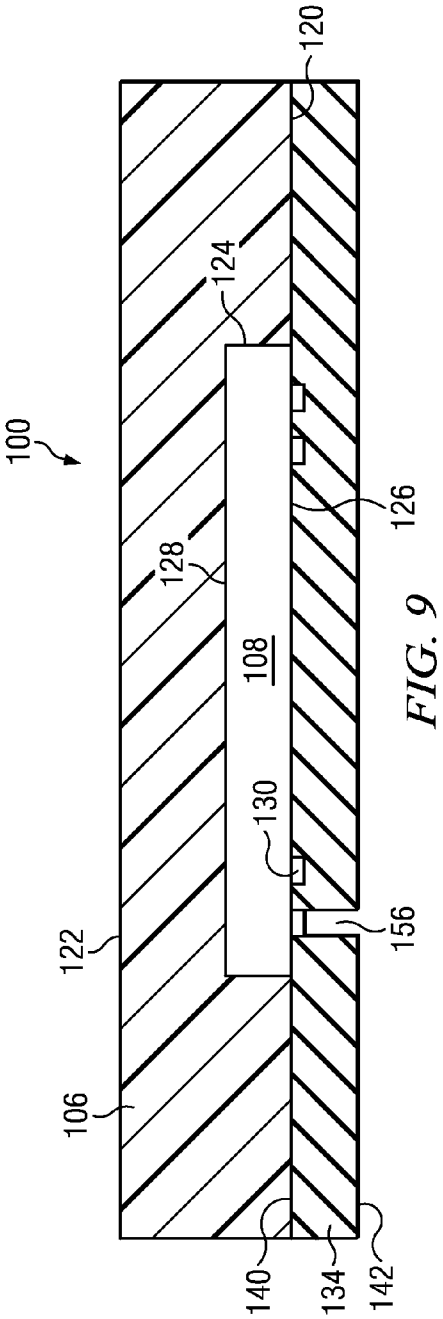
134
142

FIG. 8


100
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134
142

FIG. 9

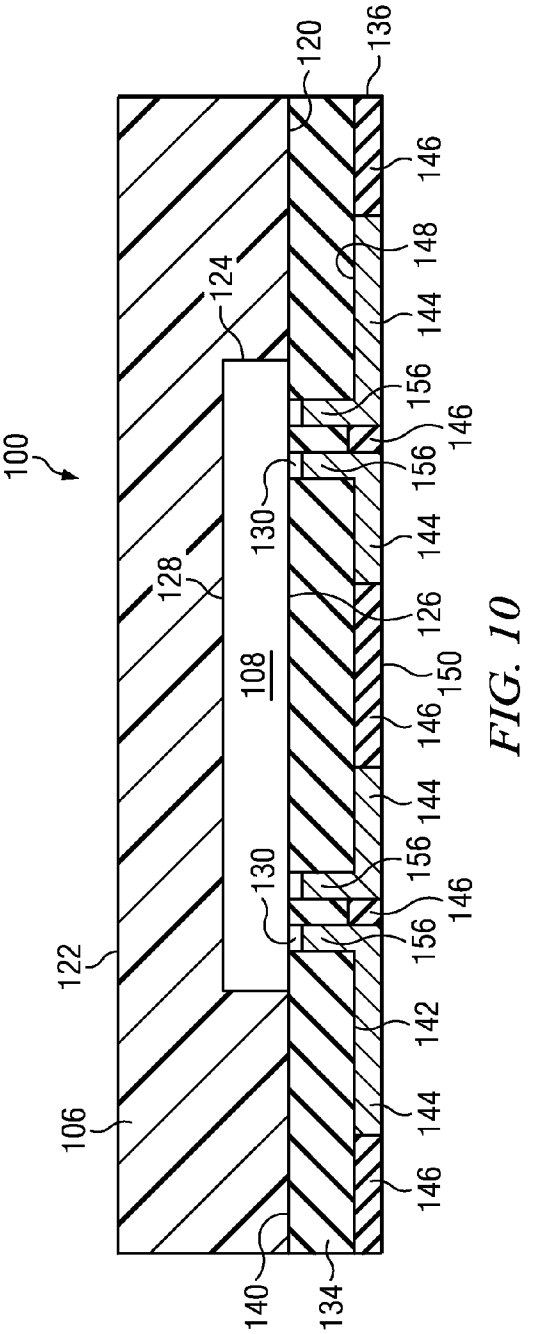
100
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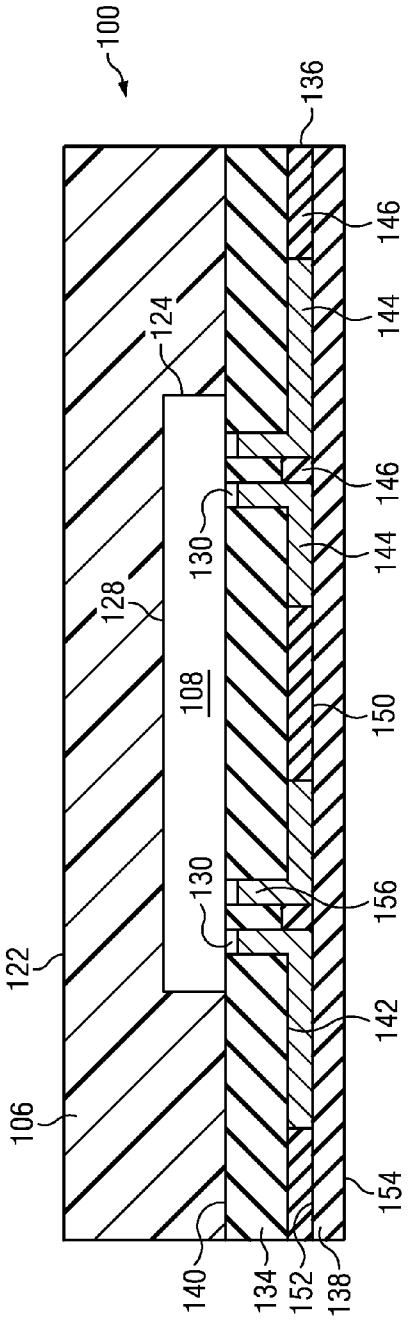
FIG. 10


100
136
146
144
124
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150
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156
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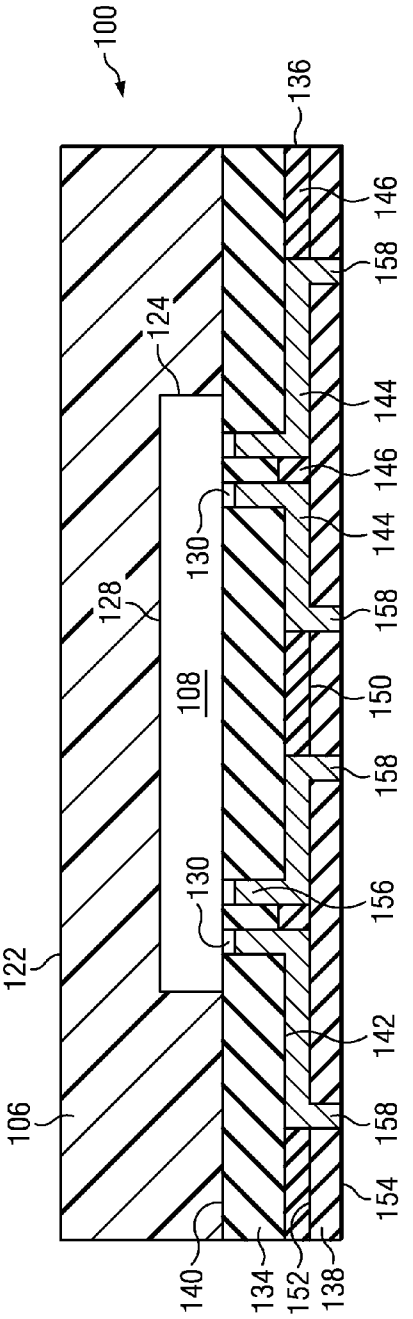
152
138

FIG. 11


100
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154
140
134
152
138

FIG. 12

INTEGRATED CIRCUIT AND METHOD OF MAKING

[0001] This patent application claims priority to U.S. provisional patent application 61/538,365 filed on Sep. 23, 2011 for PERMANENT CARRIER AND PACKAGE INTERCONNECT METHOD USING MOLD AND DISTRIBUTE APPROACH and U.S. provisional patent application 61/596,617 for INTEGRATED CIRCUIT AND METHOD OF MAKING filed on Feb. 8, 2012, which are both incorporated by reference for all that is disclosed therein.

BACKGROUND

[0002] Conventional integrated circuits have a die, which is a small circuit, electrically and/or mechanically connected to a lead frame or other connection mechanism. The electrical connection between the die and the lead frame typically consists of wire bonds connected between conductive pads on the die and conductors on the lead frame. The wire bonds are very small and delicate such that a small force applied to a wire bond can damage it. Therefore, extreme care must be taken when handling a circuit having wire bonds connected thereto. In addition to being very delicate, the wire bonds take time to connect, so they add to the cost and manufacturing time of the integrated circuit.

[0003] Many high speed and high frequency circuit applications require short leads connecting a die to a lead frame. Short leads reduce the chance of the die encountering electromagnetic interference and they affect the parasitic inductance and capacitance associated with the leads. Wire bonds are relatively long and add to the parasitic capacitance and inductance of the connection between the die and the lead frame of an integrated circuit. Wire bonds are also susceptible to electromagnetic interference.

[0004] After a conventional die is connected to a lead frame, the integrated circuit is encapsulated with an encapsulant. The encapsulation process is typically the final or near the final stage of fabrication of the integrated circuit. The encapsulant prevents contaminants from interfering with the integrated circuit. For example, the encapsulant prevents moisture from contaminating the die. The encapsulant also prevents the wire bonds from being damaged. Until the integrated circuit is encapsulated, the die, wire bonds, and other components are subject to failure by contact with contaminants. It follows that great care must be taken during the fabrication process in order to prevent the integrated circuits from being damaged prior to encapsulation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a side, cutaway view of an embodiment of an integrated circuit.

[0006] FIG. **2** is an enlarged view of a portion of the printed wiring board of the circuit of FIG. **1**.

[0007] FIG. **3** is a flow chart describing an embodiment of a method of fabricating the circuit of FIG. **1**.

[0008] FIG. **4** is a side elevation view of the circuit of FIG. **1** in the process of being fabricated wherein the die therein has been encapsulated.

[0009] FIG. **5** is a bottom plan view of the circuit of FIG. **4**.

[0010] FIG. **6** is a flow chart describing an embodiment of a method of affixing the first dielectric layer to the circuit of FIG. **1**.

[0011] FIG. **7** is a side elevation view of a first dielectric layer adhered to a sacrificial carrier.

[0012] FIG. **8** is a side elevation view of the dielectric layer and the sacrificial carrier of FIG. **7** affixed to the circuit of FIG. **4**.

[0013] FIG. **9** is a side elevation view of the circuit of FIG. **8** with the sacrificial carrier removed and with holes for vias formed in the first dielectric layer.

[0014] FIG. **10** is a side elevation view of the circuit of FIG. **9** with a conductive layer applied to the first dielectric layer wherein the conductive layer is connected to the vias.

[0015] FIG. **11** is a side elevation view of the circuit of FIG. **10** with the addition of a second dielectric layer.

[0016] FIG. **12** is a side elevation view of the circuit of FIG. **11** with vias formed through the second dielectric layer.

SUMMARY

[0017] Integrated circuits and methods of fabricating circuits are disclosed herein. One embodiment of an integrated circuit includes a die having a side, wherein a connection point is located on the side. A dielectric layer having a first side, a second side, and at least one first via extending between the first side and the second side is attached to the side of the die so that the first side of the dielectric layer is located adjacent the side of the die. A conductive layer is located adjacent the second side of the dielectric layer and the first via is electrically connected between the connection point and the conductive layer.

DETAILED DESCRIPTION

[0018] Integrated circuits (referred to herein simply as "circuits") and methods of making circuits are disclosed herein. FIG. **1** is a side, cutaway view of a circuit **100**. The circuit **100** includes an encapsulant **106**, a die **108**, a printed wiring board **110**, and a connection mechanism **112**. Embodiments of methods for fabricating the circuit **100** are described in greater detail further below.

[0019] The encapsulant **106** may be a conventional encapsulant commonly used to encapsulate integrated circuits or electronic devices. In some embodiments, the encapsulant **106** is applied by a transfer mold process. The encapsulant **106** has a first side **120** and a second side **122** located opposite the first side **120**. A void **124** that is sized to receive the die **108**, as described in greater detail below, is located in the first side **120**. In many embodiments, the encapsulant **106** is molded around the die **108**, so the void **124** is a recessed portion of the encapsulant **106** that is formed at the location of the die **108** during the encapsulation process.

[0020] The die **108** may be a conventional die that is commonly used in integrated circuits. The die **108** has a first side **126** and an opposite second side **128**. The first side **126** of the die **108** forms a substantially continuous flat surface with the first side **120** of the encapsulant **106**. Circuits and/or electronic devices (not shown) may be located in or on the die **108** in a conventional manner. For example, electronic devices may be fabricated on the second side **128**. A plurality of conductive pads **130** is located on the first side **126**. The conductive pads **130** serve to electrically connect the die **108** to external devices or conductors. The conductive pads **130** may be very thin relative to other components of the circuit **100**, however, for illustration purposes, they are shown as being substantially thick.

[0021] The printed wiring board **110** is adhered to or fabricated to the first side **126** of the die **108** and may also be adhered to or fabricated to the first side **120** of the encapsulant

106. The printed wiring board 110 may contain several layers. In the embodiment of FIG. 1, the printed wiring board 110 has three layers, a first dielectric layer 134, a conductive layer 136, and a second dielectric layer 138. The printed wiring board 110 may be fabricated separate from the circuit 100 and applied to the die 108 and the encapsulant 106 as a completed assembly. In other embodiments, the printed wiring board 110 is fabricated onto the die 108 and the encapsulant 106. Both fabrication methods are described below.

[0022] An enlarged view of the printed wiring board 110 is shown in FIG. 2. The first dielectric layer 134 has a first side 140 and a second side 142. The first side 140 is attached to or adhered to the first side 126 of the die 108, FIG. 1, and may also be attached to or adhered to the first side 120 of the encapsulant 106. The conductive layer 136 may be substantially similar to a redistribution layer in a die. The conductive layer 136 includes conductive material 144, such as copper, that serves as traces and nonconductive material 146 that is located between the conductive traces. The conductive material 144 may be metal, such as a copper foil similar or identical to copper foil used in subtractive processing, or plated in semi-additive or full additive form. An example of a copper foil includes a one half to two ounce copper foil. In other embodiments, the conductive material 144 may be a foil having several layers, such as a copper/aluminum/copper foil. The conductive layer 136 has a first side 148 and a second side 150, wherein the first side 148 is attached to or adhered to the second side 142 of the first dielectric layer 134. The nonconductive material 146 may be portions of either the first dielectric layer or the second dielectric layer 138. The second dielectric layer 138 has a first side 152 and a second side 154, wherein the first side 152 is attached to or adhered to the second side 150 of the conductive layer 136. Both the first dielectric layer 134 and the second dielectric layer 138 may be insulating materials that are commonly used in circuits.

[0023] The printed wiring board 110 serves to electrically and/or mechanically connect the die 108 to the connection mechanism 112. In order to achieve the electrical connections, a plurality of traces and vias may be located within the printed wiring board 110 to electrically connect the die 108 to the connection mechanism 112. As shown in FIGS. 1 and 2, the first dielectric layer 134 has a plurality of vias 156 extending between the first side 140 and the second side 142. The vias 156 electrically connect the conductive pads 130 on the die 108 to the conductive material 144 in the conductive layer 136 of the printed wiring board 110. The conductive layer 136 provides electrical conducting points at specific locations for the connection mechanism 112 by way of the conductive material 144. In the embodiment of FIGS. 1 and 2, vias 158 extend through the second dielectric layer 138 between the conductive layer 136 and the second side 154 of the second dielectric layer 138. It is noted that the connection mechanism 112 is electrically connected to the vias 158. Therefore, the connection mechanism 112 is electrically connected to the conductive pads 130 on the die 108.

[0024] The connection mechanism 112 may include a plurality of solder balls 160 that are electrically and mechanically connected to a plurality of conductors 162. The conductors 162 may be substantially similar to under bump metal layers used in semiconductor fabrication. The conductors 162 are electrically connected to the vias 158. It follows that electrical connections extend between the solder balls 160 and the conductive pads 130 on the die 108. It is noted that the solder balls 160 and conductors 162 are examples of devices for connecting the vias 158 to external devices and that other devices, such as pins or wire bonds, may be used to electrically connect the vias 158 to external devices.

[0025] Having described the structure of the circuit 100, methods of fabricating the circuit 100 will now be described. Reference is made to the flow chart 300 of FIG. 3, which describes a method of fabricating the circuit 100. Other fabrication methods are described further below.

[0026] The fabrication of the circuit 100 commences with providing the die 108 as described at step 304 of the flow chart 300. The die 108 is a conventional circuit that is fabricated onto a wafer or substrate. The die 108 may be of a type commonly used in integrated circuits. The die 108 may be a complete circuit meaning that no further circuit fabrication is required. However, the die 108 does need to be electrically connected to the connection mechanism 112 in order to power the die 108 and to send and receive signals as described below. As described above, the die 108 has connection points or conductive pads 130 that serve to electrically connect the die 108 to the connection mechanism 112.

[0027] The die 108 is encapsulated with the encapsulant 106 as described in step 306. The encapsulated die 108 is shown in FIG. 4, which is a side, cutaway, elevation view of the die 108 and the encapsulant 106. A bottom plan view of the encapsulated circuit 100 of FIG. 4 is shown in FIG. 5. The encapsulant 106 may be a conventional encapsulant used in the fabrication of integrated circuits. In some embodiments, a transfer mold technique is used to encapsulate the die 108. Encapsulating the die 108 at this stage of fabrication is unique. In conventional circuits, dies are not encapsulated until they are electrically connected to a connector or other connection device. For example, in flip-chip fabrication, the encapsulation process does not occur until a printed wiring board has been attached to the die. By encapsulating the die 108 at this stage of fabrication of the circuit 100, the die 108 may be handled or otherwise maneuvered with a lower probability of being damaged. The encapsulated die 108 is also less likely to become damaged by contaminants.

[0028] In the embodiments described herein, the entire die 108 except for the first side 126 is encapsulated. By encapsulating the die 108, except for the first side 126, at this point during fabrication, the die 108 is protected and the pads 130 are accessible in order to connect the die 108 to the connection mechanism 112. As shown in FIGS. 4 and 5, the encapsulant 106 may extend beyond the first side 126 of the die 108, which enables the completed circuit 100 to fit into larger packages. A first edge 172 of the encapsulant and a first edge 125 of the die 108 are spaced apart a distance 170. A second edge 176 of the encapsulant 106 and a second edge 127 of the die 108 are separated by a distance 174 as shown in FIG. 5. The distances 170, 174 determine the size of the first side 120 of the encapsulant 106, which may be substantially planar. The die 108 may be located in the encapsulant 106 in such a manner that the first side 126 of the die 108 and the first side 120 of the encapsulant 106 form a substantially planar and continuous surface.

[0029] The encapsulant 106 may be applied to the die 108 by different methods. For example, a liquid encapsulant may be molded over the die 108 and cured in a conventional manner. In other embodiments, a solid encapsulant may be formed with the void 124 located therein. The die 108 may be secured within the void 124 so that the die 108 is effectively encapsulated by the encapsulant 106. In yet other embodiments, the encapsulant 106 is cured simultaneously with the

curing of the printed wiring board **110** or components in the printed wiring board **110**. In such embodiments, the encapsulant **106** may be cured to a stage-B or jell state at this stage of fabrication. After the printed wiring board **110** is attached to the die **108** and the encapsulant **106**, the encapsulant **106** and components in the printed wiring board **110** may then be cured simultaneously. The simultaneous curing may enhance the bond between the printed wiring board **110** and the encapsulant **106**. For example, the encapsulant **106** and the first dielectric layer **134** are able to flow together in their jell state and then fully cure together.

[0030] Several different embodiments of applying the printed wiring board **110** to the die **108** will be described below. It is noted that the printed wiring board **110** replaces conventional wire bonds. Therefore, none of the embodiments of the circuit **100** described herein require wire bonds or the like between the die **108** and the connection mechanism **112**. Accordingly, all the embodiments of the printed wiring board **110** enable very short distances between the die **108** and the connection mechanism **112**, which reduces the parasitic capacitance and inductance associated with the electrical connection between the die **108** and the connection mechanism **112**.

[0031] A first embodiment of applying the printed wiring board **110** to the circuit **100** commences with applying the first dielectric layer **134** to the circuit as described at step **308** of the flow chart **300**. The application of the first dielectric layer **134** is described in greater detail by the flow chart **350** of FIG. **6**. Reference is made to FIG. **7**, which shows the first dielectric layer **134** adhered to a sacrificial carrier **177** as described in step **352** of the flowchart **350**. The first dielectric layer **134** may be laminated to the sacrificial carrier **177** by a conventional low temperature vacuum lamination process. The first dielectric layer **134** may be a non-fibrous dielectric material, such as an Ajinomoto build-up film (ABF), produced by Ajinomoto Fine-Techno Co, Inc of Japan and Ajinomoto North America, Inc. of Fort Lee, N.J., USA. The first dielectric layer **134** may have a thickness of between ten and fifty microns. The material used in the first dielectric layer **134** may have a low viscosity prior to being cured. In order to keep the first dielectric layer **134** from sliding off the sacrificial layer **177** when it is in a state having a low viscosity, the first dielectric layer **134** may be cured to a B-stage wherein the first dielectric layer **134** has the viscosity of a jell. Such a curing enables the first dielectric layer **134** to be transported by way of the sacrificial carrier **177** and be adhered to the encapsulant **105** and die **108** as described below.

[0032] The sacrificial carrier **177** may be a metal, such as a copper foil. In some embodiments, the sacrificial carrier **177** is a one half to two ounce copper foil. In other embodiments, the sacrificial layer **177** may be a foil having several layers, such as a copper/aluminum/copper foil. The sacrificial carrier **177** has a first side **178** and a second side **179**, wherein the first side **178** is adhered to or located adjacent the second side **142** of the first dielectric layer **134**. The sacrificial carrier **177** is used to apply the first dielectric layer **134** to the encapsulant **106** and the die **108** by forming a rigid carrier to support the first dielectric layer **134** so that it can be pressed against the encapsulant **106** and the die **108**.

[0033] At this stage of fabrication, the first dielectric layer **134** is adhered to the sacrificial carrier **177**. The first dielectric layer **134** may then be transported or handled by using the sacrificial carrier **177**, which reduces the likelihood of damage to the first dielectric layer **134** during handling. The jell state of the first dielectric layer **134** enables it to be applied to the circuit **100** as described at step **354** of the flow chart **350**, which yields the circuit **100** as shown in FIG. **8**. For example, the die **108** and the encapsulant **106** may be pressed onto the first dielectric layer **134**. It is noted that in some embodiments, a large sheet of a first dielectric layer is adhered to a plurality of dies, which are singulated during a later stage of fabrication.

[0034] The partially cured jell state of the first dielectric layer **134** enables it to be easily adhered to or located adjacent all the die **108** and the encapsulant **106** and reduces or eliminates the potential for voids between surfaces. More specifically, if the encapsulant **106** is in a jell state, first dielectric layer **134** and the encapsulant **106** may flow together for better adhesion. The conductive pads **130** may be embedded into the jelled first dielectric layer **134**. The first dielectric layer **134** and the encapsulant **106** may then be cured simultaneously as described at step **356** of the flow chart **350**.

[0035] The circuit **100** at this point in the fabrication process has the first dielectric layer **134** and the encapsulant **108** cured with the first dielectric layer **134** adhered to the die **108** and/or the encapsulant **108**. The sacrificial carrier **177** is then removed as described in step **358** of the flow chart **350**. In some embodiments, the sacrificial carrier **177** is etched away by a conventional etching process. The resulting circuit **100** is shown in FIG. **9**. As shown, the circuit **100** has the first dielectric layer **134** affixed thereto and the sacrificial layer **177** has been removed. As further shown in FIG. **9**, holes for the vias **156** are formed into the first dielectric layer **134** proximate the conductive pads **130** as described in step **360** of the flow chart **350**. In one embodiment, a laser is used to form the holes. In other embodiments, the holes for the vias **156** are drilled or formed using chemicals.

[0036] The holes for the vias **156** are plated or otherwise filled with a conductive material as described in step **362** of the flow chart **350**. For example, a plating material may be applied to the first dielectric layer **134** in order to form conductive paths in the vias **156**. Other methods may also be used to provide a conductive material to form the vias **156**. For example, in some embodiments, the conductive material for the vias **156** is formed when the conductive layer **136** is applied to the first dielectric layer **134**.

[0037] The conductive layer **136** is applied to the first dielectric layer as described in step **310** of the flow chart **300** of FIG. **3**. The conductive layer **136** may be applied in a manner similar to the manner in which a redistribution layer is applied to an integrated circuit. For example, a resist (not shown) may be applied to the second side **142** of the first dielectric layer **134**. It is noted that if the holes for the vias **156** have not been plated, no resist may be applied proximate the holes. The conductive layer **136** may then be applied to the second side **142** of the first dielectric layer **134** by a conventional technique, such as plating. The conductive material **144**, FIG. **2**, will adhere to the first dielectric layer **134** in locations where the resist is not present, which may include the holes for the vias **156**. The resulting circuit **100** is shown in FIG. **10**, which shows the conductive material **144** in the conductive layer **136** connected to the vias **156**.

[0038] In some embodiments, the circuit **100** as shown in FIG. **10** is complete. The circuit **100** is functional and may be connected to other devices by way of the printed wiring board **110**. For example conductors may be connected to the conductive layer **136** in order to electrically connect the circuit **100** to other components.

[0039] In other embodiments of the circuit **100**, the second dielectric layer **138** is affixed to the conductive layer **136** as described in step **312** of the flow chart **300** and as shown in FIG. **11**. As described above, the second dielectric layer **138** has a first side **152** and a second side **154**, wherein the first side **152** is adhered to or attached to the conductive layer **136**. The second dielectric layer **138** may be substantially the same material as the first dielectric layer **134**. The second dielectric layer **138** serves to protect the conductive layer **136** from damage during handling and from debris or other matter that may short or otherwise damage the conductive layer **134**. In addition, the second dielectric layer **138** serves to support the connection mechanism **112**.

[0040] The vias **158** are formed in the second dielectric layer **138** as described in step **314** of the flow chart **300** and as shown in FIG. **12**. The vias **158** extend between the first side **152** and the second side **154** of the second dielectric layer **138**. The vias **158** are fabricated by forming holes through the second dielectric layer **138** wherein the holes contact specific portions of the conductive material **144** of the conductive layer **136**. The holes may be formed in the same way as the holes that are formed in the first dielectric layer **134** to fabricate the vias **156**. Likewise, the holes may be filled with or plated with a conductive material to form the vias **158** in a manner similar to the way the vias **156** are formed.

[0041] The circuit **100** now has an encapsulated die **108** with electrical connections from the die **108** to the second side **154** of the second dielectric material **138**. The connection mechanism **112** may now be affixed to the second side **154** of the second dielectric material **138** as described in step **316** of the flow chart **300** and as shown in FIG. **1**. The connection. mechanism **112** electrically and/or mechanically connects the circuit **100** to other devices. For example, the connection mechanism **112** may provide input and output signals to and from the die **108**. The connection mechanism **112** may also enable the circuit **100** to be physically attached to a substrate (not shown), such as a printed circuit board, or other physical structure.

[0042] As briefly described above, the connection mechanism **112** may include a plurality of conductors **162** that are attached to the second side **154** of the second dielectric layer **138**. The conductors **162** are electrically connected to the vias **158** in order to provide electrical connections to the die **108**. The conductors **162** may be conventional metal layers, such as under bump metal layers that are commonly used to support solder balls **160**. The solder balls **160** may be attached to the conductors **162** in a conventional manner.

[0043] The circuit **100** has many advantages over conventional integrated circuits. For example, the circuit **100** was encapsulated early in the production process. Therefore, the circuit **100** may be handled and maneuvered with a lower probability of becoming damaged during the remaining production processes. In addition, the circuit **100** is less susceptible to damage from contaminants during production.

[0044] Electrically, the circuit **100** has many benefits over conventional integrated circuits. The circuit **100** does not require any wire bonds. Therefore, the circuit **100** is not subject to the increased parasitic capacitance or inductance associated with wire bonds. In addition, the conductive layer **136** enables the lead lengths between the conductive pads **130** on the die **108** and the connection mechanism **112** to be very short. The short distance reduces the electromagnetic interference that the circuit **100** is subject to. It follows that the circuit **100** is better suited to operate in high frequency, high speed, and low power applications.

[0045] Having described some embodiments of fabricating the circuit **100**, other embodiments, will now be described. In some embodiments, the first dielectric layer **134** is applied directly to the die **108** and the encapsulant **106** without the use of the sacrificial carrier **177**, FIG. **7**. In such an application, the circuit **100** may be positioned so that the first side **120** of the encapsulant **106** and the first side **126** of the die **108** are facing up. The first dielectric layer **134** may then be applied to the first surface **120** of the encapsulant **106** and the first surface **126** of the die **108**. The first dielectric layer **134** may then be cured wherein the curing may also simultaneously cure the encapsulant **106**. Fabrication of the circuit **100** may continue from step **360** of the flow chart **350** as described above.

[0046] In another embodiment of the fabrication process, the first dielectric layer **134** is adhered directly to the conductive layer **136** instead of being adhered to the sacrificial carrier **177**, FIG. **7**. No sacrificial carrier **177** is required to be removed in this embodiment. Rather, the conductive layer **136** and, more specifically, the conductive material **144** of the conductive layer **136**, serves as a carrier for the first dielectric layer **134**. The conductive material **144** may then be etched to form the conductive layer **136**. The vias **156** may be formed as described above. The vias **156** may also be plated so that they electrically connect with the conductive material **144** of the conductive layer **136**.

[0047] In other embodiments, heat spreaders are used in conjunction with or as an alternative to the encapsulant **106**. For example, the die **108** may be located in a heat spreader prior to encapsulation. Alternatively, the die **108** may be located in a heat spreader in lieu of encapsulation.

[0048] While illustrative and presently preferred embodiments of the invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed and that the appended claims are intended to be construed to include such variations except insofar as limited by the prior art.

What is claimed is:

1. A circuit comprising:

a die having a side, wherein a connection point is located on said side;

a first dielectric layer having a first side, a second side, and at least one first via extending between said first side and said second side, wherein said first side of said first dielectric layer is located proximate said side of said die, and wherein said first via is electrically connected to said connection point; and

a conductive layer having a first side and a second side, wherein said first side is located adjacent said second side of said first dielectric layer, at least a portion of said conductive layer being electrically connected to said first via.

2. The circuit of claim **1**, wherein said first dielectric layer is adhered to said side of said die.

3. The circuit of claim **1**, and further comprising a connection mechanism electrically connected to at least a portion of said conductive layer.

4. The circuit of claim **1**, wherein at least a portion of said die is encapsulated with an encapsulant.

5. The circuit of claim **4**, wherein at least a portion of a said first dielectric layer contacts said encapsulant.

6. The circuit of claim **1** and further comprising a second dielectric layer having a first side and a second side, wherein said first side is located adjacent said conductive layer, wherein said second dielectric layer has a second via extending between said first side and said second side, and wherein said second via is electrically connected to said conductive layer.

7. The circuit of claim **6**, and further comprising a connection mechanism electrically connected to at said second via.

8. The circuit of claim **7**, wherein said connection mechanism is mechanically connected to said second dielectric layer.

9. A method of fabricating a circuit, said method comprising:

providing a die, said die having a side, wherein a connection point is located on said side;

affixing a first dielectric layer to said first side of said die, said first dielectric layer having a first side and a second side, wherein said first side of said first dielectric layer is affixed to said side of said die; and

forming a first via through said first dielectric layer between said first side and said second side, wherein said first via is electrically connected to said connection point.

10. The method of claim **9** and further comprising encapsulating said die prior to said affixing said first dielectric layer to said side of said die wherein said encapsulating comprises substantially encapsulating said die, except for said side.

11. The method of claim **9**, and further comprising locating said die proximate a heat spreader.

12. The method of claim **9** and wherein said first dielectric layer is affixed to said die in an uncured state and further comprising:

applying an uncured encapsulant to said die; and

curing said encapsulant and said first dielectric layer simultaneously.

13. The method of claim **9**, wherein said first dielectric layer has a conductive layer affixed to said second side and further comprising electrically connecting said conductive layer to said first via.

14. The method of claim **13** and further comprising:

affixing a second dielectric layer to said conductive layer, said second dielectric layer having a first side and a second side, wherein said first side of said second dielectric layer is located adjacent said conductive layer; and

forming a second via between said conductive layer and said second side of said second dielectric layer.

15. The method of claim **14** and further comprising affixing a connection mechanism to said second side of said second dielectric layer, said connection mechanism being electrically connected to said second via.

16. The method of claim **9**, wherein said affixing a first dielectric layer comprises affixing a first dielectric material to a carrier and applying said dielectric material with said carrier to said side of said die.

17. The method of claim **16** and further comprising removing said carrier.

18. A method of fabricating a circuit, said method comprising:

encapsulating a die with encapsulant except for a first side of said die; and

after said encapsulating, attaching a dielectric substrate to said die and said encapsulant.

19. The method of claim **18**, and further comprising electrically connecting said die to a connection mechanism using conductive material that extends through said dielectric substrate.

20. The method of claim **19** wherein said electrically connecting comprises attaching a conductive layer to one side of said dielectric substrate after said attaching said dielectric substrate to said die and said encapsulant.

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