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(71) Applicant *(for all designated States except US)*: **EPCOS AG** [DE/DE]; St.-Martin-Str. 53, 81669 Munich (DE).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **VAN DEN OEVER, Léon C. M.** [NL/NL]; Heintje Davidsstraat 1, NL-5247 XG Rosmalen (NL). **BALM, Bart** [NL/NL]; Vissersstraat 31, NL-6579 AP Kekerdom (NL). **BOUWMAN, Jeroen** [NL/NL]; Groenestraat 67, NL-6679 EC Oosterhout (Nijmegen) (NL).

(74) Agent: **EPPING HERMANN FISCHER PATENTANWALTSGESELLSCHAFT MBH**; Ridlerstr. 55, 80339 Munich (DE).

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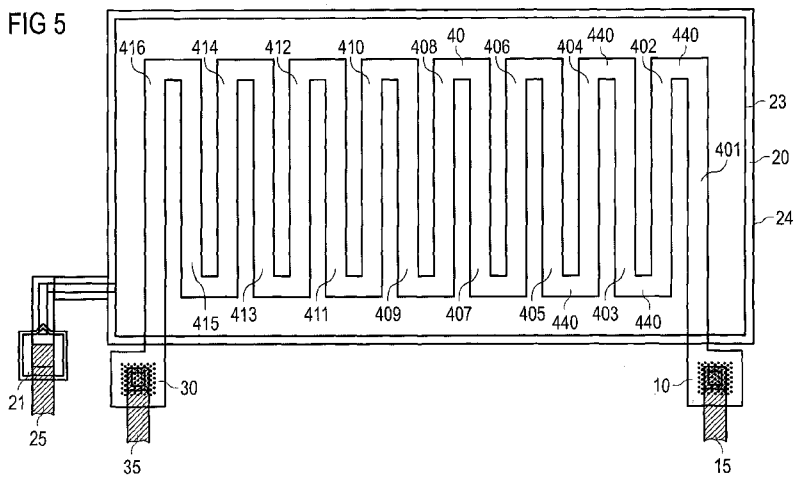
(54) Title: pHEMT HAVING A CHANNEL LENGTH LARGER THAN THE CHANNEL WIDTH

FIG 5



(57) Abstract: A semiconductor device comprises a pHEMT which comprises a source (30), a drain (10) and a channel region (40) running between the source (30) and the drain (10), the channel region (40) being located at least partly beneath a gate electrode (20), the channel region (40) having a channel length and a channel width, the channel length being the total length of the channel region (40) which is located beneath the gate electrode (20), the channel width being a width of the channel region (40) beneath the gate electrode (20), wherein the channel length is equal or larger than the channel width.

Description

pHEMT HAVING A CHANNEL LENGTH LARGER THAN THE CHANNEL WIDTH

The invention concerns a semiconductor device comprising a pHEMT.

Semiconductor circuits which are formed in GaAs technology may comprise current sources and active loads. In a conventional circuit a high ohmic resistor, for example a thin film resistor or TFR, which gives low current consumption, requires a large amount of chip area. This may be acceptable if only a few high ohmic resistors are provided. For a larger number of high ohmic resistors it may be no longer competitive due to the pressure on integration and cost and size reduction. A resistor with smaller occupied area has less resistance and causes higher current consumption.

Merged or stacked FET-HBT integration schemes, often called BiFET or BiHEMT and containing both HBT and FET or pHEMT device on a single GaAs substrate, are reported in the following papers from the CS MANTECH Conference 2007: William Peatman, Mohsen Shokrani, Boris Gedzberg, Wojciech Krystek, and Michael Trippe: "InGaP-Plus$_{TM}$: Advanced GaAs BiFET Technology and Applications"; T. Henderson, J. Middleton, J. Mahoney, S. Varma, T. Rivers, C. Jordan, and B. Avrit: "High-Performance BiHEMT HBT / E-D pHEMT Integration"; Todd D. Basso and Richard B. Brown: "A Complementary GaAs Microprocessor for Space Applications"; Ravi Ramanathan, Mike Sun, Peter J. Zampardi, Andre G. Metzger, Vincent Ho, Cejun Wei, Peter Tran, Hongxiao Shao, Nick Cheng, Cristian Cismaru, Jiang Li, Shiaw Chang, Phil Thompson, Mark Kuhlman, Kenneth Weller: "Commercial Viability of a Merged HBT-FET (BiFET) Technology for GaAs Power Amplifiers"; C. K. Lin, T. C. Tsai, S. L. Yu, C. C. Chang, Y. T. Cho, J. C. Yuan, C. P. Ho, T. Y.

Chou, J. H. Huang, M. C. Tu, and Y. C. Wang: "Monolithic Integration of E/D-mode pHEMT and InGaP HBT Technology on 150-mm GaAs Wafers". A BiHEMT integration scheme is also reported in Thomas Apel, Tim Henderson, Yu-Lung Tang and Otto Berger "Efficient Three-State WCDMA PA Integrated with High-Performeance BiHEMT HBT/E-D pHEMT Process", 2008 Radio Frequency Integrated Circuits Symposium. An FET for amplifying is reported in US 5,952,860.

It is an aim to provide a component suitable for serving as a current source or as load, wherein the component shall operate at a low current and occupy small chip area.

For this aim a semiconductor device is provided. The semiconductor device comprises a pHEMT which comprises a source, a drain and a channel region running between source and drain, the channel region being located at least partly beneath a gate electrode, the channel region having a channel length and a channel width, the channel length being the total length of the channel region which is located beneath the gate electrode, the channel width being the width of the channel region beneath the gate electrode, wherein the channel length is equal or larger than the channel width.

A pHEMT or pseudomorphic high electron mobility transistor is a type of a field effect transistor or FET. The current, namely the current Ids between drain and source, of a FET scales with the ratio W/L, which means Ids is proportional to W/L, wherein W is the channel width and L is the channel length. Reducing the channel width W and/or increasing the channel length L causes reduction of the current.

The pHEMT having the channel length L>=W is a long-gate pHEMT, which may be used as a current source for low current generation or as an active load. This pHEMT occupies less chip

area than a conventional resistor, which may result in cheaper products.

The channel region comprises at least one portion which is located beneath the gate electrode. The total length is the sum of the lengths of the portions of the channel region which are located beneath the gate electrode.

Preferably, the channel region has a first end which is located adjacent to the drain and a second end which is located adjacent to the source, the portion between the first end and the second end is located beneath the gate electrode. In other words, the channel region is totally or essentially totally located beneath the gate electrode.

In one embodiment the channel length is significantly larger than the channel width, which means L>>W. This reduces the current consumption of the pHEMT significantly. In one embodiment the channel length is twice as large as the channel width. Preferably, the channel length is at least ten times as large as the channel width.

In one embodiment the channel length is larger than 0.5µm or one micrometer, which is significantly larger than the channel length of a conventional component.

In one embodiment the pHEMT is a depletion mode or D-mode type transistor, which means that it is conducting when Vgs is above a negative threshold (Vt), so it is on at Vgs=0V.

In one embodiment the pHEMT is formed in GaAs technology. The pHEMT may serve as an active load or a current source in an integrated circuit formed in GaAs technology.

Simple design rules yield a space saving layout for the long-gate pHEMT. In one embodiment the drain has a width which is larger than the channel width. Additionally or alternatively, the source has a width which is larger than the channel width. If the channel width is smaller than the widths of the drain and the source, the contour line around the drain, the source, and the channel region looks like a dog bone or dumbbell. The combination of reduced channel width and increased gate length results in reducing the ratio W/L which causes reduction of the current consumption.

In one embodiment the channel region located beneath the gate electrode comprises a first portion and second portion, the first and second portion extend between a first border area of an area which is located beneath the gate electrode and a second border area of the area which is located beneath the gate electrode, wherein the second border area is opposite to the first border area. In this embodiment the channel region does not extend straightly between the source and the drain. The channel region meanders, which means it runs back and forth. This is a space saving layout. The meandering channel region may run in curves. In one embodiment the meandering channel region has straight portions, wherein the edges of the portions touch at an angle, for example at a rectangular angle. In an alternative embodiment the channel region is formed as a spiral.

In one embodiment the gate electrode comprises a gate terminal which is located above the source. This reduces the chip area occupied by the pHEMT. Preferably, the gate electrode and the source are connected so that Vgs=0V, wherein Vgs is the voltage between the gate electrode and the source, so that the pHEMT has only two terminals. A potential can be applied to the gate and the source by means of the gate terminal.

Alternatively, the device maybe used with three terminals and a potential applied between gate and source.

The long-gate pHEMT is an attractive component for current sources and active loads in GaAs technology. Long-gate pHEMTs can be used in GaAs BiFET, combining HBT and pHEMT, as well as in GaAs pHEMT technology, or in other technologies.

For low current consumption and high equivalent small-signal resistance the ratio W/L is reduced. Also the layout may be enhanced by means of a dog-bone-shaped pHEMT, a meandering channel and a gate-source short, for example.

Further features and refinements become apparent from the following description of the exemplary embodiments in connection with the accompanying figures.

Figure 1 shows a schematic layout of an embodiment of a conventional pHEMT.

Figure 2 shows a schematic layout of an embodiment of a long-gate pHEMT.

Figure 3 shows an exemplary layout of an embodiment of a pHEMT, wherein the channel width is further reduced.

Figure 4 shows an exemplary layout of an embodiment comprising a multitude of pHEMTs according to figure 3.

Figure 5 shows an exemplary layout of an embodiment of a pHEMT having a meandering channel region.

Figure 6 shows an exemplary layout of an embodiment of a pHEMT having a channel region formed as a spiral.

Figure 7 shows an exemplary layout of an embodiment of a pHEMT having a gate terminal located above the source.

Figures 8A and 8B illustrate the application of a long-gate pHEMT in bias circuits.

Figures 9A and 9B illustrate the application of long-gate pHEMTs in a differential pair.

Figures 10A and 10B illustrate the application of a long-gate pHEMT in an inverter.

Figure 1 shows a schematic layout of a conventional pHEMT. The pHEMT or pseudomorphic high electron mobility transistor is a type of a FET or field effect transistor.

The pHEMT may be formed in a wafer which may be single or multi-layered and may comprise combinations of the group III-V elements, e.g. GaAs, AlGaAs, InGaAs, InGaP, AlAs, and the like, or combinations thereof. Preferably, the substrate comprises GaAs.

The pHEMT may comprise a layer stack (not shown in figure 1) including a substrate layer, e.g. GaAs, wherein a buffer layer, e.g. GaAs, may be arranged on the substrate layer. A channel layer, e.g. InGaAs, is provided. The channel layer may be sandwiched between a barrier layer, e.g. AlGaAs, and the buffer layer.

The pHEMT comprises a drain 10, a source 30, and a channel region 40. The channel region runs between the drain 10 and the source 30. In one embodiment the drain 10 and the source 30 comprise a further layer, e.g. GaAs, which is arranged on the barrier layer. This further layer is outside the channel

region 40. A drain contact 11 is located on the drain 10. A source contact 31 is located on the source 30.

The region outside a contour line 50 around the drain 10, source 30 and the channel region 40 is isolating. The pHEMT may be isolated by an implantation. Such an implantation may be accomplished through the use of a mask, which is formed by a photoresist. During manufacturing, the photoresist may be arranged on portions of the surface of the layer stack which are not to be isolated. In this embodiment the mask would be arranged on the area inside the contour line 50. The mask is removed after implantation. The isolation, maybe formed by the implantation, defines the width W of the channel region 40 between the source 30 and the drain 10.

The pHEMT further comprises a gate electrode 20, which is arranged over the channel region 40. During manufacturing, the further layer over the channel region may be removed, for example by etching. The gate electrode may be formed on the barrier layer over the channel region and defines the length L of the channel region 40 between the source 30 and the drain 10.

The channel region 40 has a channel width W, which is the width of the channel region 40, and a channel length L, which is the length of the channel region 40 located beneath the gate electrode 20. In this embodiment, the channel width W is larger than the channel length L. L may be 0.5µm for a standard pHEMT or much longer for a long-gate pHEMT and W may be 3µm.

A pipe-like channel for the flow of the current is formed along the channel region in the channel layer when operation potentials are applied to the drain contact 11, the source contact 31 and the gate electrode 20.

Figure 2 shows a schematic layout of a long-gate pHEMT which has a channel length L that is larger than the channel width W. This pHEMT also comprises a drain 10, a source 30 and a gate electrode 20.

The embodiment shown in figure 2 differs from the embodiment shown in figure 1 by the dimension of the channel region 40 which is covered by the gate electrode. The embodiment shown in figure 2 is a long-gate pHEMT, which means that the channel region 40 has a channel length L that is equal or larger than the channel width W. In one embodiment L is equal, but usually much larger than 0.5µm. An integrated device having such pHEMTs may be smaller than an integrated device having a layout which is based on pHEMTs having a gate length of 0.5µm.

In one embodiment the ratio W/L is smaller than 1. In a further embodiment the ratio W/L is smaller than 1/3. In a further embodiment the ratio W/L is smaller than 1/5. In a further embodiment the ratio W/L is smaller than 1/10. In a further embodiment the ratio W/L is smaller than 1/100. In a further embodiment the ratio W/L is smaller than 1/1000.

A depletion mode or D-mode pHEMT may be used as active load or current source. This pHEMT is a FET with a negative threshold voltage VT. As VT is mainly given by technology, typically about -1V, the current consumption may be changed by the layout.

The device characteristics like the current Ids between the drain 10 and the source 30 scales with the ratio W/L. High performance devices, which operate at high speed, with low noise and serve as low ohmic switch, have a short gate length, e.g. 0.5µm.

For reducing the current consumption the channel width W may be reduced and/or the channel length L may be enlarged. Such a long-gate pHEMT having a small ratio W/L may be suitable for operation with lower reference current which causes low power consumption and may serve as active load which has a high equivalent small-signal resistance.

Figure 3 shows an exemplary layout of a pHEMT which has a drain 10, a source 30 and a channel region 40 running between the drain 10 and the source 30. The surrounding region which is the region outside the contour line 50 around the drain 10, the source 30 and the channel region 40 is isolating.
A drain contact 11 is provided to which a potential can be applied by a first metal interconnect 15, for example. In one embodiment, the drain contact 11 is electrically connected through a via 27, which is formed in an isolated layer (not shown in figure 3) covering the drain 10, with a metal layer 28 (dotted) which is arranged on the drain 10. A source contact 31 is provided to which a potential can be applied by a second metal interconnect 35, for example. The source contact 31 may be connected with the source 30 in a similar way as described above.

A gate electrode 20 is arranged above the channel region 40. The gate electrode 20 has a gate terminal 21 to which a potential can be applied by a third metal interconnect 25, for example. In this embodiment the gate terminal 21 is located adjacent to the source 30. The gate electrode 20 and the gate terminal 21 may be made of metal, for example gold.

This embodiment is a long-gate pHEMT, wherein the channel length L is larger than the channel width W. Further, the width W of the channel region 40 is smaller than a width of the WD of the drain 10 and a width WS of the source 30. The

drain 10, the channel region 40, and the source 30 have a contour like a dog-bone.

Reducing the width of the source 30 and the drain 10 is limited by the size of the source/drain contacts 31, 11. The source/drain contacts 31, 11 have to be dimensioned so that the metal interconnects 35, 15 can be connected and manufactured in a reliable manner. Preferably, the source 30 and the drain 10 are formed so that the contacts 31, 11 are centered on the source 30 or the drain 10, which means that the source 30 and the drain 10 are larger than the contacts 31, 11. Forming a channel region 40 which has a smaller width W than the widths WD, WS of the drain 10 and the source 30 causes reduction of the ratio W/L which comes along with reduced current consumption in comparison with the pHEMT having a rectangular contour line 50 around the drain 10, the source 30 and the channel region 40.

Assuming that the widths WD, WS of the drain 10 and the source 30 are 7µm, a pHEMT having a rectangular contour line 50 has a channel width W=7µm. A pHEMT having a contour line 50 shaped like a dog-bone may have a channel width W=3µm. Thus, the current consumption of the latter is 7/3 times lower or for the same current consumption the occupied chip area is only 3/7 times, in comparison with the pHEMT having a rectangular contour line 50.

Figure 4 shows an exemplary layout which comprises a multitude of long-gate pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600, wherein the contour lines 50 of the drains 10, the sources 30 and the channel regions 40 are formed like dog-bones. In this embodiment sixteen pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600 are provided. The pHEMTs 100, 200, 300, 400, 500, 600, 700, 800,

900, 1000, 1100, 1200, 1300, 1400, 1500, 1600 are arranged in a row. The channel region 40 of the first pHEMT 100 is located adjacent to the channel region 40 of the second pHEMT 200. The drain 10 of the first pHEMT 100 is located adjacent to the source 30 of the second pHEMT 200. The source 30 of the first pHEMT 100 is located adjacent to the drain 10 of the second pHEMT 200. The drain 10 of the third pHEMT 300 is located adjacent to the source 30 of the second pHEMT 200. The source 30 of the third pHEMT 300 is located adjacent to the drain 10 of the second pHEMT 200, and so on. The odd-numbered pHEMTs 100, 300, 500, 700, 900, 1100, 1300, 1500 are orientated so that their sources 30 are directed to a first direction, which is the top of figure 4 in this embodiment. The drains 10 are directed to a second direction, which is the bottom of figure 4 in this embodiment. The even-numbered 200, 400, 600, 800, 1000, 1200, 1400, 1600 pHEMTs are orientated so that their drains 10 are directed to the first direction, and the sources 30 being directed to the second direction. In other words, each pHEMT is orientated contrariwise to the pHEMT or the pHEMTs which is or are located adjacent to this pHEMT.

A single gate electrode 20 is located above the channel regions 40 of the pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600. A gate terminal 21 is provided to which a potential can be applied.

The source contact 31 of the first pHEMT 100 is electrically coupled with the drain contact 11 of the second pHEMT 200. The source contact 31 of the second pHEMT is electrically coupled with the drain contact 11 of the third pHEMT. The source contact 31 of the third pHEMT 300 is electrically coupled to the drain contact 11 of the fourth pHEMT 400, and so on. Metal interconnections 5 are used for electrically coupling the drain and source contacts 11, 31 of neighbouring pHEMTs.

The embodiment shown in Figure 4 comprises a multitude of N=16 pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600, which are connected in series. N is the number of pHEMTs. Each channel region 40 has a channel length L, e.g. 40µm in this embodiment. This embodiment is equivalent to a pHEMT having a total channel length N*L=16*40µm=640µm and the same channel width as the dog-bone-shaped pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600.

Figure 5 shows a further exemplary layout of a pHEMT which comprises a drain 10, a channel region 40, and a source 30 running between the drain 10 and the source 30. The channel region 40 meanders. Meandering means that the channel region 40 comprises a multitude of portions 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, which run between a first border area of the area beneath the gate electrode 20 to a second border area of the area, wherein the first border area is opposite to the second border area. The channel region may comprise straight portions, wherein the portions touches at an angle, e.g. at a rectangular angle, as shown in figure 5. An alternative embodiment (not shown) has a meandering channel region 40 which runs in curves.

A first portion 401 of the channel region is located adjacent to a second portion 402 of the channel region. A third portion 403 of the channel region is located adjacent to the second portion 402 of the channel region, and so on. In this embodiment sixteen parallel portions 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 are provided. Each portion 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 has a top and a bottom. The top of the first portion 401 is connected with the top of the second portion 402 by a connecting portion 440 of the channel region. The bottom of the second portion 402 is

connected to the bottom of the third portion 403 by a connecting portion 440 of the channel region. The top of the third portion 403 is connected to the top of the fourth portion 404 by a connecting portion 440 of the channel region, and so on. The bottom of the first portion 401 extends to the drain 10. The bottom of the sixteenth portion 416 extends to the source 30. In this embodiment the connecting portions 440 are orientated essentially orthogonal with respect to the portions 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 which they connect.

A gate electrode 20 is arranged above the channel region 40. In this embodiment the gate electrode 20 comprises a first layer 23 and a second layer 24 arranged on the first layer. The second layer 24 is slightly larger than the first layer 23, so that the second layer 24 overlaps. In one embodiment the difference between the edges of the first and second layers 23, 24 is about 0.5µm.

The channel length L is the length of the meandering channel region 40 located beneath the gate electrode 20 which is formed as a plate. The channel width W is smaller than the width of the source 30 and the drain 10.

The layout shown in figure 5 is more efficient than the layout shown in figure 4. The layout shown in figure 4 comprises 16 pHEMTs 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600. Each pHEMT 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600 may have a channel length of 40µm, which causes a total length of the channels 16*40um=640µm. Assuming the layout shown in figure 5 has an equal or a similar vertical extension like the layout shown in figure 4, the channel region 40 may have 16 portions, a portion having a length of about 54µm. This includes the length of a straight portion

401, 402, 430, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 and a connection portion 440. The straight portions 401, 402, 430, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 shown in figure 5 are longer than the channel regions 40 shown in figure 4, because the layout shown in figure 4 comprises many sources 30 and drains 10 which require a lot of space. The channel length L in figure 5 is about 16*54µm=864µm. This means that the channel length in figure 5 is increased by the factor 1.35.

Moreover, the layout in figure 5 has a smaller horizontal extension than the layout shown in figure 4. In figure 4, the channel width is 3µm. The distance between two neighbouring channel regions 40 is 7µm due to required space of the sources and drains 30, 10. Thus, the channel region 40 horizontally extends over 16*(3µm+7µm)-7µm=153µm. In figure 5, the channel width W is also 3µm. The distance between two neighbouring straight channel portions 401, 402, 430, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416 is 3µm. The channel region 40 horizontally extends over 16*(3µm+3µm)-3µm=93µm. This means that the horizontal extension of the layout in figure 4 is increased by the factor 1.65 in comparison to the layout shown in figure 5.

Meandering and reducing the channel width reduce the occupied chip area. In one embodiment the saving of chip area compared with a multitude of long-gate pHEMTs having a rectangular contour line is about the factor 5≈7/3*1.35*1.65.

The meandering shape of the channel region causes a channel length L which is significantly larger than the channel width W. The principle of meandering creates a long and narrow channel region 40 running between the source 30 and the drain 10. The channel region 40 is fully covered by the overlaying gate electrode 20. A meandering channel region is an effective

way to reduce the chip area of a long-gate pHEMT. Alternatives with other shapes are also possible.

Figure 6 shows a further exemplary layout of a pHEMT comprising a drain 10 and a source 30. A channel region 40 runs between the drain 10 and the source 30. The channel region 40 is formed as a spiral. The embodiment of the spiral shown in figure 6 comprises straight portions, wherein two of the straight portions touch at a rectangular angle. One embodiment of a spiral (not shown) is rounded, which means the spiral is a curve which emanates from a central point, getting progressively farther away as it revolves around the point.

A gate electrode 20 is arranged over the channel region 40 and the source 30, which is located in the centre of the spiral. The drain 10 is located beyond the gate electrode 20. A gate terminal 21 is provided. The source 30 may be electrically connected to the gate electrode 20, which means that the voltage Vgs between the gate electrode 20 and the source 30 is Vgs=0.

The embodiment shown in figure 6 is a pHEMT which comprises two terminals 11, 21. This is contrary to the embodiments shown before, these embodiments having three terminals. One terminal is formed by a drain contact 11. The other terminal is formed by the gate terminal 21, which is electrically connected with the gate electrode 20 and the source 30.

The embodiments shown in figures 5 and 6 may serve as current sources which generate currents of about 1µA or a few microamperes. Compared to conventional devices, which include stacking of pHEMTs having a gate length of 0.5µm and a channel width of 7µm, for example, or the use of TFR resistors having about 50Ohm/square, the area saving is in the orders of magnitudes.

One embodiment of a pHEMT similar to the one shown in figure 5 may have a ratio L/W=729µm/3µm=243. Assuming the ratio L/W of an embodiment of a (standard) symmetric triple-0.5µm-gate pHEMT is L/W=2*3*0.5µm/7µm=0.43, 567 pHEMTs in series are needed for an equivalent L/W ratio as the long-gate pHEMT having the meandering channel region. Assuming the ratio L/W of an embodiment of a triple-0.5µm-gate pHEMT is L/W=3*0.5µm/3µm=0.5, 486 pHEMTs in series are needed for an equivalent L/W ratio as the long-gate pHEMT having the meandering channel region.

Figure 7 shows a further exemplary layout of a pHEMT, which comprises a drain 10, a source 30 and a channel region 40 located beneath a gate electrode 20. The contour line 50 of the drain 10, the channel region 40 and the source 30 is shaped like a dog-bone.

In this embodiment the gate terminal 21 is positioned over the source 30, wherein the gate electrode 20 and the source 30 are shorted. In one embodiment a metal layer is arranged on the surface of the source 30. The metal layer is connected with a stacked gate-source-contact through a via in an isolating layer located between the metal layer and the stacked gate-source-contact 31. The stacked gate-source-contact is formed by gate contact 21 which is arranged above or beneath the source contact 31. In an alternative embodiment the gate contact and the source contact are integrally formed which means that one contact is provided, the contact being connected with the gate electrode and with the metal layer. The pHEMT having a stacked gate-source contact is more compact than a pHEMT having three terminals.

It should be noted that in one embodiment (not shown) which has a spiral channel region 40 like the embodiment shown in figure 6, the gate terminal is located over the source 30.

This embodiment requires less chip area than the embodiment which is shown in figure 6.

The long-gate pHEMTs may be used in current sources and active loads, which may be used in circuit design in GaAs technology. The active loads and current sources are implemented by using D-mode pHEMTs.

A current source is used for example in bias circuits. The current source gives a specified and stable reference current. Figure 8A shows a diagram of a bias circuit with a current source generating Iref. Figure 8B shows a diagram of a bias circuit, wherein the current source is implemented by a D-mode pHEMT 101. The long-gate pHEMT is in particular suitable for generating low currents.

An active load is used for example as load in a differential pair or load in an inverter.

Figure 9A shows a diagram of a differential pair having load resistors R1 and R2. Figure 9B shows a diagram of a differential pair, wherein the load resistors have been replaced by active loads, which are D-mode pHEMTs 102, 103. The active loads consume less chip area than a resistor and have a higher voltage gain Av=gm*RL, wherein RL=d Vds/ d Ids. The current source which generates the current Itail in figure 9A is also replaced by a pHEMT 104.

Figure 10A shows a diagram of an inverter having a load resistor R4. Figure 10B shows a diagram of the inverter, wherein the load resistor R4 is replaced by an active load which is a D-mode pHEMT 105.

Other implementations are within the scope of the claims. Elements of different embodiments may be combined to form implementations not specifically described herein.

Reference numerals

5, 15, 25, 35	metal interconnect
10	drain
11	drain contact
20	gate electrode
21	gate terminal
23	first layer
24	second layer
27	via
28	metal layer
30	source
31	source contact
40	channel region
50	contour line
401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416	portion of channel region
440	connection portion
100, 200, 400, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600,	
101, 102, 103, 104, 105	pHEMT
L	channel length
R1, R2, R3, R4, R5	resistor
W	channel width
WD	drain width
WS	source width

Claims

1. Semiconductor device comprising a pHEMT which comprises a source (30), a drain (10), and a channel region (40) running between the source (30) and the drain (10), the channel region (40) being located at least partly beneath a gate electrode (20), the channel region (40) having a channel length (L) and a channel width (W), the channel length (L) being the total length of the channel region (40) which is located beneath the gate electrode (20), the channel width (W) being the width of the channel region (40) beneath the gate electrode (20), wherein the channel length (L) is equal or larger than the channel width (W).

2. Semiconductor device according to claim 1, wherein the channel region (40) has a first end which is located adjacent to the drain (10) and a second end which is located adjacent to the source (30), the portion of the channel region (40) between the first end and the second end being located beneath the gate electrode (20).

3. Semiconductor device according to claim 1 or 2, wherein the channel length (L) is significantly larger the channel width (W).

4. Semiconductor device according to any of the claims 1 to 3, wherein the channel length (L) is larger than 0.5µm.

5. Semiconductor device according to any of the claims 1 to 4, wherein the pHEMT is a depletion mode transistor.

6. Semiconductor device according to any of the claims 1 to 5, wherein the pHEMT is formed in GaAs technology.

7. Semiconductor device according to any of the claims 1 to 6, wherein the drain (10) has a width (WD) which is larger than the channel width (W).

8. Semiconductor device according to any of the claims 1 to 7, wherein the source (30) has a width (WS) which is larger that the channel width (W).

9. Semiconductor device according to any of the claims 1 to 8, wherein the channel region (40) located beneath the gate electrode (20) comprises a first portion (401) and second portion (402), the first and second portions (401, 402) extending between a first border area of an area which is located beneath the gate electrode (20) and a second border area of the area, wherein the second border area is opposite to the first border area.

10. Semiconductor device according to any of the claims 1 to 9, wherein the channel region (40) runs in a meandering way.

11. Semiconductor device according to any of the claims 1 to 10, wherein the channel region (40) is formed as a spiral.

12. Semiconductor device according to any of the claims 1 to 11, wherein the gate electrode (20) comprises a gate terminal which is located above the source (30).

13. Semiconductor device according to claim 12, wherein the gate electrode (20) and the source (30) are bypassed.

FIG 1

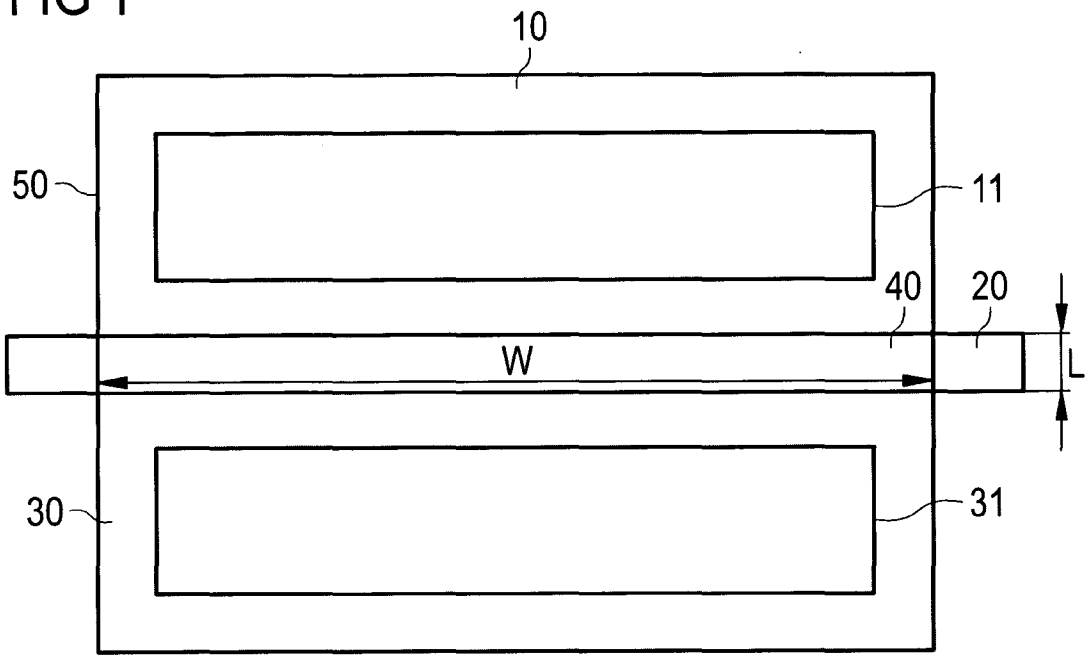


FIG 2

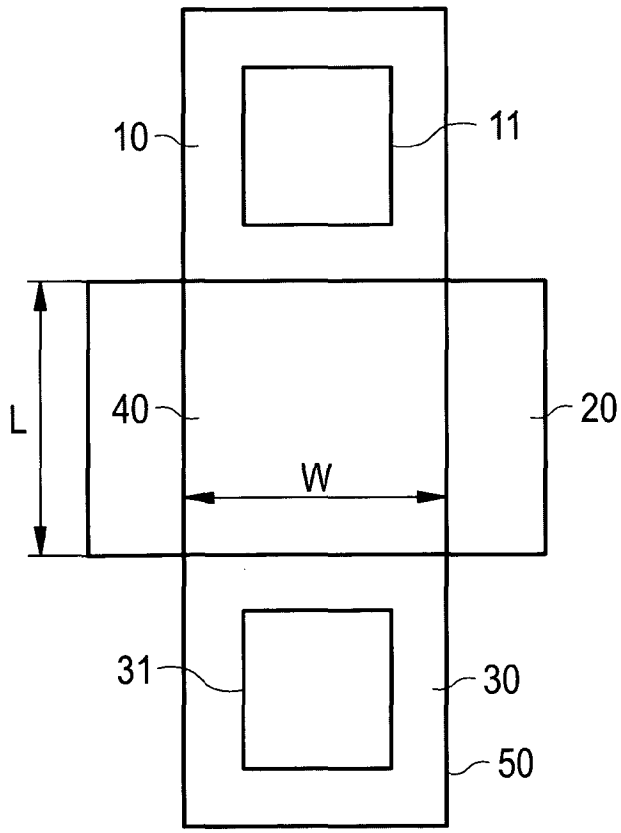
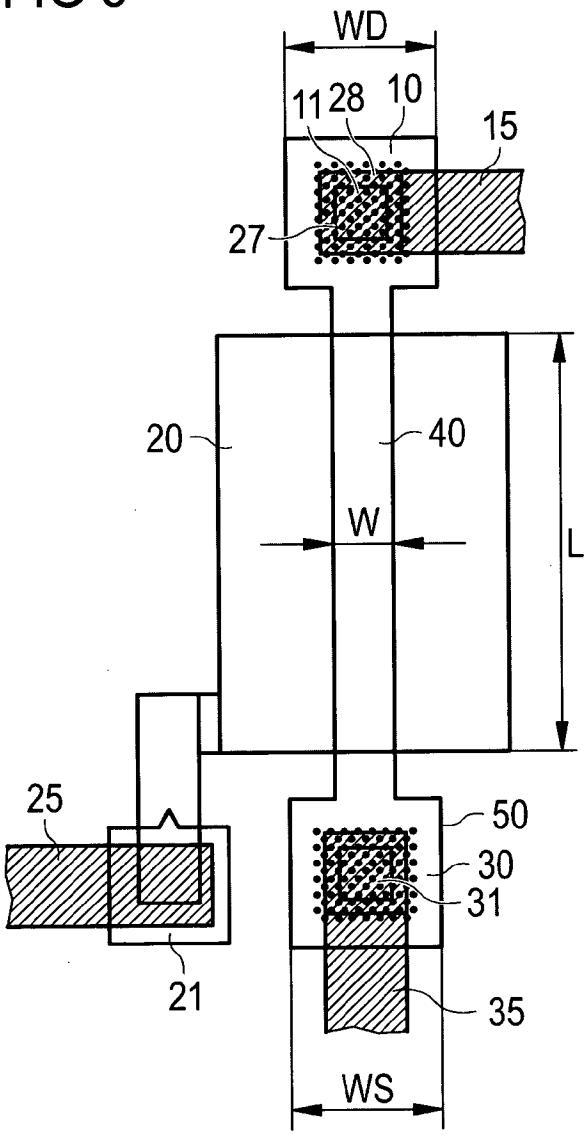


FIG 3



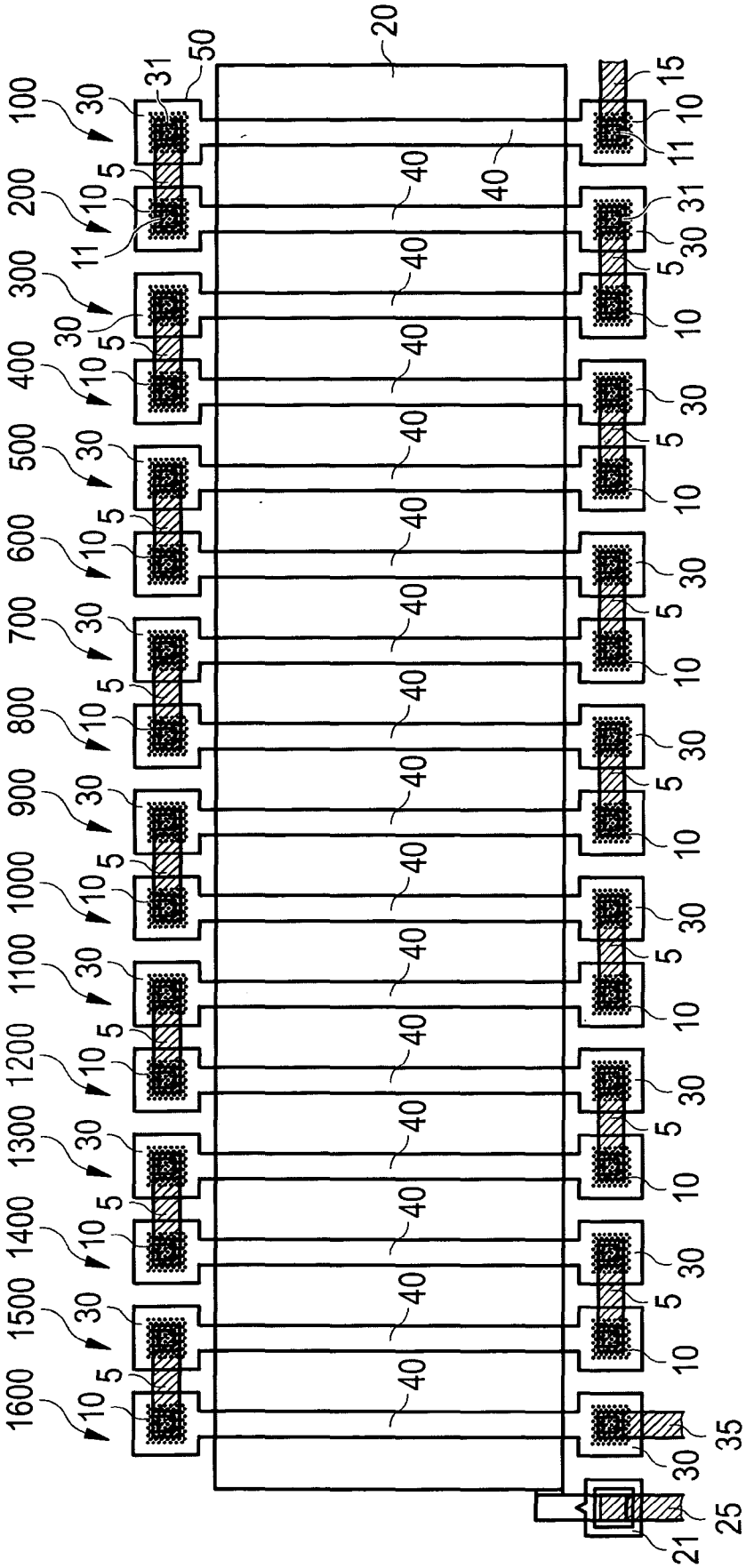

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FIG 4

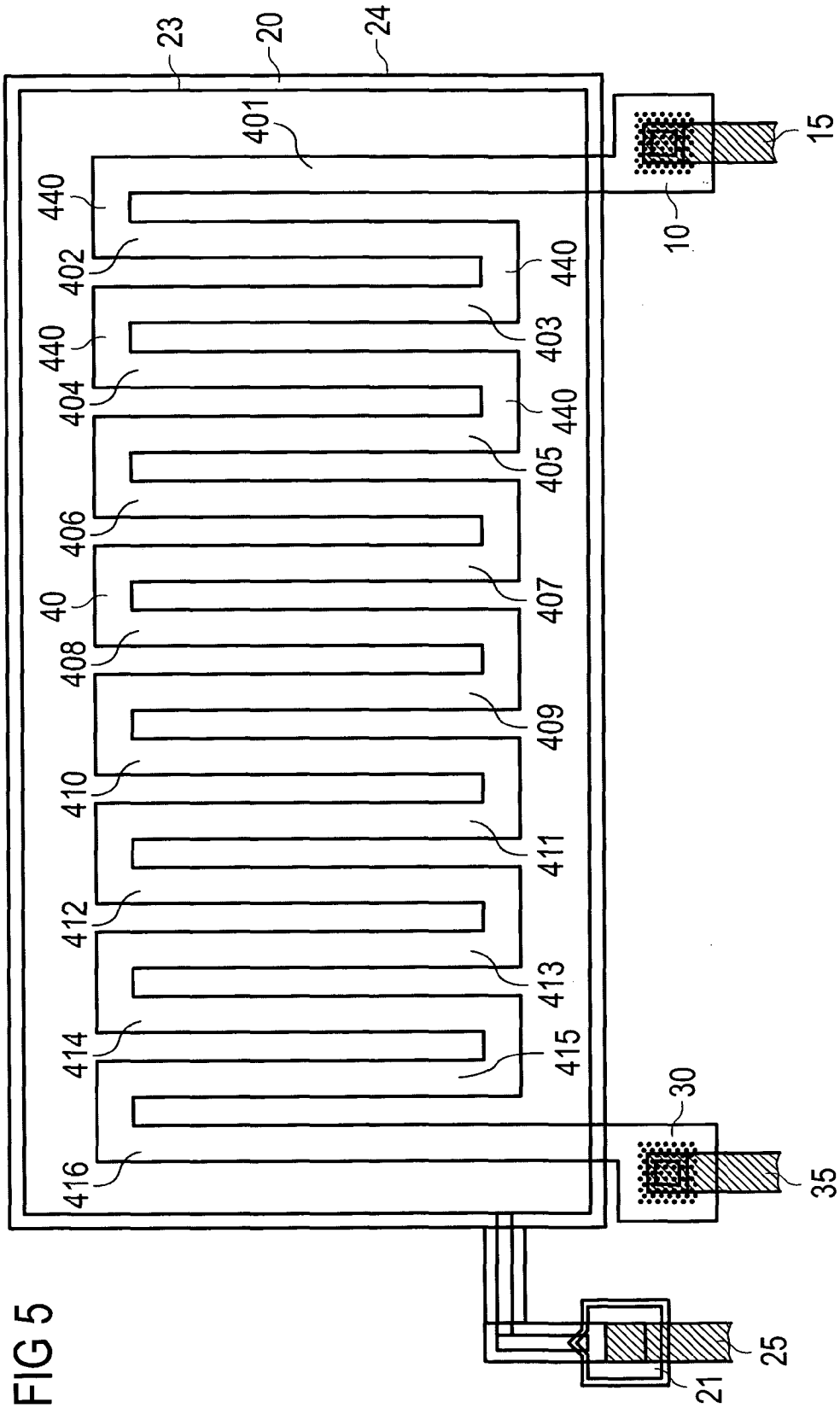
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FIG 5

FIG 6

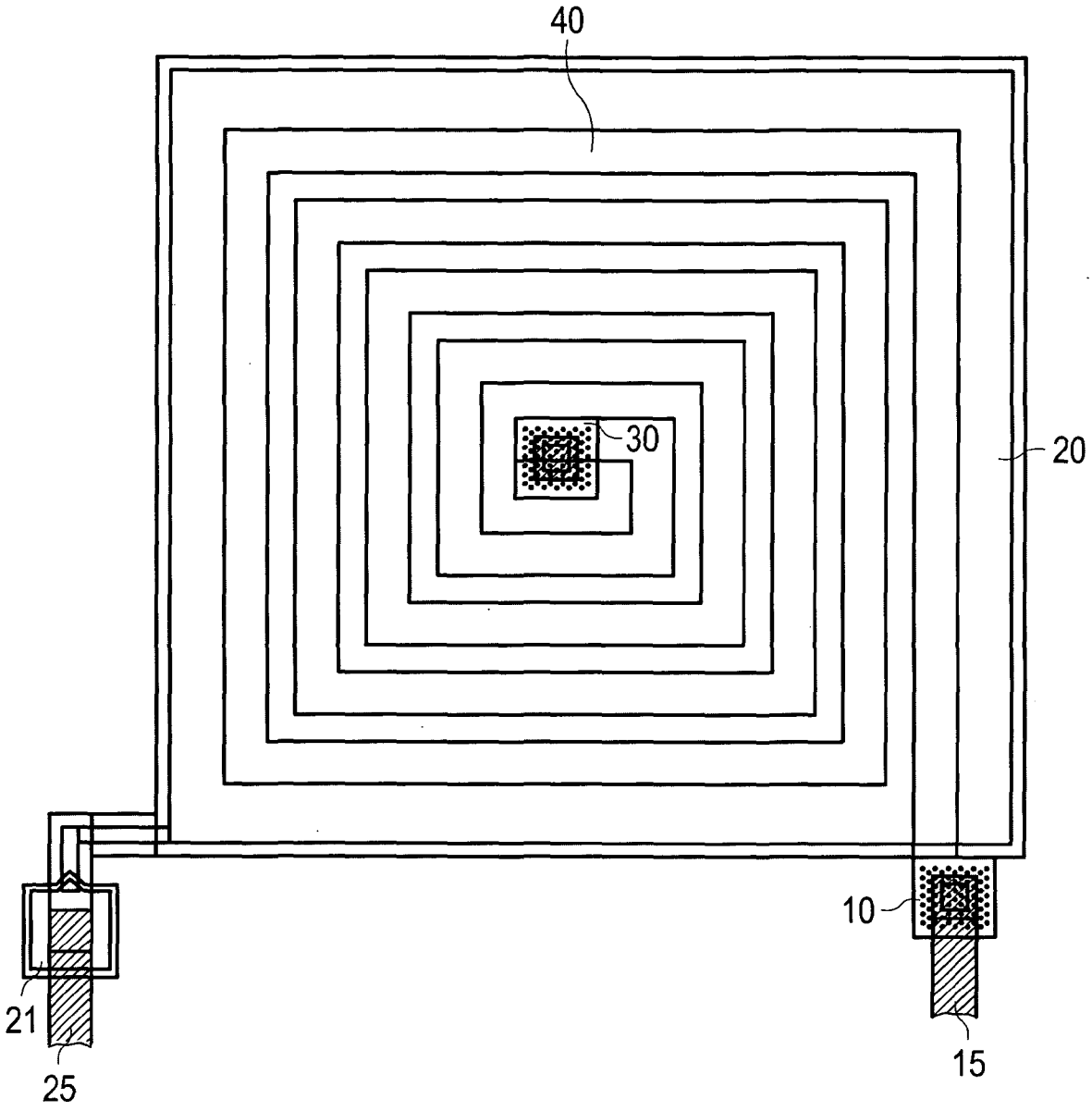


FIG 7

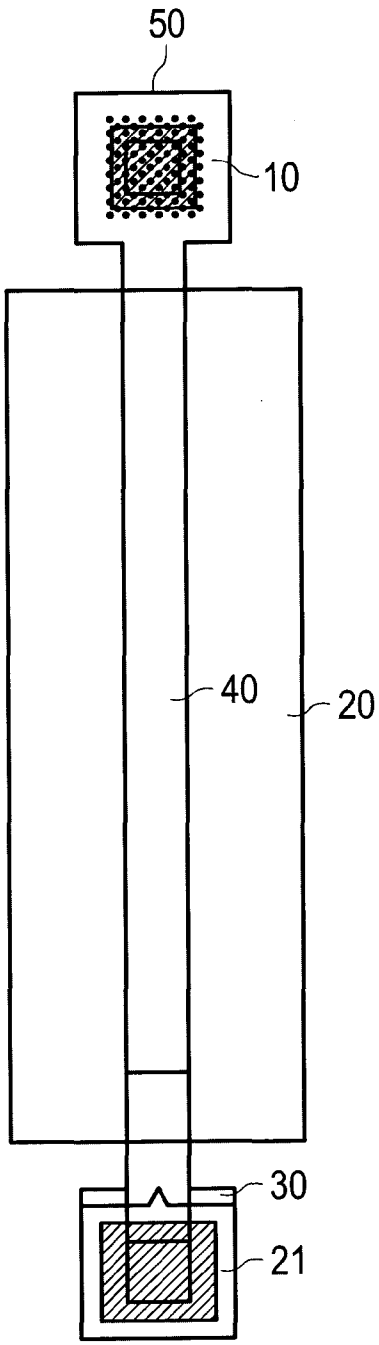


FIG 8A

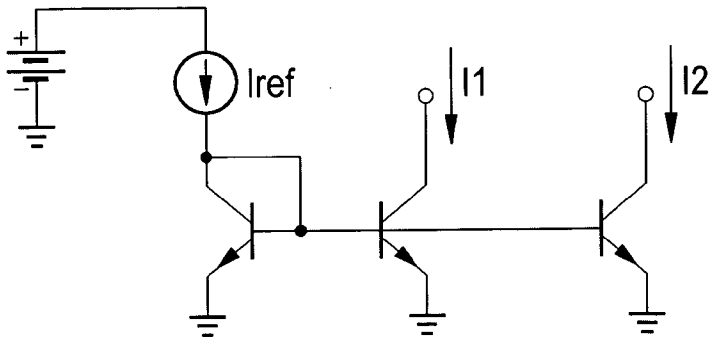


FIG 8B

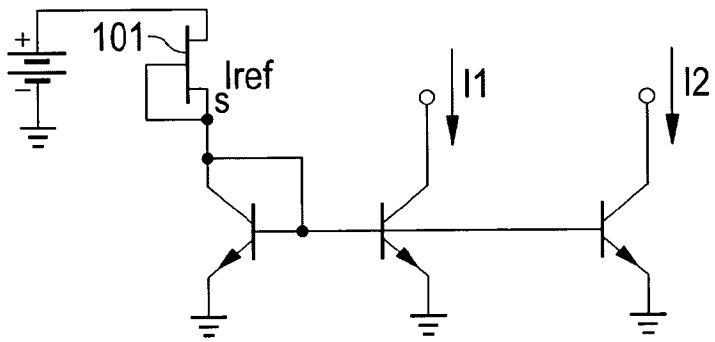


FIG 9A

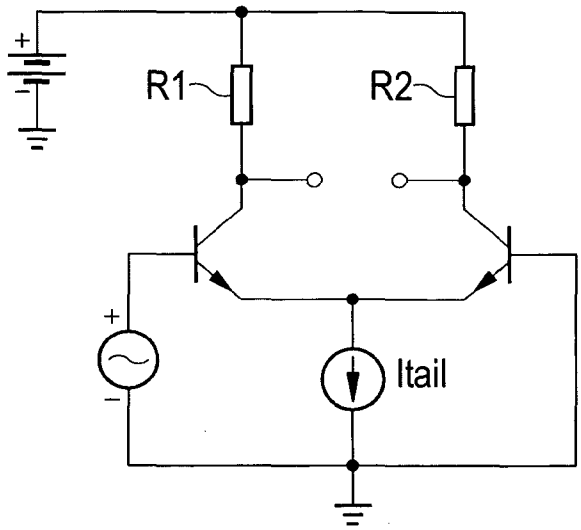


FIG 9B

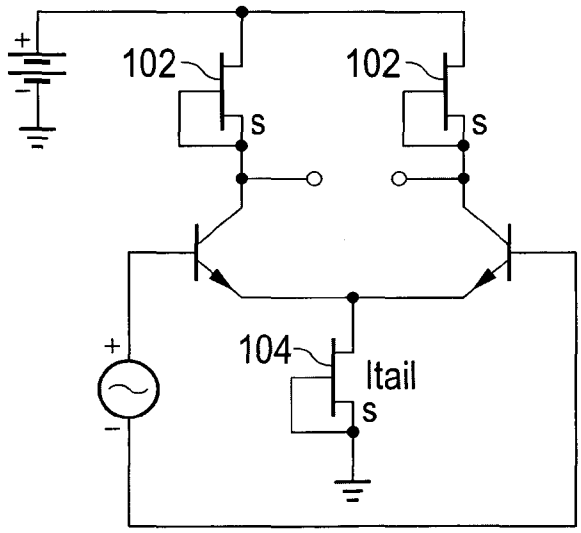


FIG 10A

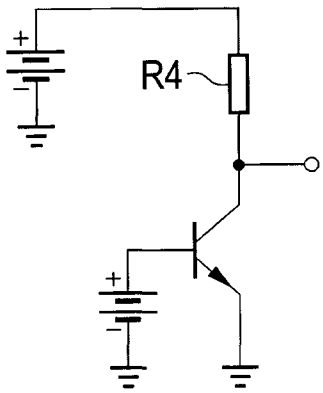
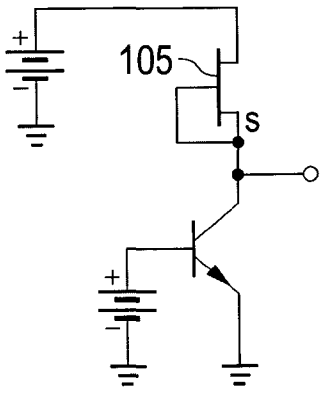


FIG 10B



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/052853

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/335 H01L29/10 H01L29/778
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 498 360 B1 (JAIN FAQUIR C [US] ET AL) 24 December 2002 (2002-12-24) column 1, line 1 - column 5, line 23; figures 2a-2c, 3a-3d	1-6,12, 13 7-11
Y	US 4 404 578 A (TAKAFUJI YUTAKA [JP] ET AL) 13 September 1983 (1983-09-13) Figures 3, 9a-9d, 10 and corresponding text	7-11
A	WO 02/50914 A2 (EUROP ORG FOR NUCLEAR RESEARCH [CH]; SNOEYS WALTER JAN MARIA [FR]) 27 June 2002 (2002-06-27) Figures 6, 16, 17, 20, 21 and corresponding text	7-11
A	EP 0 563 847 A2 (MATSUSHITA ELECTRIC IND CO LTD [JP]) 6 October 1993 (1993-10-06) * abstract; figures 1a, 1b	1-11

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 July 2010	23/07/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dauw, Xavier

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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EP 0563847 A2	06-10-1993	DE 69325673 D1	26-08-1999
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		JP 5275463 A	22-10-1993