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Koshiba

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[45] **July 16, 1974**

[54] **AUTOMATIC APPARATUS FOR SEQUENCING REPAIR WORK IN OPTIMUM ORDER ON MALFUNCTIONS OF GROUPED OPERATING MACHINES**

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[63] Continuation-in-part of Ser. No. 73,694, Sept. 21, 1970, abandoned.

[30] **Foreign Application Priority Data**

Sept. 19, 1969 Japan 44-74840

[52] **U.S. Cl.** **340/172.5**

[51] **Int. Cl.** **G06f 11/00**

[58] **Field of Search** .... 340/172.5, 146.1 R, 146.1 C

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Assistant Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

Apparatus for use in a mill having a plurality of operating machines, wherein the apparatus includes sensing means for detecting machine malfunctions, memory means for determining the order in which repairs should be made to malfunctioning machines, and a repair operator's carriage having means for moving it from one malfunctioning machine to another in the predetermined order and along the shortest route.

7 Claims, 13 Drawing Figures

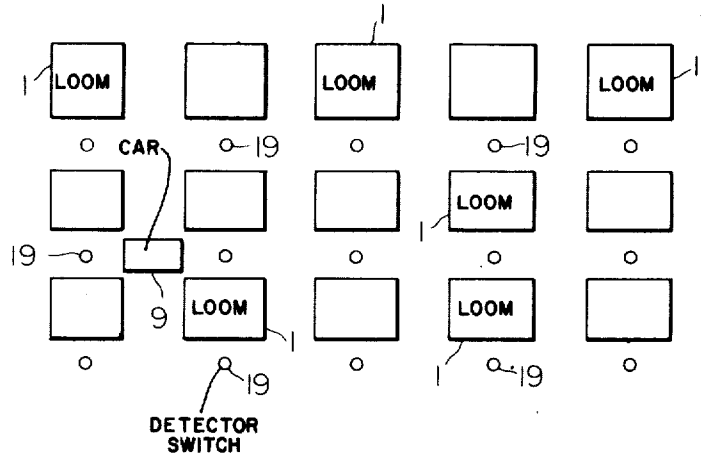


Fig. 1

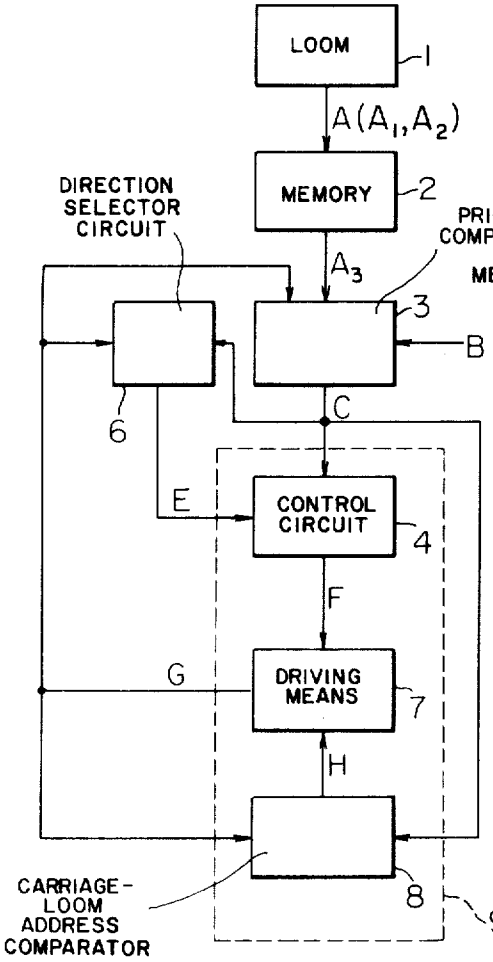

LOOM
1
A(A1,A2)
MEMORY
2
DIRECTION SELECTOR CIRCUIT
PRIORITY COMPARATOR & MEMORY
A3
3
B
6
C
E
CONTROL CIRCUIT
4
F
G
DRIVING MEANS
7
H
8
9
CARRIAGE-LOOM ADDRESS COMPARATOR

Fig. 2

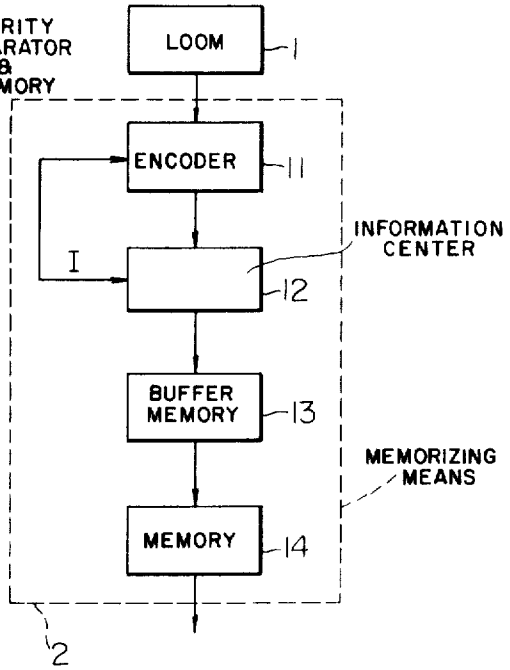

LOOM
1
ENCODER
11
INFORMATION CENTER
I
12
BUFFER MEMORY
13
MEMORIZING MEANS
MEMORY
14
2

Fig. 3

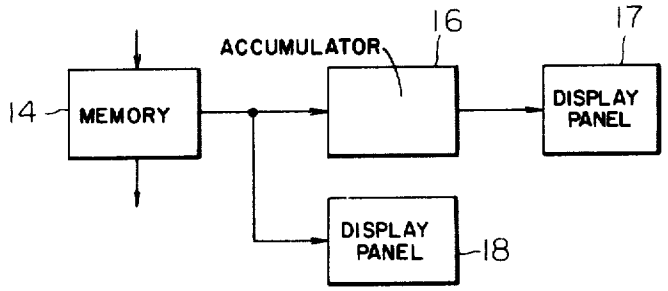

ACCUMULATOR
16
17
14
MEMORY
DISPLAY PANEL
DISPLAY PANEL
18

Fig. 4

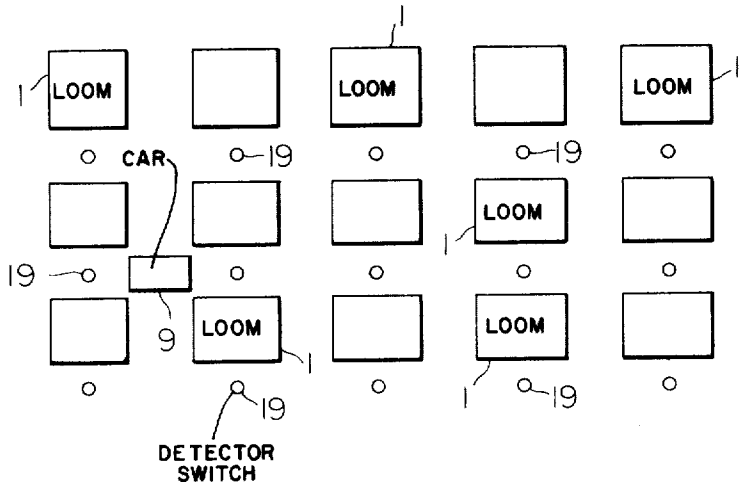

LOOM
CAR
19
9
DETECTOR SWITCH

Fig. 5A

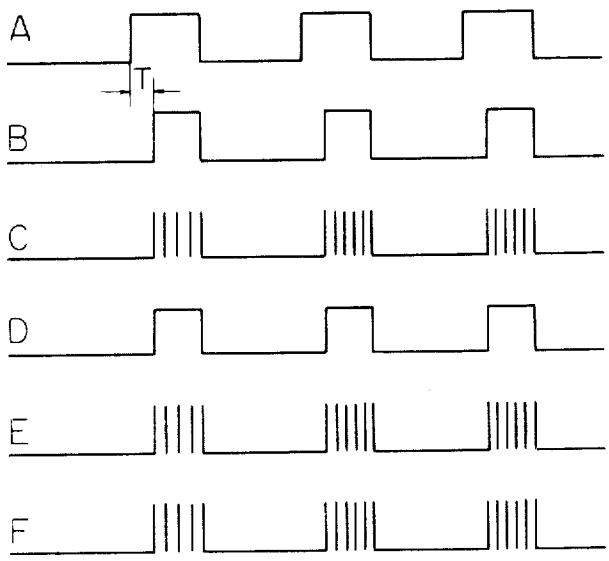


Fig. 5-1

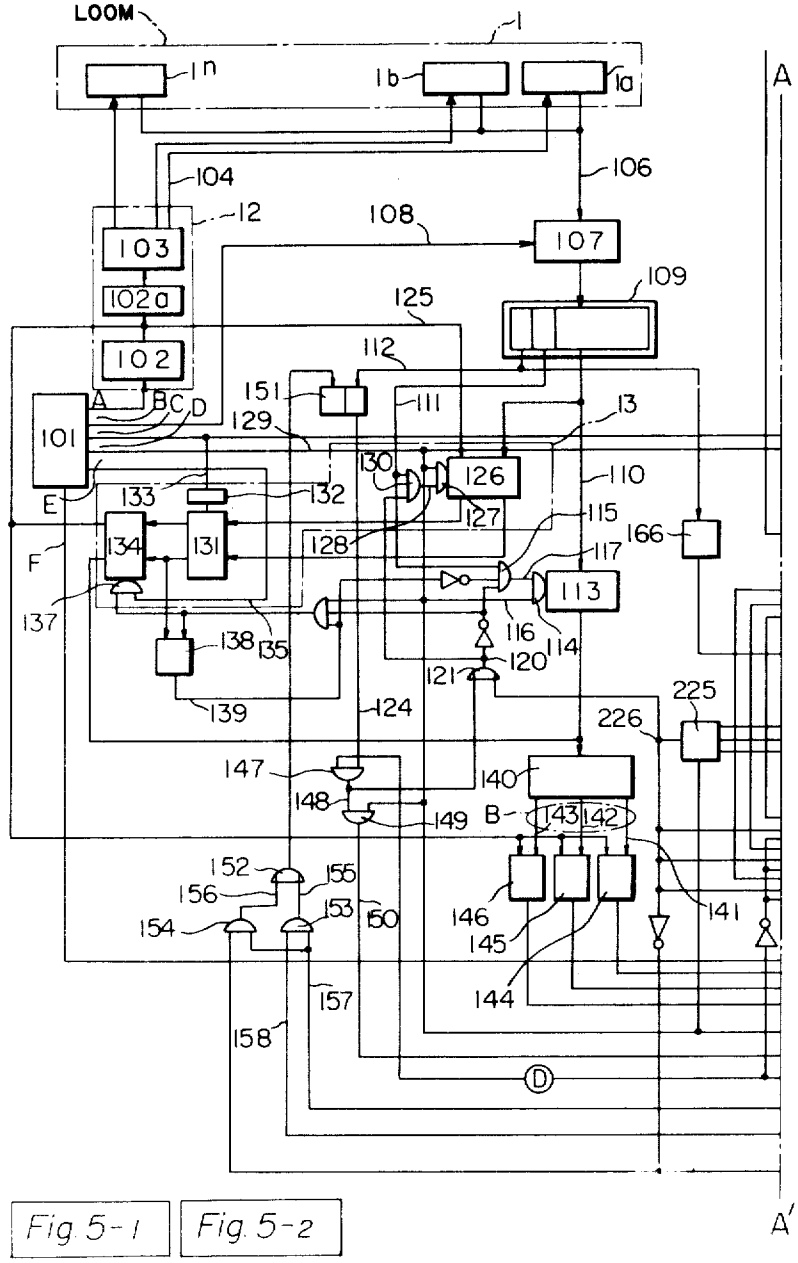


Fig. 5-1 | Fig. 5-2

Fig. 5-2

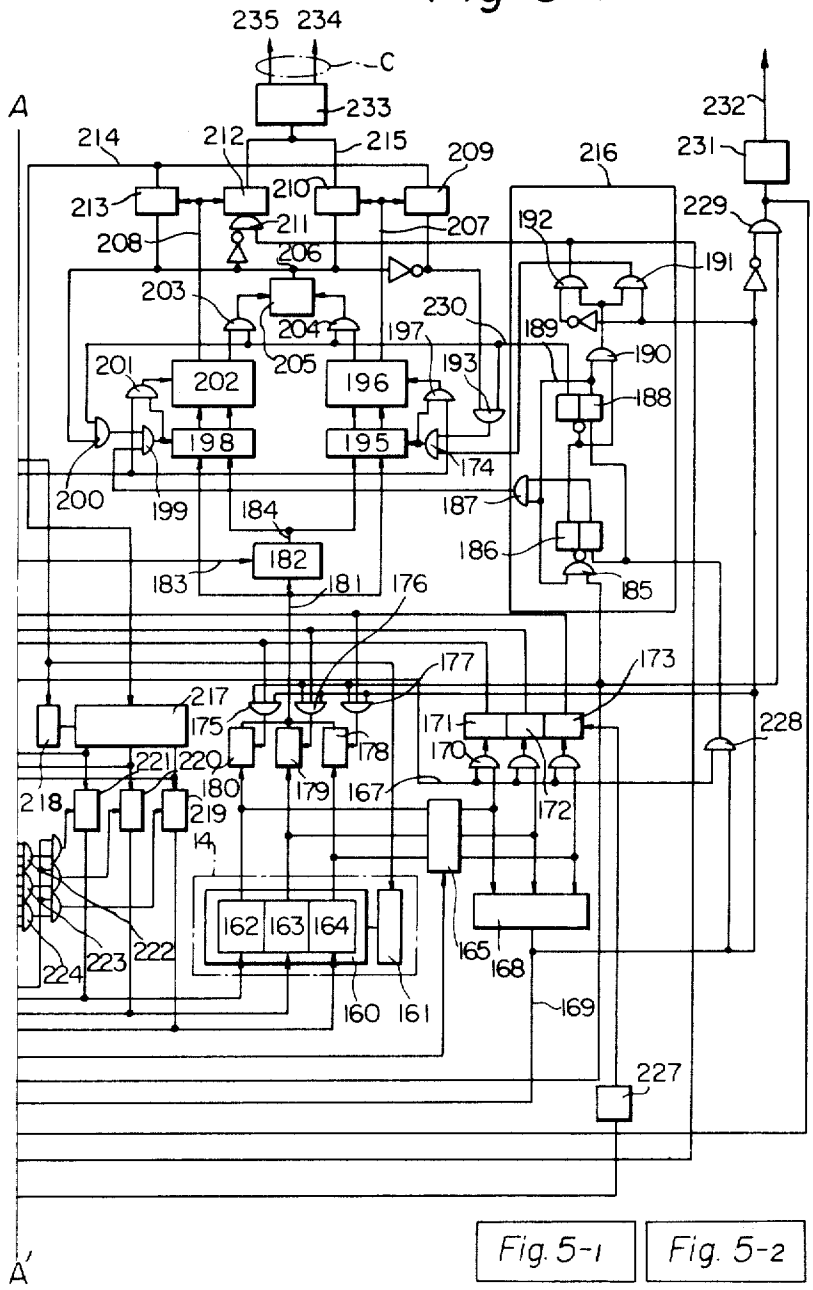


Fig. 5-1 Fig. 5-2

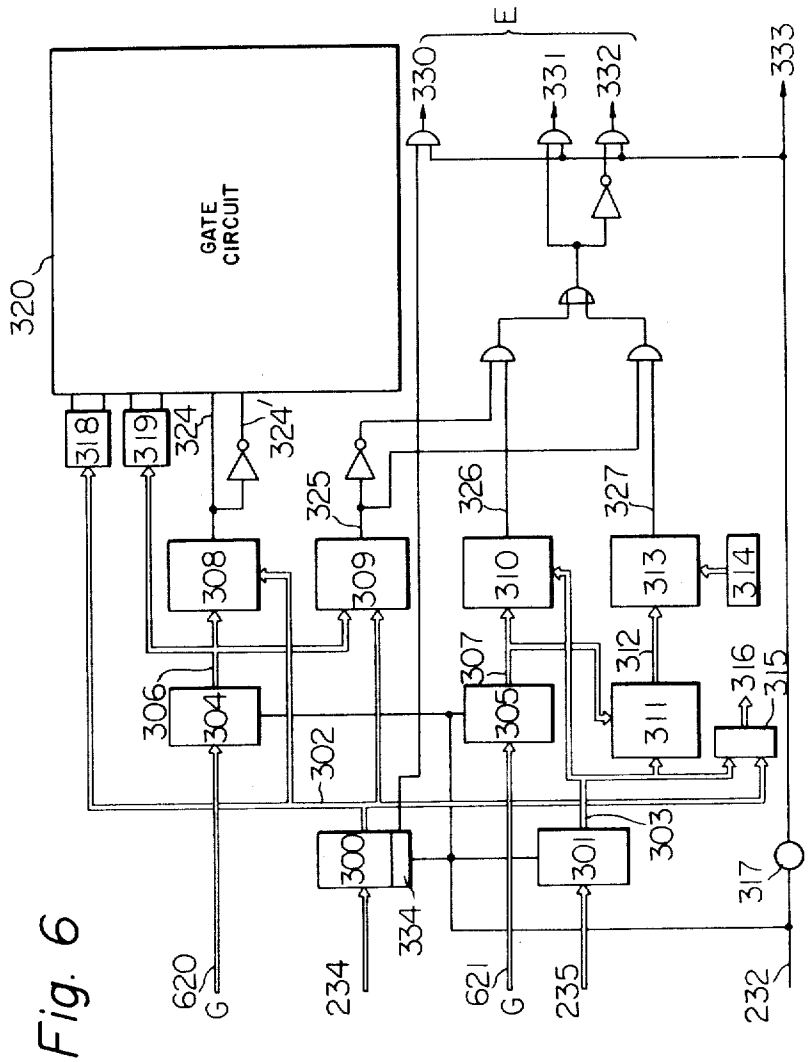

GATE CIRCUIT
320
318
319
324
324
325
326
327
330
331
332
333
E
308
309
310
313
314
306
304
307
305
312
311
316
315
302
303
300
301
317
620
G
234
334
621
G
235
232

Fig. 6

Fig. 7

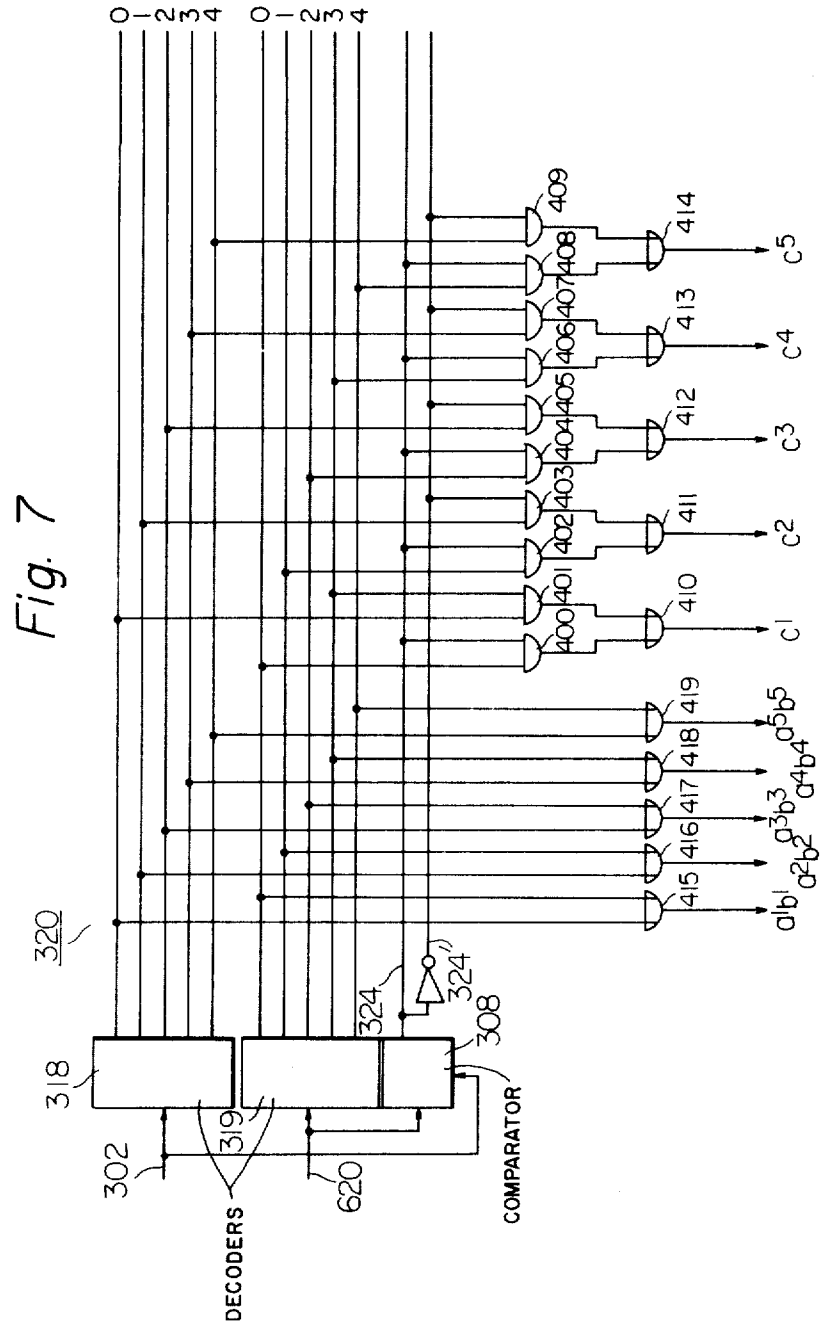

0 1 2 3 4
0 1 2 3 4
320
318
319
302
620
DECODERS
324
324
308
COMPARATOR
409
408
407
406
405
404
403
402
401
400
414
413
412
411
410
c5
c4
c3
c2
c1
419
418
417
416
415
a5b5
a4b4
a3b3
a2b2
a1b1

Fig. 8

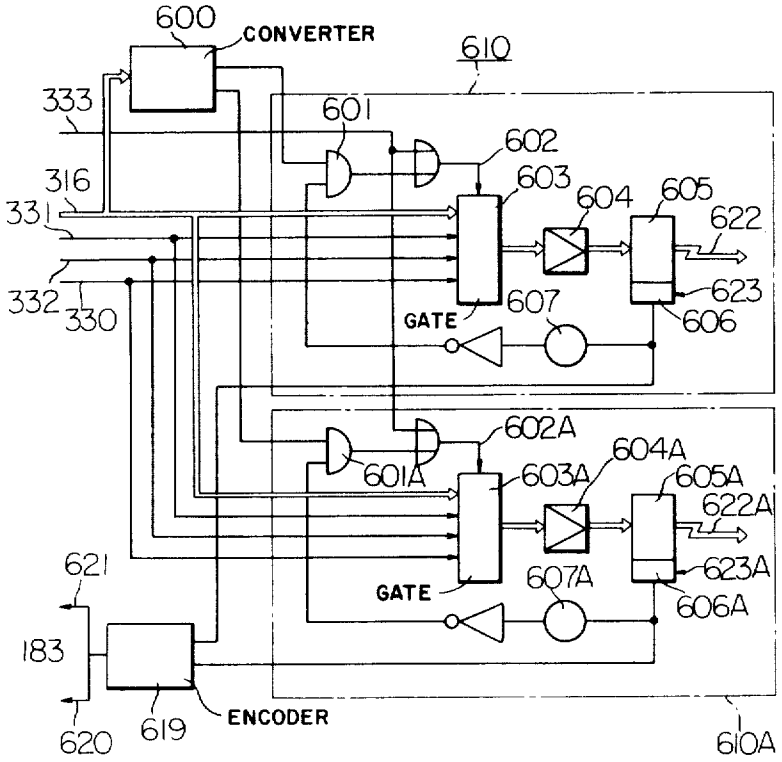

600
CONVERTER
610
333
601
602
316
603
604
605
622
331
623
332
330
GATE
607
606
602A
604A
601A
603A
605A
622A
621
GATE
607A
623A
606A
183
ENCODER
620
619
610A

Fig. 9

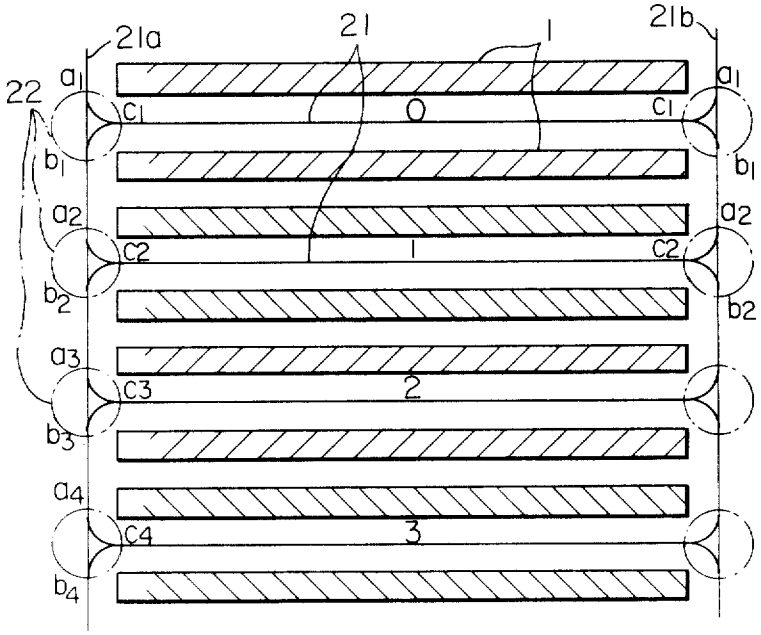

21a
21
1
21b
22
a1
c1
0
b1
a2
c2
1
b2
a3
c3
2
b3
a4
c4
3
b4

Fig. 10

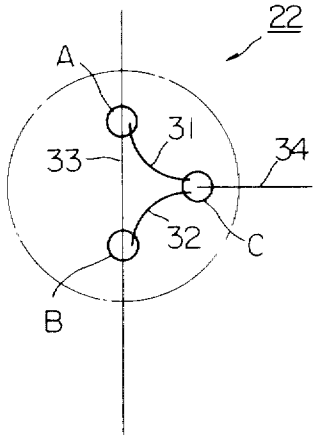
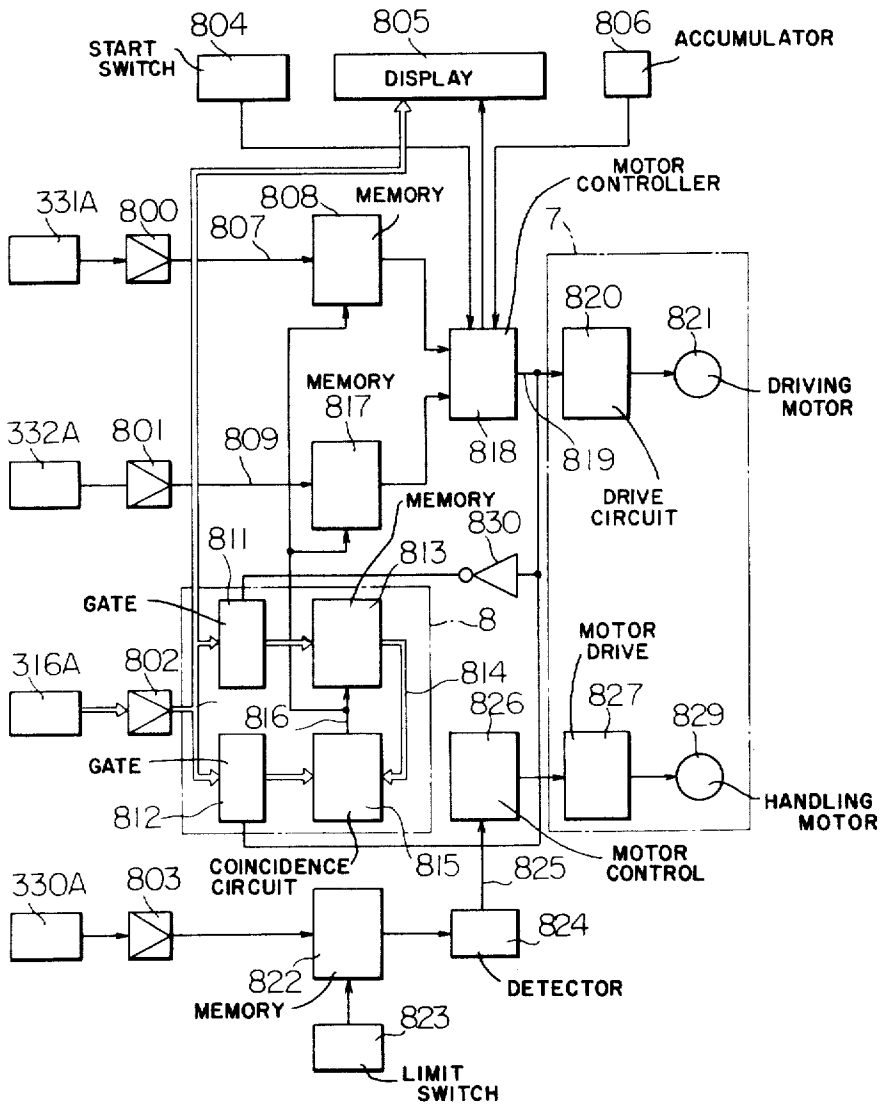

22
A
31
33
34
32
C
B

Fig. 11


804
START SWITCH
805
DISPLAY
806
ACCUMULATOR
MOTOR CONTROLLER
331A
800
808
MEMORY
807
7
820
821
DRIVING MOTOR
MEMORY
817
332A
801
809
818
819
DRIVE CIRCUIT
MEMORY
830
811
813
GATE
8
MOTOR DRIVE
316A
802
814
826
827
829
816
GATE
HANDLING MOTOR
812
815
825
MOTOR CONTROL
330A
803
COINCIDENCE CIRCUIT
824
822
DETECTOR
MEMORY
823
LIMIT SWITCH

AUTOMATIC APPARATUS FOR SEQUENCING REPAIR WORK IN OPTIMUM ORDER ON MALFUNCTIONS OF GROUPED OPERATING MACHINES

RELATED APPLICATION

This application is a continuation-in-part application of our copending application Ser. No. 73,694 filed Sept. 21, 1970, now abandoned.

BACKGROUND OF THE DISCLOSURE

The present invention relates to automatic apparatus for moving a carriage for transporting a repair operator between a plurality of machines. The apparatus senses malfunctions of the machines, determines the priority in which repairs must be made, and advances the carriage to the various malfunctioning machines according to the priority sequence and along the shortest route.

When manufacturing work such as a weaving operation is performed by a plurality of operating machines installed in a mill, cases are encountered wherein two or more machines stop simultaneously due to such causes as consumption of the material, malfunction of some machine parts, completion of an operation cycle requiring the machine to be reset, or accidental breakage of the material during processing. Furthermore, it may be necessary in some instances to perform service procedures even when the machines themselves do not stop. Such servicing and repair of the machines must be performed as quickly as possible so as to maintain the operational efficiency of the machines. Usually, this repair work is performed by operators who watch the operational condition of the machines in the mill, and eliminate any malfunctions which are recognized. Some of the malfunctions can be repaired very easily and within a short time, while other malfunctions require complicated repair and a long down-time for that machine. Therefore, when multiple malfunctions occur simultaneously, and at different machines, it is necessary for the operator to decide the sequence in which the machines must be serviced. In the case of a weaving mill, for example, wherein thread breakage may occur in one of a plurality of weaving looms, it is necessary for the weaver to rush to that loom to mend the thread. When the abovedescribed malfunction takes place at several looms simultaneously, the weaver has to decide which loom he should rush to first. Conventionally, this decision is based on the operator's empirical judgement, and if such decision is erroneous, it results in a serious decrease in the operational efficiency of the machines.

A principal object of the present invention is to provide an apparatus capable of sequentially carrying the repair operator to a plurality of malfunctioning machines in accordance with the optimum priority in which repairs should be made, thereby maintaining the highest operational efficiency of the machines.

SUMMARY OF THE INVENTION

In order to attain the above-described object, in the automatic apparatus of the present invention, information signals corresponding to the causes of the machine malfunctions are compared with predetermined patterns of operational priority signals for the machines, whereupon an address signal of the machine producing the information signal of first priority is produced. This address signal is compared with an address signal of the carriage, and the resultant distance signal is used for selection of the driving direction of the carriage. Both the priority machine address signal and the direction signal are brought into a control circuit of the carriage, which produces a corresponding operational signal for exciting the driving means of the carriage. The instantaneous location relationship between the carriage and the machine of the first priority is continuously detected, and the carriage is stopped when it arrives at the location of the priority machine. Driving control of the carriage can be shifted from automatic to manual and vice versa.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the present invention will be made apparent from the ensuing description, which is directed, for the convenience of the explanation, to the case wherein a plurality of weaving looms are installed in a weaving mill, reference being made to the accompanying drawings, wheerein:

FIG. **1** is a block diagram of a principal arrangement of the automatic apparatus of the present invention,

FIG. **2** is a block diagram of a detailed arrangement of the memory means shown in FIG. **1**,

FIG. **3** is a block diagram of the memory circuit shown in FIG. **2**, together with its related display parts,

FIG. **4** is a schematic plan view of a mill equipped with a plurality of machines and corresponding carriage detector switches,

FIG. **5** comprising FIGS. **5–1** and **5–2** is a detailed logic circuit of memorizing means **2** and comparing means **3** of FIG. **1**,

FIG. **5A** is the waveform of the output signal of control unit **101** of FIG. **5**,

FIG. **6** is a detailed block diagram of direction selector circuit **6** of FIG. **1**,

FIG. **7** is a logic circuit of gate circuit **320** of FIG. **6**,

FIG. **8** is a block diagram of the auxiliary circuits which apply the control signal to a carriage,

FIG. **9** shows a plurality of machines and corresponding paths of a carriage together with a plurality of cross points,

FIG. **10** shows the logical structure of a cross point, and

FIG. **11** is a detailed block diagram of the logic circuit of a carriage **9** of FIG. **1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In a preferred embodiment of the invention, as illustrated in FIG. **1**, the automatic apparatus includes a plurality of looms **1**, which have means for sensing failures and for generating malfunction signals A, composed of cause-information signals A_1, and machine address signals A_2. The signals A are centralized and brought into memory means **2** connected to respective looms **1**. The cause-information signals A_1 are given characteristic patterns in accordance with the kinds and types of the causes of the loom malfunction, while the locations of the looms **1** producing the cause-information signals A_1 are represented by the predetermined machine address signals A_2.

The combined output signal A_3 from the memory means **2**, defining the priority values and positions of

the malfunctioning machines is coupled to a priority comparator and memory means **3**, which is provided with a circuit for scanning the priority sequence of the information signals A_3 in reference to a reference operation pattern signal B previously stored in the comparator and memory means **3**. By the operation of this priority scanning circuit, the information signals are sequentially registered in a register of the comparator and memory means **3** in the order of their priority.

In some cases, two or more loom malfunctions have equal priority. In order to select the loom malfunction of the first priority, the address signals of the looms producing the registered information signals are compared with a carriage address signal G. In the case where the malfunctions of two looms are ranked equally, in view of the reference operation pattern signal B, the loom located closest to the position of the operator's carriage is selected as the loom of the first priority, and a corresponding priority loom (machine) address signal C is produced so as to be transmitted to a control circuit **4** on the operator's carriage **9**. This priority loom address signal C is compared with the carriage address signal G within the comparator and memory means **3**. Both the address signal C and the carriage address signal G are brought into a direction selector circuit **6** and a resultant direction signal E is coupled to the control circuit **4** of the carriage **9**. Upon receipt of the priority loom address signal C from the comparing means **3** and the direction signal E from the direction selector circuit **6**, the control circuit **4** produces an operational command signal F which is coupled to the driving means **7** for the carriage. The driving means **7** is provided with a device for producing the carriage address signal G showing the location of the operator's carriage **9** with respect to a 0 reference point fixed in the mill. This carriage address signal G is transmitted to a carriage-loom address comparator **8** also receiving the priority loom address signal C from the comparator and memory means **3**. When the carriage **9** arrives at the location of the loom of the first priority, the carriage loom address comparator **8** produces a stop signal H, and the driving operation of the driving means **7** is thereby terminated. Upon arrival at the loom, the operator performs the repair work necessary to eliminate the malfunction of that loom, and, after completion of this repair work, the loom is restarted and a signal reporting this completion of the repair work resets the automatic apparatus of the present invention.

Control of the driving means **7** can be shifted from automatic to manual by operating a switch mounted on the carriage **9**, so that it is also possible for the operator to manually control the driving means **7** of the carriage to direct it on the basis of his empirical judgement.

In a practical embodiment, signals C and E are transmitted to a carriage **9** through an auxiliary circuit (not shown in FIG. **1**). The structure of said auxiliary circuit will be explained later in connection with FIG. **8**.

A detailed arrangement of the memory means **2** is shown in FIG. **2**, wherein there are provided encoders **11** related to the respective looms **1**, an information center **12** connected to the respective loom encoders **11**, and a buffer memory **13** coupled between the information center **12** and a memory **14**.

When the malfunction takes place on a certain loom **1**, this malfunction is first sensed by a corresponding mechanical signal. For example, breakage of a warp may be detected by a downward movement of a corresponding dropper. Next, this mechanical signal is transduced into a corresponding electric signal and further encoded into a corresponding malfunction cause-information signal by the encoder **11** associated with that loom **1**. Malfunction cause-information signals, obtained in this manner, are subjected to a scanning operation by a scanning pulse signal I emitted by the information center **12**, and the picked up information signals are transmitted to the information center **12**. Simultaneously, the address signals of the malfunctioning looms are also transmitted to the information center **12**. In this case, the address signals are informative of the location of the loom of malfunction with respect to the **0** reference point suitably selected in the mill. The address of the looms may be given in the form of matrix representations or in the form of X - Y coordinates. From this information center **12**, the information signals are transmitted to the buffer memory **13** which is provided with a distribution circuit. By the operation of the distribution circuit, these information signals are compared with data signals previously provided in the buffer memory **13** and are registered into the memory **14** according to the kinds and types of the causes of the loom malfunctions.

In the arrangement shown in FIG. **2**, the memory **14** may be connected to additional elements as shown in FIG. **3**. An accumulator **16** for accumulating the non-running time of the looms and a display panel **18** for the causes of the loom malfunctions are connected in parallel to the memory **14**, in an arrangement receptive of the output signal of the memory **14**. A display panel **17** for the non-running time for the respective malfunctions is connected to the accumulator **16**.

In the case of the above described embodiment, the driving means **7** is provided with a device for producing the carriage address signal G showing the location of the operator's carriage **9** with respect to the 0 point fixed in the mill. However, this device can be replaced by spaced detector switches **19** planted in the floor of the mill along the advancing paths of the operator's carriage **9**, as shown in FIG. **4**. When the operator's carriage **9** passes the position of a certain detector switch **19**, that detector switch **19** produces a signal corresponding to the carriage address signal G and this signal is transmitted to the comparator and memory means **3**. The pattern of the signal is formed according to the relationship of the location of that detector switch **19** with respect to the 0 point fixed in the mill. Further, the advancing direction of the operator's carriage **9**, during its travel, is also sensed by these detector switches **19**. The detector switches **19** may be interspersed so as to show the location of the carriage **9** either in a matrix representation or in the form X - Y coordinates.

The operation of memorizing means **2** and comparing means **3** in FIG. **1** will now be explained in full in connection with the logical circuit of FIG. **5**. In FIG. **5**, machines **1***a*, **1***b*, . . . **1***n* correspond to a loom **1** of FIG. **1**. A circuit having address counter **102**, binary-decimal converter **102***a* and driver **103** corresponds to information center **12** of FIG. **1**. A circuit having gate **126**, register **131**, gate **134** and their relating circuits corresponds to buffer memory **13** of FIG. **1**. A circuit having register circuit **160** and step up circuit **161** corresponds to memory **14** of FIG. **1**. And the rest of FIG. **5** corresponds to comparing means **3** of FIG. **1**. Further priority signals **141**, **142** and **143** correspond to signal

B of FIG. 1, and output signals **234** and **235** correspond to address signal C of FIG. 1. As the structure of the logical circuit of FIG. 5 is easily understood by anyone skilled in the art from above explanation and reference number table at the end of this specification, no explanation about the structure of the logical circuit of FIG. 5 is necessary, and the operation of FIG. 5 is next explained.

1. A pulse signal from control unit **101** steps up the content of address counter **102**, which scans the machine address and gives an address of the machine which should forward the data. Each output terminal A, B, C, D and E of control unit **101** gives the corresponding signal shown in FIG. 5A.

2. The machine address given by address counter **102** is converted from binary number to decimal number by binary-decimal converter **102***a*, and the driving signal appears at one of the address lines **104** which provide the output signal of driver **103.**

3. Data **106** from machine 1 (**1***a*, **1***b*, . . . , **1***n*) is received by receiver **107**, and said data **106** is stored in register **109** by read-signal **108** from control unit **101** to register **109.** Data **106** has condition flag **111**, end-flag **112**, working information, and priority information.

4. When condition flag **111** stored in register **109** is on, it means the corresponding machine is requesting the work, and data **106** is processed only when said flag is on.

5. When condition flag **111** is on, and end flag **112** is off, AND gate **114** and **115** connected to gate **113** open together with gate **113**, then data **110** is sorted by priority circuit **140** according to the priority of data **110.** Said priority circuit **140** provides one of priority signals **141**, **142** or **143**, which open one of the corresponding gates **144**, **145** and **146.** Accordingly, the machine number of the problem is stored in register **160.** The actual data **110** sent from the machine **1** is not stored in register **160**, but is indicated at the panel of the machine.

6. Said register **160** is controlled by step-up circuit **161** so as to store the data from the most significant digit.

7. Suppose that end flag **112** of data stored in register **109** is 1, flip-flop **151** is set to 1 and one-shot-multivibrator **166** is triggered, and the highest priority stored in one of registers **162**, **163** and **164** is detected by priority detector **165.** One of flip-flops **171**, **172** and **173** is set to 1 according to the coincidence of the output of one-shot multivibrator **166** with one of the outputs of priority circuit **160.**

8. If there is no data in register **160**, that is to say, if work is not requested, zero-detection circuit **168** detects this state and outputs zero to output line **169**, which closes gate **147.** Therefore the operation of the circuit in FIGS. **5-1** and **5-2** finishes, and said circuit waits data **110** by keeping open gate **113.**

9. If there is some data stored in one of registers **162**, **163** and **164** of register **160**, gate **147** opens and the output **120** of OR gate **121** becomes 1, and said output **120** closes gate **113** through the invertor. Therefore input data cannot be received and gate **149** opens. The clock pulse **129** from output terminal D goes through said gates **147** and **149**, and opens gate **185**, and the operation of priority decision begins.

10. At the same time output signal **148** of AND gate **147** opens AND gate **130** through OR gate **121** and output signal **120**, and data from machine **1** is stored in register **131**, which stores both the content of data **110** and the address of the machine.

11. Initial operation control **216** has two flip-flops **186** and **188**, and some gates. Said flip-flops **186** and **188** are reset to zero by the output of AND gate **228**, The output of AND gate **228** is provided if there are both pulse signals **228.** from one-shot multivibrator **166** just after appearing end-flag **112**, and output signal **169** of zero detection circuit **168.** Said circuit **168** tests if there is any data stored in register **160.**

12. In the condition that initial operation control **216** is set to initial condition, when the second clock pulse appears from the output **150** of gate **149**, output **189** of flip-flop **188** becomes 0 and gate **185** is closed. Accordingly the operation of control **216** stops automatically.

13. The first clock pulse inverts flip-flop **186**, and the output **169** of zero detection circuit **168** opens gate **191** and closes gate **192.** Gate **200** is closed as output **230** of flip-flop **188** is zero. Accordingly output of gate **199** becomes zero and gate **198** closes. At the same time register **160** is stepped up.

14. When there is only one data in one of three registers **162**, **163** and **164** chosen according to priority, the second clock pulse provides zero at output line **169** of zero detection circuit **168**, and closes AND gate **191.** Gate **195** closes too as the outputs of gate **178**, **179** and **180** are zero. At the same time, gate **192** opens, which opens gate **212** and sends data relative to the location of the machine from buffer register **202** to output line **215.**

15. Output signal of zero detection circuit **168**, which is now zero, is applied to gate **229** through the invertor, and clock pulse **150** is also applied to said gate **229** through gate **149.** The output signal **157** of said gate **229**, and output signal **158** of gate **192** reset flip-flop **151** to zero through gates **153**, **154** and **152.** At the same time one-shot multivibrator **231** is triggered, which provides priority signal **232.**

16. When there are more than two data chosen according to priority in one of three registers **162**, **163** and **164**, output line **169** of zero detection circuit **168** provides 1. Therefore gate **191** opens, which opens gate **195**, and the machine location data **181** of the second machine, which is the output signal of gates **178**, **179** and **180**, and distance data **184** to a carriage are stored in a buffer register **196.** At this time flip-flop **188** inverts, which closes gate **185.** And as output line **230** provides signal 1, gates **203** and **204** open. Accordingly distance data stored in buffer registers **196** and **202** are applied to comparison circuit **205.**

17. Comparison circuit **205** provides the output signal and opens gate **213** when distance data stored in register **202** is larger than that stored in register **196.** Accordingly machine location **208** stored in buffer register **202**, which has low priority, is sent to a buffer register **217** through output line **214.** Said register **217** also stores said data from the most significant digit by means of step-up circuit **218.**

18. As gate **210** opens at the same time, machine location data **207** stored in the buffer register **196** appears at output line **215.** Further as gate **200** and **198** open, the next data stored in a register having the second priority goes to the buffer register **202** with the next clock pulse.

19. On the other hand, when distance data stored in the register **196** is equal to or larger than that stored in the register **202**, the output of comparison circuit **205** is zero and gate **209** opens. Accordingly machine location data **207** stored in the buffer register **196** goes to the buffer register **202** through output line **214.** Further, as gate **212** opens, machine location data **208** stored in the buffer register **202** appears at output line **215**, and, opening gate **193** and **195**, the next data is stored in the buffer register **196.**

20. The above operation, of comparing two distances, is repeated until output **169** of zero detection circuit **168** becomes zero. The machine location data with a larger distance which has a lower priority is stored in a buffer register **217.**

21. As explained above, when the content of a register with the highest priority becomes zero, X coordinate **234**, Y coordinate **235** and priority signal **232** relating to the machine with the highest priority are provided by output signal **169** of zero detection circuit **168.**

22. When the output of zero detection circuit **168** becomes zero, one of gates **222, 223** and **234** opens and the data stored in the register **217** returns to the original register.

23. Said operation finishes when the output signal **226** of zero detection circuit **225** becomes zero. Said output signal **226** opens gate **134** of the buffer register **131** through OR gate **121**, and AND gates **136** and **137.** A clock pulse from output terminal E of control unit **101** is applied to gates **134** through **137.** Said clock pulse is divided into short period pulses, the number of which are proportional to the maximum memory capacity of a register **131.** The data **125** showing machine location and data **110** showing working information stored in a register **131** go to priority circuit **140.** The address of a machine corresponding to data **125** is stored in register **160** from priority circuit **140** through one of gates **144, 145** and **146.** Control unit **101** is designed so as to apply the next clock pulse **129** (D in FIG. 5A) just after all data stored in the buffer register **131** has been stored in the register **160.**

24. Signal **226** opens gate **154** and resets flip-flop **151** through the invertor just after the transportation of data between buffer registers finishes. At this time as output **120** of OR gate **121** becomes zero, gate **113** opens again and input data from machine **1** can be received.

FIG. **6** shows a detailed block diagram of direction selector circuit **6** of FIG. **1**, and FIG. **7** shows detailed logical circuit of gate circuit **320** of FIG. **6.** Carriage address signal G of FIG. **1** is applied to gate **304** and **305** in FIG. **6** as X coordinate **620** and Y coordinate **621.** Output signal **330, 331** and **332** correspond to direction signal E of FIG. **1.** The output signal of gate circuit **320** is applied to points in FIG. **9** so as to control said points and lead the carriage **9** to the front of the machine which delivered a request. In FIG. **7**, output **0 – 4** of decoder circuits **318** and **319** are shown, but the outputs of more than 5 of decoder circuits **318** and **319** are not shown for the sake of brevity.

The operation of FIG. **6** and FIG. **7** is described hereinafter.

1. As machine **1** is arranged to locate both sides of a path as shown in FIG. **9**, a carriage **9** turns right or left according to the location of a machine. If the machine stands on the right side of the path, the carriage turns to the right and vice versa. Priority signal **232** sets X coordinate **234** and Y coordinate **235** of the machine location to registers **300** and **301**, respectively. Output signal **330** which handles the carriage toward the machine with the problem is provided according to the sense (0 or 1) of the least significant digit **334** of the X coordinate of machine location signal **234.**

2. The path number that the carriage must go through in FIG. **9** is calculated from X coordinate **234** of machine **1.** The least significant digit of X coordinate **234** of machine location stored in the register **300** is cleared as it has been used for handling of a carriage. The path number **302** that the carriage must go through is obtained by shifting said X coordinate right for one digit. Said path number **302** is applied to comparison circuit **308** and compared with X coordinate **620** of the carriage at this time, which is also applied to comparison circuit **308** through gate **304.** Output **324** of comparison circuit **308** determines whether path number **302** is larger than X coordinate **620** of the carriage or not. Points A, B and C in FIG. **9** and FIG. **10** are controlled by said output signal **324**, the output of decode circuit **318** which decodes path number **302**, and the output of decode circuit **319** which decodes the X coordinate of a carriage at this time.

3. Comparison circuit **308** provides output signal one when path number **302** is larger than X coordinate **620** of the carriage.

4. As explained hereinafter points A and B are controlled by one of signals a_1b_1, a_2b_2, . . . which are the output signals of gates **415 – 419** in FIG. **7.** Point C is controlled by one of signals c_1, c_2, . . . which are the output signals of gates **410 – 414.** For instance, suppose comparison circuit **308** provides an output signal, decode circuit **318** provides an output signal at output terminal 0, and decode circuit **319** provides an output signal at output terminal 0. In such a case signals a_1b_1 and c_1 appear as in FIG. **7**, and thus corresponding points a_1, b_1 and c_1 are controlled.

5. The direction of movement of the carriage is controlled as follows. A carriage stands on the desired path when path number **302**, where the machine is located, coincides with X coordinate **306** of a carriage. In this case comparison circuit **309** provides zero output. The other comparison circuit **310** compares Y coordinate **621** of a carriage through gate **305** with Y coordinate **303** of the machine. When Y coordinate **621** of the carriage is larger than Y coordinate **303** of the machine, said comparison circuit **310** provides output signal **326** and normal signal **331.** On the other hand when Y coordinate **621** of the carriage is equal to or smaller than Y coordinate **303** of the machine, said comparison circuit **310** provides zero output, and reverse signal **332** is provided. The normal signal **331** or the reverse signal **332** drives the carriage to the normal direction or the reverse direction in the particular path.

6. The comparison circuit **309** provides output signal 1 when X coordinate **306** of the carriage is not the same as path number **302.** In this case Y coordinate **303** of the machine and Y coordinate **307** of the carriage are applied to an adder **311**, which provides the sum **312** of them. The comparison circuit **313** compares said sum **312** with N provided from constant number generator **314**, where N is equal to the number of machines lined in one path. If N is larger than the sum **312**, the comparison circuit **313** provides output **327** and normal signal **331** through some gates. On the

other hand if N is equal to or smaller than the sum **312**, said comparison circuit **313** provides zero output and reverse signal **332**.

FIG. **8** shows a detailed block diagram of an auxiliary circuit which sends a signal to the carriage and receives a signal from the carriage. In FIG. **8**, priority end signal **333** from FIG. **6**, coordinates **316** signal of the goal machine, normal signal **331**, reverse signal **332**, and handling signal **330** are applied to a unit circuit **610**, **610A**, ... The unit circuit **610** provides output signal **622**, which includes information of each input signal **333**, **316**, **331**, **332** and **330**. Output signal **622** is applied to the carriage **9** through detector switch **19** by wireless. Further, the carriage **9** provides signal **623** through detector switch **19** to unit circuit **610** by wireless. The X coordinate and Y coordinate of the carriage **9** at any moment are obtained from said signal **623** through encoder **619**. The number of unit circuits **610** installed corresponds to the number of detector switches **19**.

FIG. **9** shows the arrangement of a machine **1** and a path **21** of a carriage **9** together with a point **22**. A plurality of machines **1** are arranged on both sides of a path **21** (0, 1, 2, . . .) and constitute a pair of machine lines (0 and 1, 2 and 3, 4 and 5 . . .). Further common paths **21***a* and **21***b* are provided for all machines commonly. Transportation of a carriage **9** between path **21***a* or **21***b*, and path **21** is carried out through the switch over of a point **22**. The switch over of a point **22** is carried out, as mentioned above, by the output signal of FIG. **7**. That is to say, the carriage **9** of FIG. **1** is introduced to the front of the machine of the problem through suitable control of a point **22** of FIG. **9**.

FIG. **10** shows the logical structure of a point **22**. A point **22** has sub-paths **31**, **32**, **33** and **34**, and sub-switches A, B and C. Sub-switch C connects sub-paths **31** and **34** when the control signal from gates **410** – **414** in FIG. **7** is zero, while it connects sub-paths **32** and **34** when said signal is one. Further sub-switches A and B control the transportation of the carriage between sub-path **33** and **34** through sub-path **31** or **32**. Sub-switch A connects sub-path **31** with sub-path **33** when the control signal from gates **415** – **419** in FIG. **7** is zero, and disconnects sub-path **31** with sub-path **33** when said signal is one. Sub-switch B connects or disconnects sub-path **32** with sub-path **33** according to the control signals from gates **415** – **419** in FIG. **7**.

FIG. **11** shows a circuit carried on the carriage **9** in FIG. **1**. In FIG. **11**, a circuit including drive circuit **820**, driving motor **821**, motor drive circuit **827** and handling motor **829** corresponds to driving means **7** in FIG. **1**. A circuit including gates **811** and **812**, memory **813** and coincidence circuit **815** corresponds to address comparator **8** in FIG. **1**. The rest of FIG. **11** corresponds to control circuit **4** in FIG. **1**. In FIG. **11**, reference numbers **331A**, **332A**, **316A** and **330A** mean sensors which pick up the information signal from **331**, **332**, **316** and **330** in FIG. **8** through detector switch **19** by wireless.

1. Normal signal from sensor **331A** and reverse signal from sensor **332A** are stored in memories **808** and **817** through amplifiers **800** and **801**, respectively. On one hand, a repairman watches and confirms the next address of the machine to be repaired and its direction (normal or reverse) by means of display **805**, and switches on the start switch **804**. On the basis of said information, the output **819** of motor controller **818** is applied to drive circuit **820**. Therefore, the driving motor starts to rotate in a predetermined sense, and the carriage **9** moves forward or backward according to the sense of rotation of motor **821**. Accelerator **806** controls the speed of the carriage **9** as desired.

2. Handling information from handling sensor **330A** is stored in memory **822** through amplifier **803**. Handling motor **829** rotates in a sense according to the sense of said handling information. Therefore, the chair on which a repairman sits on the carriage **9** (not shown) turns its direction to the desired machine, and memory **822** is cleared by limit switch **823**.

3. During the carriage **9** stops, output **819** of motor controller **818** is zero, therefore, said output **819** opens gate **811** through invertor **830**. Accordingly the coordinates of the goal machine as picked up by sensor **316A** is stored in memory **813** through said gate **811**. When the carriage **9** starts, gate **811** closes, and gate **812** opens. Coincidence circuit **815** provides an output signal when the output of memory **813** coincides with the output of gate **812**. Said output signal clears memories **813**, **808** and **817** to zero, causing the motor **821** stop. Thus the carriage **9** stops in front of the desired machine.

The foregoing description has been given for clearness of understanding only. No unnecessary limitations should be understood therefrom, as modifications will be obvious to those skilled in the art.

As an aid in the understanding of the logical circuits, described in this specification, a reference number table is provided below.

Reference number table

1.	loom	101.	control unit
2.	memorizing means	102.	address counter
3.	comparing means	102A.	binary-decimal converter
4.	control circuit	103.	driver
6.	direction selector circuit	104.	address line
7.	driving means	106.	data
8.	address comparator	107.	receiver
9.	carriage	108.	signal
11.	encoder	109.	register
12.	information center	110.	data
13.	buffer memory	111.	condition flag
14.	memory	112.	end flag
16.	accumulator	113.	AND gate
17.	display panel	114.	AND gate
18.	display panel	115.	AND gate
		116.	clock pulse
		117.	output signal of AND gate 115
19.	detector switch	120.	output signal
21.	path	121.	OR gate
		124	output signal of a flip-flop 151
22.	point	125.	data showing machine location
		126.	AND gate
		127.	AND gate
		128.	output signal of AND gate 130

Reference number table

31.	path
32.	path
33.	path
34.	path
135.	divided pulse
137.	AND gate
138.	zero detection circuit
139.	output signal of 138
140.	priority circuit
141.	priority signal
142.	priority signal
143.	priority signal
144.	AND gate
145.	AND gate
146.	AND gate
147.	AND gate
148.	output signal
149.	AND gate
150.	clock pulse
151.	flip-flop
152.	OR gate
153.	AND gate
154.	AND gate
155.	output signal of AND gate 153
156.	output signal of AND gate 154
157.	output signal
158.	output signal
160.	register
161.	step up circuit
162.	register
163.	register
164.	register
165.	priority detector
166.	one shot multivibrator
167.	pulse signal
168.	zero detection circuit
169.	output line
170.	AND gate
171.	flip-flop
172.	flip-flop
173.	flip-flop
174.	AND gate
175.	AND gate
176.	AND gate
177.	AND gate
178.	AND gate
215.	smaller data
216.	timing counter
217.	data register
218.	step up circuit
219.	AND gate
220.	AND gate
221.	AND gate
222.	gate
223.	gate
224.	gate
225.	zero detection circuit
226.	signal
227.	one shot multivibrator
228.	AND gate
229.	gate
230.	output line
231.	one shot multivibrator
232.	priority signal
233.	register
234.	X coordinate of machine location
235.	Y coordinate of machine location
300.	register
301.	register
302.	path number
303.	Y coordinate of a machine
304.	gate
305.	gate
306.	X coordinate of the carriage
307.	Y coordinate of the carriage
308.	comparison circuit
309.	comparison circuit
310.	comparison circuit
311.	adder
312.	output of 311 (sum)
313.	comparison circuit
621.	Y coordinate of a carriage
622.	output of 605
129.	clock pulse
130.	AND gate
131.	register
132.	step up circuit
133.	clock pulse
134.	AND gate
179	AND gate
180.	AND gate
181.	machine location data
182.	computer circuit for distance
183.	the same as 620 and 621
184.	distance data to the carriage
185.	gate
186.	flip-flop
187.	AND gate
188.	flip-flop
189.	output signal
190.	AND gate
191.	gate
192.	gate
193.	gate
195.	gate
196.	buffer register
197.	AND gate
198.	gate
199.	gate
200.	gate
201.	AND gate
202.	buffer register
203.	gate
204.	gate
205.	comparison circuit
206.	output signal
207.	machine location data
208.	machine location data
209.	gate
210.	gate
211.	AND gate
212.	AND gate
213.	AND gate
214.	larger data
314.	constant number generator
315.	gate
316.	output of 315
317.	one shot circuit
318.	decode circuit
319.	decode circuit
320.	gate circuit
324.	output of 308
325.	output of 309
327.	output signal
330.	handling
331.	normal signal
332.	reverse signal
333.	priority end signal
334.	LSD (least significant digit)
400. ~ 409	AND gate
410. ~ 419.	OR gate
600.	binary-decimal converter
601.	AND gate
602.	output of 601
603.	gate
604.	amplifier
605.	pointer
606.	pointer
607.	one shot circuit
610.	unit circuit
619.	encoder
620.	X coordinate of the carriage
813.	memory (X, Y)
814	output signal of memory 813
815.	coincidence circuit
816	output signal of coincidence circuit 815

Reference number table

623.	signal indicating carriage pass	817.	memory (reverse) motor
800. 803.	amplifier	818.	controller
804.	start switch	819.	output of 818
805.	display	820.	drive circuit
806.	accelerator	821.	driving motor
807.	output of 800	822.	memory (handling)
808.	memory (normal)	823.	limit switch
809.	output of 801	824.	detection circuit of direction of the chair
810.	output of 802	825.	output signal
811.	gate	826.	motor control circuit
812.	gate	827.	motor drive circuit
		829.	handling motor

I claim:

1. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence comprising, a driven carriage for transporting an operator to work stations in an optimum sequence, means at each work station having means developing output work information signals representative of work that is to be preformed at the individual work stations and work information signals having a priority and an address, memory means receptive of the output work information signals and work information signals for combining them into combined work information signals and memorizing them, a priority comparator circuit receptive of the combined work information signals from said memory means for determining the priority sequence of all the combined work information signals received and developing output priority address signals representative of the address priority of the sequence of work at the work stations, a direction-selector circuit receptive of the priority address signals and a signal representative of the instantaneous address of the carriage developing resultant direction signals, a control circuit receptive of the priority address signals from said priority comparator circuit and said resultant direction signals from said direction-selector circuit for developing operational command signals for driving the carriage in accordance with the command signals and having means developing a signal representative of the instantaneous address of the carriage relative to a given reference address, and a work-address comparator means for applying a stop signal to the driving means when the carriage arrives at the work stations sequentially in accordance with said priority.

2. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claim **1,** in which said means at each work station comprises a loom at each work station and said means developing the work information signals comprises means detecting a fault at a corresponding one of the looms and said work information signals comprising information content representative of the nature of the faults.

3. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claim **2,** in which said memory means comprises encoders, means connected to said encoders emitting scanning signals for said encoders, a buffer memory connected to the last mentioned means provided with a distribution circuit and a memory connected to said buffer memory.

4. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claim **3,** in which said memory means comprises accumulator means for accumulating the downtime of the individual looms, a display panel connected to said memory means and another display connected to said accumulator means.

5. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claim **4,** in which said priority comparator circuit comprises means receptive of a reference signal and means for comparing the work information signal with said reference signals for developing said output priority address signals when some of the work information signals have equal priority.

6. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claims **5** including means to shift said driving means to manual control from automatic control.

7. An automatic apparatus for transporting an operator to a plurality of work stations in an optimum sequence according to claim **1,** in which said driving means comprises means for reversibly driving said carriage.

* * * * *

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,824,558 Dated July 16, 1974

Inventor(s) HEIJI KOSHIBA

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

COL. 5, line 64, delete "gates 147 and" and insert --gate--.

COL. 6, line 8, delete "228" and insert --167--.

REFERENCE NUMBER TABLE

COL. 9

NO. 3. delete "comparing means" and insert --comparator and memory means--;

COL. 10

NO. 102A. delete "102A" and insert --102a--.

NO. 113. delete "AND".

COL. 11

NO. 144. delete "AND";

NO. 145. delete "AND";

NO. 146. delete "AND";

NO. 150. delete "clock pulse" and insert --output signal of gate 149--;

NO. 178. delete "AND";

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,824,558 Dated July 16, 1974

Inventor(s) HEIJI KOSHIBA

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

COL. 11

NO. 215. delete "smaller data" and insert --output line--;

NO. 216. delete "timing counter" and insert --initial operation control--.

COL. 12

--NO. 136. gate-- is to be added after "134. AND gate";

NO. 179. delete "AND";

NO. 180. delete "AND";

NO. 212. delete "AND":

NO. 213. delete "AND";

NO. 214. delete "larger data" and insert --output line--;

--NO. 326. output signal-- is to be added after "135. output of 309";

NO. 330. after "handling" insert --signal;

--NO. 830. inverter-- is to be added after "816. output signal coincidence circuit 815";

Signed and Sealed this

twenty-ninth Day of July 1975

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks