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(54) Title: SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING SEMICONDUCTOR STRUCTURES

(57) Abstract: A method of patterning a semiconductor film is described. According to an embodiment of the present invention, a hard mask material is formed on a silicon film having a global crystal orientation wherein the semiconductor film has a first crystal plane and second crystal plane, wherein the first crystal plane is denser than the second crystal plane and wherein the hard mask is formed on the second crystal plane. Next, the hard mask and semiconductor film are patterned into a hard mask covered semiconductor structure. The hard mask covered semiconductor structured is then exposed to a wet etch process which has sufficient chemical strength to etch the second crystal plane but insufficient chemical strength to etch the first crystal plane.

SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING SEMICONDUCTOR STRUCTURES

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[001] The present invention relates to the field of semiconductor processing and more particularly to semiconductor structures and their methods of fabrication.

2. DISCUSSION OF RELATED ART

[002] In order to increase the performance of modern integrated circuits, such as microprocessors, silicon on insulator (SOI) transistors have been proposed. Silicon on insulator (SOI) transistors have an advantage in that they can be operated in a fully depleted manner. Fully depleted transistors have an advantage of ideal subthreshold gradients for optimized on current/off current ratios. An example of a proposed SOI transistor which can be operated in a fully depleted manner is that of a tri-gate transistor 100, such as illustrated in Figure 1. Tri-gate transistor 100 includes a silicon body 104 formed on insulating substrate 102 having buried oxide layer 103 formed on a monocrystalline silicon substrate 105. A gate dielectric layer 106 is formed on the top and sidewalls of the silicon body 104 as shown in Figure 1. A gate electrode 108 is formed on the gate dielectric layer and surrounds the body 104 on three sides essentially providing a transistor 100 having three gate electrodes (G1, G2, G3) one on each of the sidewalls of the silicon body 104 and one on the top surface of the silicon body 104. A source region 110 and a drain region 112 are formed in silicon body 104 on opposite sides of gate electrode 108 as shown in Figure 1. The active channel region is the region of the silicon body located beneath gate electrode 108 and between the source region 110 and drain

region 112. An advantage of a tri-gate transistor 100 is that it exhibits good short channel effects (SCEs). One reason tri-gate transistors 100 exhibit good short channel effects is that the nonplanarity of such devices places the gate electrode 108 in such a way as to surround the active channel region on all three sides.

BRIEF DESCRIPTION OF THE DRAWINGS

[003] **Figure 1** illustrates a nonplanar or tri-gate transistor.

[004] **Figures 2A-2E** illustrate a method of forming a semiconductor structure in accordance with embodiments of the present invention.

[005] **Figure 2F** is an illustration of a nonplanar transistor formed from the structure of Figure 2E.

[006] **Figures 3A-3C** illustrate a method of forming a semiconductor structure in accordance with embodiments of the present invention.

[007] **Figures 3D** is an illustration of a nonplanar transistor utilizing a semiconductor structure of Figure 3C.

[008] **Figures 4A-4C** illustrate a method of forming a semiconductor structure in accordance with embodiments of the present invention.

[009] **Figure 4D** is an illustration of a nonplanar transistor utilizing the semiconductor structure of Figure 4C.

[0010] **Figure 5** is an illustration of a portion of an integrated circuit which includes an n type field effect transistor and a p type field effect transistor with a non parallel orientation on a substrate.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0011] Embodiments of the present invention describe semiconductor structures and methods of forming semiconductor structures. In the following description numerous specific details are set forth in order to provide a thorough understanding of the present invention. In other instances, well known semiconductor processes and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

[0012] The present invention utilizes atomic layer control of single crystalline semiconductor structures to maximize performance of semiconductor devices. In embodiments of the present invention, hard mask covered single crystalline structures are exposed to anisotropic wet etches. The wet etch has sufficient chemical strength to overcome the activation energy barrier of the chemical etching reaction in order to etch less dense planes of the semiconductor structure, but insufficient chemical strength to overcome the activation energy barrier of the chemical etching reaction, thereby not etching high density planes. By choosing proper crystal orientation and by forming a hard mask over the less dense planes of the structure and by using a wet etch chemistry with the appropriate chemical strength, one can form semiconductor structures with desired faceting, crystal orientation and sidewall smoothing. In embodiments of the present invention, natural facets in epitaxial silicon are exploited to negate edge roughness in three-dimensional silicon channel structures. In an embodiment of the present invention, natural facets are exploited to form a three-dimensional channel structure which enables good gate control of the channel region. In yet other embodiments of the present invention, semiconductor bodies of PMOS and NMOS transistors are formed with specific

arrangement on single crystalline semiconductors to exploit the crystal orientation and achieve increased mobility for both holes and electrons. Other aspects of the present invention will become obvious from the detailed description which follows.

[0013] A method of forming a three-dimensional semiconductor structure utilizing a self limiting etch and natural faceting is illustrated in Figures 2A-2F in accordance with embodiments of the present invention. The fabrication of a semiconductor structure begins with a substrate 200. In an embodiment of the present invention, substrate 200 is a silicon on insulator (SOI) substrate. A SOI substrate 200 includes a lower monocrystalline silicon substrate 202. An insulating layer 204, such as silicon dioxide or silicon nitride, is formed on monocrystalline substrate 202. A single crystalline silicon film 206 is formed on the top of the insulating layer 204. Insulating layer 204 is sometimes referred to as a "buried oxide" or a "buried insulating" layer and is formed to a thickness sufficient to isolate single crystalline silicon film 206 from lower monocrystalline silicon substrate 202. In an embodiment of the present invention, the insulating layer is a buried oxide layer formed to a thickness between 200-2000Å. In an embodiment of the present invention, the silicon film 206 is an intrinsic (i.e., undoped) silicon epitaxial film. In other embodiments, the single crystalline silicon film 206 is doped to a p type or n type conductivity with a concentration level between $1x10^{16}$ - $1x10^{19}$ atom/cm^3. Silicon film 206 can be insitu doped (i.e., doped while it is deposited) or doped after it is formed on insulating layer 204 by, for example, ion implantation. Doping silicon film 206 after it is deposited enables both n type devices and p type devices to be fabricated on the same substrate. In an embodiment of the present invention, silicon film 206 is formed to a thickness which is approximately equal to the height desired of the subsequently formed silicon structure. In an embodiment of the present invention, the single crystalline silicon film 206 has a thickness of less than 30 nanometers and ideally around 20 nanometers or less.

[0014] A silicon on insulator (SOI) substrate 200 can be formed in any well known method. In one method of forming the silicon on insulator substrate, known as the

SIMOX technique, oxygen atoms are implanted at a high dose into a single crystalline silicon substrate and then annealed to form buried oxide 204 within the substrate. The portion of the single crystalline silicon substrate above the buried oxide becomes the silicon film 206. Another technique currently used to form SOI substrates is an epitaxial silicon film transfer technique which is generally referred to as "bonded SOI". In this technique, a first silicon wafer has a thin oxide grown on its surface that will later serve as the buried oxide 204 in the SOI structure. Next, a high dose hydrogen implant is made into the first silicon wafer to form a stress region below the silicon surface of the first wafer. The first wafer is then flipped over and bonded to the surface of a second silicon wafer. The first wafer is then cleaved along the high stress plane created by the hydrogen implant. The cleaving results in a SOI structure with a thin silicon layer on top, the buried oxide underneath, all on top of the second single crystalline silicon wafer. Well known smoothing techniques, such as HCl smoothing or chemical mechanical polishing (CMP) can be used to smooth the top surface of the silicon film 206 to its desired thickness.

[0015] Although the present invention will be described with respect to silicon structures formed on silicon on insulator (SOI) substrates, the present invention can be carried out on standard monocrystalline silicon wafers or substrates to form a "bulk" device. The silicon structures can be formed directly from the monocrystalline silicon wafer or formed from epitaxial silicon films formed on a monocrystalline silicon substrate. Additionally, although embodiments of the present invention are illustrated with respect to the formation of single crystalline silicon structures and devices formed therefrom, the methods and structures of the present invention are equally applicable to other types of semiconductors, such as but not limited to germanium (Ge), a silicon germanium alloy (Si_xGe_y), gallium arsenide (GaAs), indium antimonide (InSb), gallium phosphide (GaP), and gallium antimonide (GaSb). Accordingly, embodiments of the present invention include semiconductor structures and methods of forming semiconductor structures utilizing semiconductors, such as but not limited to germanium (Ge), a silicon germanium

alloy (Si_xGe_y), gallium arsenide (GaAs), indium antimonide (InSb), gallium phosphide (GaP), and gallium antimonide (GaSb).

[0016] In Figure 2A, single crystalline silicon film 206 has a (100) global crystal orientation, as defined by the $\overline{xy}$ plane. A silicon film with a (100) global crystal orientation has a <100> plane which is planar with the surface of the film. That is, as illustrated in Figure 2A, a single crystalline silicon film with a (100) global crystal orientation has a <100> plane which lies in the $\overline{xy}$ plane with a normal axis in the z direction.

[0017] In the following description round brackets ( ) are used to illustrate the global crystal orientation of the film, as defined by the $\overline{xy}$ plane and along the z direction, while pointed brackets < > are used to describe specific local planes within said globally defined crystalline film.

[0018] Additionally, as illustrated in Figure 2A, a single crystalline silicon with a (100) crystal orientation has a pair of <110> planes which are perpendicular to one another. That is, the (100) single crystalline silicon has a <110> plane which lies in the $\overline{zx}$ plane with a normal axis extending in the **y** direction and has a <110> plane which lies in the $\overline{zy}$ plane and with a normal axis in the x direction. In an embodiment of the present invention, silicon film 206 with a (100) global crystal orientation is etched to form a silicon structure which has a pair of laterally opposite sidewalls which are formed from the <110> plane and a second pair of laterally opposite sidewalls, perpendicular thereto, which lie in the <110> plane.

[0019] In order to etch silicon film 206 into a silicon body, a hard mask material 208 can be formed on the top surface 219 of silicon film 206. Hard mask material 208 is a material which can provide a hard mask for etching of silicon film 206. Hard mask material 208 is a material which can retain its profile during the etching of silicon film 206. Hard mask material 208 is a material which will not etch or will only slightly etch during the etching of silicon film 206. In an embodiment of the present invention, the hard mask material is formed of a material such that the etchant used to etch silicon film

206 will etch silicon film 206 at least 5 times faster than the hard mask material and ideally at least 10 times faster. That is, in an embodiment of the present invention, the silicon film and the hard mask are chosen to provide an etch selectivity of at least 5:1 and ideally at least 10:1. In an embodiment of the present invention, hard mask material 208 is formed from silicon nitride or silicon oxynitride. In an embodiment of the present invention, hard mask material 208 is formed from a silicon nitride film with between 0-5% carbon, formed by a low pressure chemical vapor deposition (LPCVD) process. Hard mask material 208 is formed to a thickness sufficient to retain its profile during the entire etch of silicon film 206 but not too thick to cause difficulties in patterning. In an embodiment of the present invention, the hard mask material 208 is formed to a thickness between 3 nanometers to 50 nanometers and ideally to a thickness around 10 nanometers.

[0020] Next, as also shown in Figure 2B, a photoresist mask 210 is formed on hard mask material 208. Photoresist mask 210 contains the feature pattern to be transferred into silicon film 206. Photoresist mask 210 can be formed by any well known technique, such as by blanket depositing photoresist material and then masking, exposing and developing the photoresist material into a photoresist mask 210 having the desired pattern for a silicon film 206. Photoresist mask 210 is typically formed of an organic compound. Photoresist mask 210 is formed to a thickness sufficient to retain its profile while patterning hard mask film 208 but yet is not formed too thick to prevent its lithographic patterning into the smallest dimensions (i.e., critical dimensions) possible with the photolithography system and process used. In an embodiment of the present invention, photoresist mask 210 is orientated on single crystalline silicon film 206 so as to define a photoresist mask with a pair of laterally opposite sidewalls aligned with a <110> crystal plane and a second pair of laterally opposite sidewalls, perpendicular to the first, aligned with the <110> plane.

[0021] Next, as shown in Figure 2C, hard mask material 208 is etched in alignment with photoresist mask 210 to form a hard mask 212 as shown in Figure 2C. Photoresist mask 210 prevents the underlying portion of hard mask material 208 from being etched.

In an embodiment of the present invention, the hard mask material 208 is etched with an etchant which can etch the hard mask material but does not etch the underlying silicon film 206. In an embodiment of the present invention, the hard mask material is etched with an etchant that has almost perfect selectivity to the underlying silicon film 206. That is, in an embodiment of the present invention, the hard mask etchant etches the hard mask material 208 at least 20 times faster than the underlying silicon film 206 (i.e., etchant has a hard mask to silicon film selectivity of at least 20:1). When hard mask material 208 is a silicon nitride or silicon oxynitride film, hard mask material 208 can be etched into a hard mask 212 utilizing a dry etch process, such as a reactive ion etching. In an embodiment of the present invention, a silicon nitride or silicon oxynitride hard mask is reactively ion etched utilizing a chemistry comprising CHF_3 and O_2 and Ar.

[0022] Next, as also shown in Figure 2C, after hard mask film 208 has been patterned into a hard mask 212, photoresist mask 210 may be removed by well known techniques. For example, photoresist mask 210 may be removed utilizing "piranha" clean solution which includes sulfuric acid and hydrogen peroxide. Additionally, residue from the photoresist mask 210 may be removed with an O_2 ashing.

[0023] Although not required, it is desirable to remove photoresist mask 210 prior to patterning silicon film 206 so that a polymer film from the photoresist does not form on the sidewalls of the patterned silicon film 206. For example, when silicon film 206 is used as a semiconductor body or fin in a nonplanar device, it is desirable to first remove the photoresist mask prior to etching the silicon film because dry etching processes can erode the photoresist mask and cause polymer films to develop on the sidewalls of the silicon body which can be hard to remove and which can detrimentally affect device performance.

[0024] Next, as shown in Figure 2D, silicon film 206 is etched in alignment with hard mask 212 to form a patterned silicon film 214 which has a first pair of laterally opposite sidewalls 218 aligned with the <110> crystal plane and a second pair of laterally opposite sidewalls 220 aligned with the <110> crystal plane. Hard mask 212 prevents the underlying portion of silicon film 206 from being etched during the etch process. In an

embodiment of the present invention, the etch is continued until the underlying buried oxide layer 204 is reached. Silicon film 206 is etched with an etchant which etches silicon film 206 without significantly etching hard mask 212. In an embodiment of the present invention, silicon film 206 is etched with an etchant which enables silicon film 206 to be etched at least 5 times and ideally 10 times faster than hard mask 212 (i.e., etchant has a silicon film 206 to hard mask 212 etch selectivity of at least 5:1 and ideally at least 10:1). Silicon film 206 can be etched utilizing any suitable process. In an embodiment of the present invention, silicon film 206 is anisotropically etched so that the silicon body 214 has nearly vertical sidewalls 218 formed in alignment with the sidewalls of hard mask 212. When hard mask 212 is a silicon nitride or silicon oxynitride film, silicon film 206 can be etched utilizing a dry etch process, such as a reactive ion etch (RIE) or plasma etch with a chemistry comprising Cl_2 and HBr.

[0025] After etching silicon film 206 to form silicon body or structure 214, the sidewalls 218 will typically have a line edge roughness 222 of about 2-4 nanometers. When forming a silicon body or structure with a width between sidewalls 218 of only 20-30 nanometers, such a surface roughness is unacceptably large and can detrimentally affect device performance.

[0026] Accordingly, in an embodiment of the present invention, the silicon structure 214 is exposed to a wet etch or a "faceting" etch while hard mask 212 is present on structure 214 in order to remove the edge roughness and/or to tailor the shape of the structure to enhance device performance. In an embodiment of the present invention, the hard mask 212 capped silicon structure 214, is exposed to an anisotropic wet etch. The wet etchant has sufficient chemical strength to overcome the activation energy barrier of the chemical etching reaction in order to etch less dense planes of the semiconductor structure, but insufficient chemical strength to overcome the activation energy barrier of the chemical etching reaction, thereby not etching high density planes.

[0027] In an embodiment of the present invention, a wet etch chemistry and process are used which can etch the less dense <100> and <110> planes but which cannot etch the

higher density <111> planes. Because hard mask 212 covers the less dense <100> plane on the top surface of the silicon structure 214, said less dense plane is protected from etching. Because the less dense plane <100> on the top surface is shielded and because the etch does not have a sufficient chemical strength to etch the <111> plane, the wet etch stops on the first total intact or contiguous <111> plane as shown in Figure 2E. In this way, the "faceting" or wet etch is self limiting. Thus, upon self-limitation of the wet etch, only <111> planes and etch-resistant films used to shield the less dense <110> and <100> planes remain exposed. The faceting etch of the present invention can be said to be an anisotropic etch because it etches in one direction at one rate while etching in other directions at a second slower rate or not at all. Because the etch process etches the <100> and <110> planes but not the <111> planes, the faceting or wet etch forms a silicon structure 230 having sidewalls 232 defined by the <111> plane as shown in Figure 2E. The anisotropic wet etch removes the surface roughness 222 from sidewalls 218 (Figure 2D) and generates optically smooth sidewalls 232 as shown in Figure 2E. Additionally, after exposing the structure 214 to the faceting etch for a sufficient period of time, sidewalls 218 are defined by the <111> plane and generate a structure 230 with a v-shape or inwardly tapered sidewalls 232. The sidewalls 232 angle inward from the top surface 219 of structure 230 at an angle ***alfa*** of 62.5 degrees. In an embodiment of the present invention, the top surface 219 of structure 230 has a width (W1) between laterally opposite sidewalls 232 of between 20-30 nm and the bottom surface has a width (W2) between laterally opposite sidewalls of between 10-15 nm.

[0028] In an embodiment of the present invention, the wet etch or "faceting" etch is a hydroxide based etch with a sufficiently low hydroxide concentration and nucleophillicity (i.e. chemical strength) so that there is no etching of the fully intact <111> planes. In an embodiment of the present invention, structure 214 is exposed to a faceting or wet etch which comprises less than 1% ammonia hydroxide (NH_4OH) by volume. In an embodiment of the present invention, structure 214 is exposed to a wet etchant comprising between 0.2-1% NH_4OH by volume at a temperature range between 5-25°C. In an

embodiment of the present invention, sonic energy at the frequency range between 600-800 kilohertz dissipating between 0.5-3 watts/cm^2 is applied to the etch solution during the faceting etch. In an embodiment of the present invention, the hard mask capped silicon structure is exposed to the faceting etch for between 15 seconds – 5 minutes.

[0029] In another embodiment of the present invention, the faceting or wet etch can comprise ultra-dilute (< 0.1% by volume) aqueous solutions of tetraalkylammonium hydroxides (e.g. tetraethylammonium hydroxide and tetramethylammonium hydroxide at a temperature between 5 and 20°C).

[0030] The fabricated silicon structure 230 can be used to fabricate semiconductor devices, such as transistors and capacitors, as well as micro-electrical mechanical systems (MEMS) and opto-electronic devices. In an embodiment of the present invention, semiconductor structure 230 is used as a semiconductor body or fin for a nonplanar or thee-dimensional transistor, such as but not limited to a tri-gate transistor, a dual gate transistor, a FINFET, an omega-FET or a pi-FET.

[0031] In an embodiment of the present invention, silicon structure 230 provides a silicon body or fin for a tri-gate transistor 240 illustrated in Figure 2F. In order to fabricate a tri-gate transistor 240 as illustrated in Figure 2F, hard mask 212 is removed from silicon structure 230. In an embodiment of the present invention, when hard mask 212 is a silicon nitride or silicon oxynitride film, a wet etch comprising phosphoric acid in de-ionized water may be used to remove the hard mask. In an embodiment of the present invention, the hard mask etchant comprises an aqueous solution of between 80-90% phosphoric acid (by volume) heated to a temperature between 150-170°C and ideally to 160°C. In an embodiment of the present invention, after removing hard mask 212, the substrate can be cleaned utilizing standard SC1 and SC2 cleans. It is desirable to clean the substrate after removal of the hard mask with phosphoric acid because phosphoric acid typically includes many metallic impurities which can affect device performance or reliability. It is to be appreciated that if one desires to form a FINFET or a dual gate device, the hard mask 212 may be left on silicon structure 230 in order to isolate the top

surface of the semiconductor structure 230 from control by a subsequently formed gate electrode.

[0032] Next, a gate dielectric layer 250 is formed on the sidewalls 232 as well as on the top surface of semiconductor body 230. Gate dielectric layer 250 can be any well known and suitable gate dielectric layer, such as but not limited to a silicon dioxide or silicon nitride gate dielectric layer. Additionally, gate dielectric layer 250 can be a high-k gate dielectric layer, such as but not limited to hafnium oxide, zirconium oxide, titanium oxide and tantalum oxide. Any well known technique, such as but not limited to chemical vapor deposition and atomic layer deposition may be utilized to form gate dielectric layer 250.

[0033] Next, a gate electrode 260 is formed on gate dielectric layer 250 on the top surface and sidewalls of semiconductor structure 230 as illustrated in Figure 2F. Gate electrode 260 is formed perpendicular to sidewalls 232. The gate electrode can be formed from any well known gate electrode material, such as but not limited to doped polycrystalline silicon, as well as metal films, such as but not limited to tungsten, tantalum, titanium, and their nitrides. Additionally, it is to be appreciated that a gate electrode need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a lower metal film formed on the gate dielectric layer with a top polycrystalline silicon film. The gate dielectric layer and gate electrode may be formed by blanket depositing or growing the gate dielectric layer over the semiconductor body and then blanket depositing a gate electrode material over the gate dielectric layer. The gate dielectric layer and gate electrode material may then be patterned with well know photolithography and etching techniques to form gate electrode 260 and gate dielectric layer 250 as illustrated in Figure 2F. Alternatively, the gate dielectric layer and gate electrode may be formed utilizing a well known replacement gate process. A source region 272 and a drain region 274 are formed in silicon body 230 on opposite sides of gate electrode 260 as illustrated in Figure 2F. Any well known and suitable technique, such as solid source diffusion or ion implantation may be used to form source and drain regions.

In an embodiment of the present invention, the source region 272 and drain region 274 are formed to a concentration between $1x10^{19} - 1x10^{21}$ atoms/cm^3.

[0034] The fabricated nonplanar transistor 240 includes a semiconductor body 230 surrounded by gate dielectric layer 250 and gate electrode 260 as shown in Figure 2F. The portion of the semiconductor body 230 located beneath the gate dielectric and gate electrode is the channel region of the device. In an embodiment of the present invention the source and drain region are doped to a first conductivity type (n type or p type) while the channel region is doped to a second opposite conductivity type (p type or n type) or is left undoped. When a conductive channel is formed by gate electrode 260 in the channel region of silicon body 230, charges (i.e., holes or electrons) flow between the source and drain region along the <110> plane in silicon body 230. That is, in transistor 240, charge migration is along the <110> crystal plane in structure 240. Is has been found that charge migration in the <110> direction provides good hole mobility. Accordingly, in an embodiment of the present invention, device 240 is a p type device where the source and drain regions are formed to a p type conductivity and where the carriers are holes. Additionally, by inwardly tapering the sidewalls of silicon body 230, gate electrode 260 has good control over the channel region of body 230 enabling fast turn "on" and turn "off" of transistor 240.

[0035] Figures 3A-3D illustrate a method of forming a monocrystalline silicon body or structure in accordance with another embodiment of the present invention. As shown in Figure 3A, a hard mask 312 is formed on a single crystalline silicon film 306 having a (100) global crystal orientation. Hard mask 312 can be formed as described above. In Figure 3A, however, the hard mask 312 is orientated on silicon film 306 to produce a pair of sidewalls which are aligned with the <100> plane and a second pair of sidewalls which are also aligned to the <100> plane. (It is to be appreciated that the orientation of hard mask 312 is rotated approximately 45° in the $\overline{xy}$ plane from the orientation of hard mask 212 in Figure 2A.)

[0036] Next, as illustrated in Figure 3B, the (100) global crystal orientation silicon film 306 is etched in alignment with the hard mask 312 to produce a silicon structure 314 which has a pair of laterally opposite sidewalls 318 which are aligned with the <100> plane and a second pair of sidewalls 320, which are perpendicular to the first pair and which are also aligned with the <100> plane. Silicon film 306 can be etched as described above.

[0037] Next, the silicon structure 314 is exposed to a faceting wet etch while hard mask 312 is present on the top surface 319 of silicon structure 314. The faceting wet etch has a sufficient chemical strength to etch the less dense <110> and <100> planes but insufficient strength to etch the high density <111> plane. Because the less dense <100> plane on the top surface 319 of the silicon structure 314 is covered by the hard mask 312 and because the etch does not have sufficient chemical strength to etch the <111> plane, the silicon structure 314 is transformed into a silicon structure 330 having a pair of sidewalls 332 having a "V" notched shape formed by intersecting <111> planes as illustrated in Figure 3C. As before, the faceting etch is self limiting, and stops at the first contiguous <111> planes. The <111> planes of sidewalls 332 meet at an angle β of approximate 55°. A combination of crystal orientation, atom shielding, and a well-controlled anisotropic wet etch enables the formation of silicon structure 330 with "V" notch sidewalls 332.

[0038] As discussed above, the silicon structure 330 can be used to create silicon nonplanar or three-dimensional devices as well as micro-machines and MEMS devices. In an embodiment of the present invention, the silicon structure 330 is used to form a nonplanar transistor, such as a tri-gate transistor 330 as illustrated in Figure 3D. Gate electrode 360 is formed perpendicular to sidewalls 332 as shown in Figure 3D. The nonplanar device has a gate dielectric layer 350 and a gate electrode 360 formed over and around a portion of silicon body 330 as illustrated in Figure 3D. A source region 372 and a drain region 374 are formed in the silicon body 330 on opposite sides of the gate electrode. The charge migration from the source to the drain region in transistor 340 is

parallel to or in alignment with the <100> plane. Because charge migration is along the <100> plane, the silicon structure 330 provides good electron mobility and is therefore ideal for use in the fabrication of an n type field effect transistor (NFET) where the carriers are electrons and the source region 372 and drain regions 374 are n type conductivity.

[0039] Figures 4A-4D illustrates a method of forming a semiconductor body or structure in accordance with another embodiment of the present invention. As shown in Figure 4A, a substrate 400, such as a silicon on insulator (SOI) substrate which includes a lower monocrystalline silicon substrate 402, a buried oxide layer 404 and a single crystalline silicon film 406 is provided. Although, a silicon on insulator substrate 400 is ideally used, other well known semiconductor substrates can be used as set forth above. In an embodiment of the present invention, single crystalline silicon film 406 has a (110) global crystal orientation as shown in Figure 4A. A single crystalline silicon film with a (110) global crystal orientation has a <110> plane of the silicon lattice which is planar to or parallel with the surface of the film. That is, as illustrated in Figure 4A, a single crystalline silicon film with a (110) global crystal orientation has a <110> plane in the $\overline{xy}$ plane with a normal axis in the z direction. Additionally, a single crystalline silicon film with a (110) global crystal orientation has <111> planes and <110> planes which are orthogonal to each other and orthogonal to a <110> plane. That is, in a single crystalline silicon film 406 with (110) global crystal orientation there are <111> planes which lie in the $\overline{xz}$ plane with normal axis in the y direction and there are <110> planes which lie in the $\overline{zy}$ plane and have a normal axis in the x direction as shown in Figure 4A. Next, a hard mask 412, as shown in Figure 4A, is formed on single crystalline silicon film 406 having a (110) crystal orientation as described above. Hard mask 412 is orientated on silicon film 406 to produce a pair of sidewalls aligned with <110> plane and a second pair of perpendicular sidewalls which are aligned with the <111> plane. Hard mask 412 can be formed of materials and by methods described above.

[0040] Next, as illustrated in Figure 4B, the (110) silicon film is etched in alignment with hard mask 412 to produce a silicon structure 414 which has a pair of laterally opposite sidewalls 418 which are parallel with or aligned with the <110> plane and a second pair of sidewalls 420, which are perpendicular to the first pair 418 which are parallel with or aligned with a <111> plane. Hard mask 412 capped silicon structure 414 is then exposed to a faceting wet etch. The faceting wet etch has sufficient chemical strength to etch the less dense <110> plane, but insufficient chemical strength to etch the higher density <111> plane. Because the less dense <110> plane of the top surface 419 is covered by hard mask 412 and because the etch does not have sufficient chemical strength to etch the <111> plane, structure 414 is transformed into structure 430 having a pair of laterally opposite sidewalls 432 defined by <111> planes as illustrated in Figure 4C. After exposing structure 414 to the faceting etch for a sufficient period of time, the sidewalls 432 are defined by the <111> planes and generate a structure with a v-shape or inwardly tapered sidewalls. The sidewalls 432 angle inward from the top surface 419 of structure 430 at an angle ***gamma*** of approximately 62.5 degrees. In an embodiment of the present invention, the top surface 419 has a width (W1) between laterally opposite sidewalls 430 of between 20 – 30 nm and a bottom surface has width (W2) between laterally opposite sidewalls 440 of between 10 – 15 nm. A combination of crystal orientation, hard mask shielding, and a wet etch with the appropriate chemical strength enables the formation of silicon structure 430 with inwardly tapered sidewalls 432.

[0041] As discussed above, structure 430 can be used to create a variety of well known semiconductor devices, such as silicon nonplanar or three-dimensional devices, as well as opto-electronic devices and MEMS devices. In an embodiment of the present invention, the silicon structure 430 is used to form a silicon body of nonplanar transistor, such as a tri-gate transistor 440, as illustrated in Figure 4D. The tri-gate transistor 440 has a gate dielectric layer 450 and a gate electrode 460 formed over and around a portion of silicon body 430 as illustrated in Figure 4D. The gate electrode 460 runs in a direction perpendicular to sidewalls 432 as shown in Figure 4D. The gate dielectric layer 450 and

gate electrode 460 may be formed of any suitable material and suitable known method, such as described above. A source region 472 and a drain 474 are formed in silicon body 430 on opposite sides of gate electrode 460 as illustrated in Figure 4D. The charge migration from the source region 472 to the drain region 474 in silicon body 430 is parallel to or in alignment with the <110> plane. The inwardly tapered sidewalls 432 of silicon body 430 provide good gate control 460 of the channel region of the device which enables the fast turn "on" and turn "off" of device 440.

[0042] Although the present invention thus far has been described with respect to the shaping or "faceting" of single crystalline silicon structures utilizing a combination of crystal orientation, hard mask shielding, and well controlled wet etchants, concepts of the present invention are equally applicable to other types of single crystalline semiconductor films, such as but not limited to germanium (Ge), a silicon germanium alloy (Si_xGe_y), gallium arsenide (GaAs), indium antimonide (InSb), gallium phosphide (GaP), and gallium antimonide (GaSb). For example, a single crystalline indium antimonide (InSb) structure can be faceted utilizing a wet etchant comprising an aqueous solution of 0.05-0.1 mol/L citric acid at a temperature range between 5-15°C. Similarly, a single crystalline gallium arsenide (GaAs) structure can be faceted by exposing a hard mask covered gallium arsenide structure to a wet etchant comprising an aqueous solution of less than 0.05 mol/L citric acid at a temperature range between 5-15°C.

[0043] Additionally, in an embodiment of the present invention, an integrated circuit is formed from a p type transistor and an n type transistor 520 which are orientated and/or shaped to optimize the performance of each type of transistor. For example, as illustrated in Figure 5, in an embodiment of the present invention a single crystalline silicon film having a (100) global crystal orientation is patterned as described with respect to Figures 2A-2F to form a silicon body 512 for a p type nonplanar transistor 510 wherein the charge (hole) migration is parallel with a <110> plane and is also patterned as described with respect to Figures 3A-3D to form a silicon body 522 for a n type nonplanar transistor 520 wherein charge (electron) migration is parallel with a <100> plane. Accordingly, in an

embodiment of the present invention, a p type nonplanar transistor and an n type nonplanar transistor are orientated in a non-parallel (e.g., 45°C offset) manner with respect to one another on a substrate in order to optimize the hole mobility for the p type transistor and the electron mobility for the n type transistor. In other embodiments of the present invention, the semiconductor bodies of the p type device and the n type device are oriented with respect to one another to enable the faceting etch to shape the bodies into structures which optimize performance for each device type. In this way, the performance of an integrated circuit which includes both an n type nonplanar transistor and a p type nonplanar transistor can be greatly improved.

IN THE CLAIMS

We claim:

1. A method of patterning a semiconductor film comprising:

forming a hard mask material on a semiconductor film having a global crystal orientation wherein the semiconductor film has a first crystal plane and a second crystal plane wherein said first crystal plane is denser than the second crystal plane and wherein said hard mask is formed on said second crystal plane;

patterning said semiconductor film and said hard mask material into a hard mask covered semiconductor structure; and

exposing said hard mask covered semiconductor structure to a wet etch process which has sufficient chemical strength to etch said second crystal plane but insufficient chemical strength to etch said first crystal plane.

2. The method of claim 1 wherein said semiconductor film is silicon.

3. The method of claim 1 wherein said semiconductor film is selected from the group consisting of germanium (Ge), silicon germanium alloy (Si_xGe_y), gallium arsenide (GaAs), indium antimonide (InSb), gallium phosphide (GaP), and gallium antimonide (GaSb).

4. A method of patterning a monocrystalline silicon film comprising:

forming a hard mask on a monocrystalline silicon film;

etching said monocrystalline silicon film in alignment with said hard mask to form a hard mask covered monocrystalline silicon structure with a top surface and a pair of laterally opposite sidewalls; and

exposing said hard mask covered monocrystalline silicon film to a wet chemical etchant to etch away a portion of said monocrystalline silicon film wherein said etchant is self-limiting so that it stops on the first contiguous <111> crystalline plane.

5. The method of claim 4 wherein said monocrystalline silicon film has a (100) global crystal orientation.

6. The method of claim 5 wherein after etching said silicon structure said sidewalls are aligned with a <110> plane.

7. The method of claim 5 wherein after etching said silicon structure said sidewalls are aligned with a <100> plane.

8. The method of claim 4 wherein said monocrystalline silicon film has a (110) global crystal orientation.

9. The method of claim 8 wherein after etching said silicon structure said sidewalls are aligned with a <110> plane.

10. The method of claim 4 further comprising after exposing said structure to said wet etch, forming a gate dielectric and a gate electrode above said top surface of said silicon structure and on said sidewalls of said structure.

11. The method of claim 10, further comprising removing said hard mask prior to forming said gate dielectric and gate electrode.

12. The method of claim 10 further comprising forming a source region and drain region in said silicon structure on opposite sides of said gate electrode.

13. The method of claim 4 wherein said wet etch has a chemical strength sufficient to etch <100> and <110> planes but insufficient chemical strength to etch <111> planes.

14. The method of claim 4 wherein said wet etchant comprises NH_4OH.

15. The method of claim 14 wherein said wet etchant comprises NH_4OH and water, wherein said NH_4OH concentration is less than 1% by volume.

16. The method of claim 15 wherein said NH_4OH concentration is between 0.2-1% by volume and said etchant has a temperature between 5-25°C.

17. An integrated circuit comprising:

a first nonplanar transistor having a first semiconductor body, wherein charge migration in said first semiconductor body is along a first direction; and

a second nonplanar transistor having a second semiconductor body, wherein charge migration in said second semiconductor body is along to a second direction wherein said second direction is not parallel to said first direction.

18. The integrated circuit of claim 17 wherein said first direction is approximately 45 degrees with respect to said second direction.

19. The integrated circuit of claim 17 wherein said first nonplanar transistor is an n type field effect transistor and wherein said first semiconductor body is formed from a single crystalline silicon film and wherein said first direction is parallel to a <100> plane of said silicon crystalline silicon film.

20. The integrated circuit of claim 17 wherein said second nonplanar transistor is a p type field effect transistor and wherein said single crystalline second semiconductor body is a single crystalline silicon film and wherein said second direction is parallel to a <100> plane.

21. The integrated circuit of claim 17 wherein said second nonplanar transistor is a p type field effect transistor and wherein said first semiconductor body is formed from a single crystalline silicon film and wherein said first direction is parallel to a <110> plane of said silicon film, and wherein said first nonplanar transistor is a n type field effect transistor, wherein said second semiconductor body is a single crystalline silicon film, and wherein said second direction is parallel to a <100> plane.

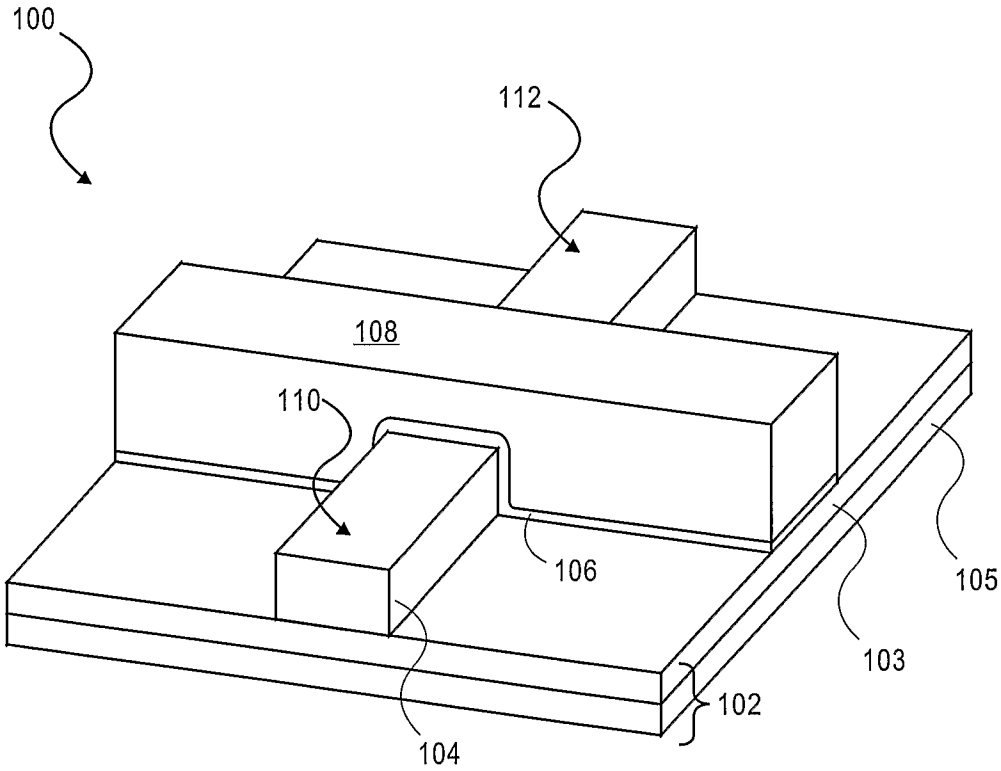

FIG. 1
(PRIOR ART)

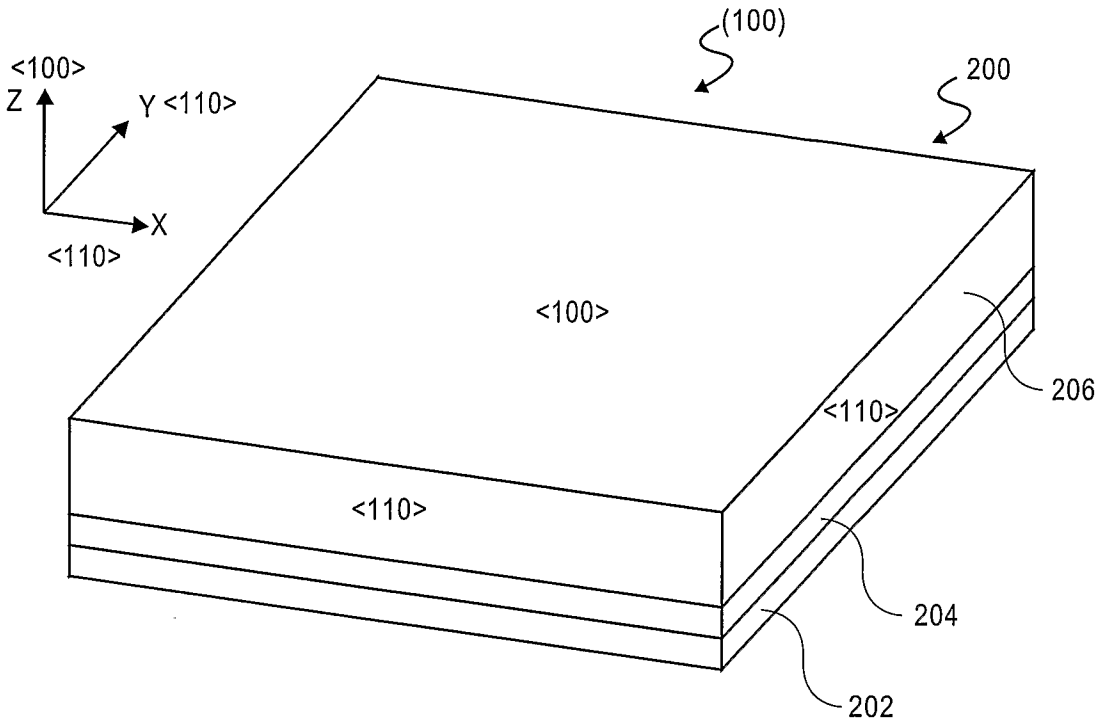
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FIG. 2A

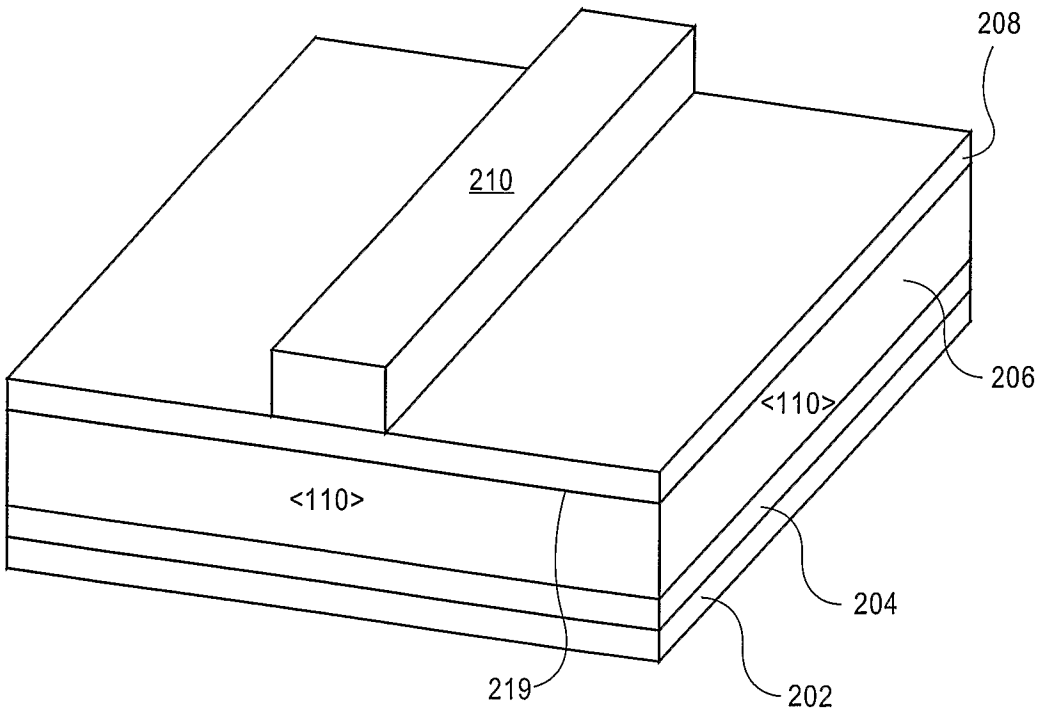
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FIG. 2B

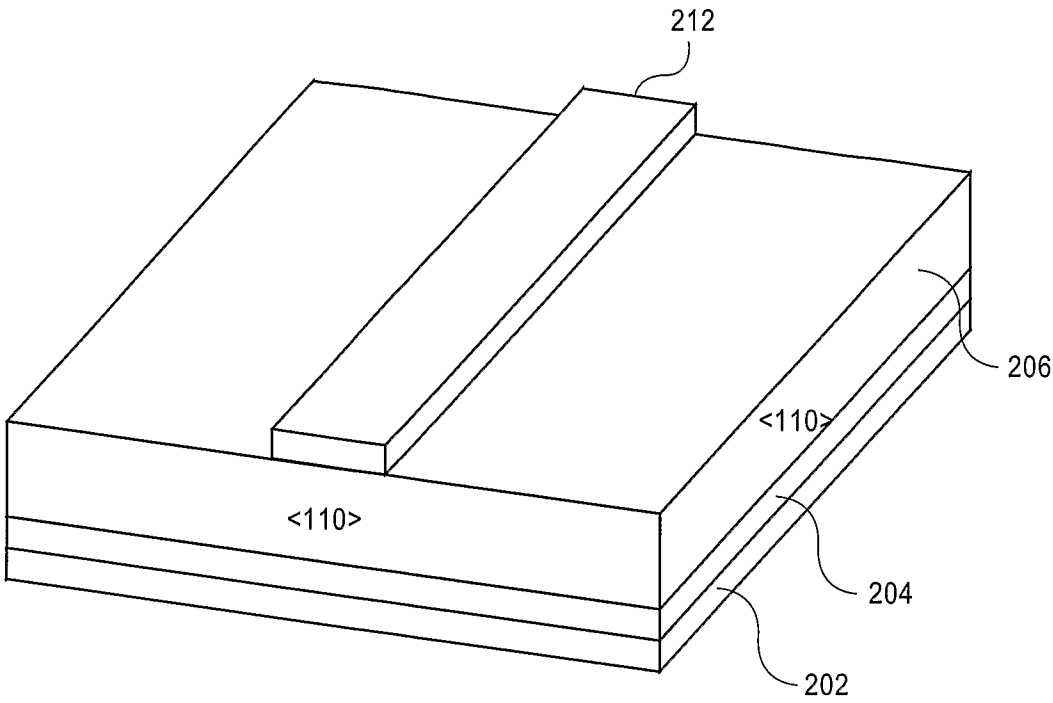
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FIG. 2C

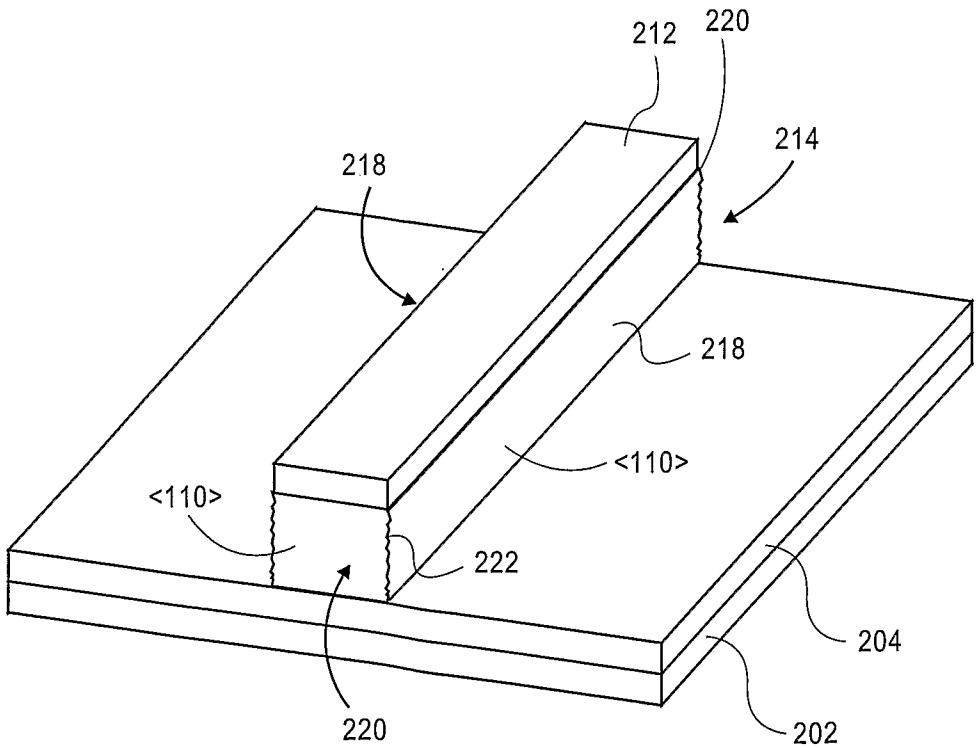
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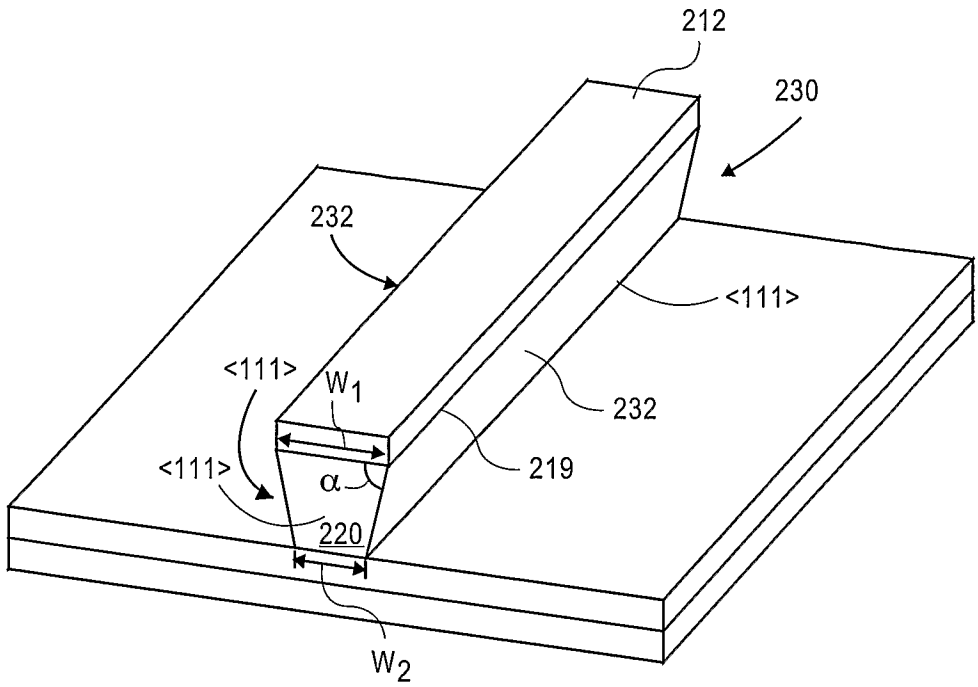
FIG. 2D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α
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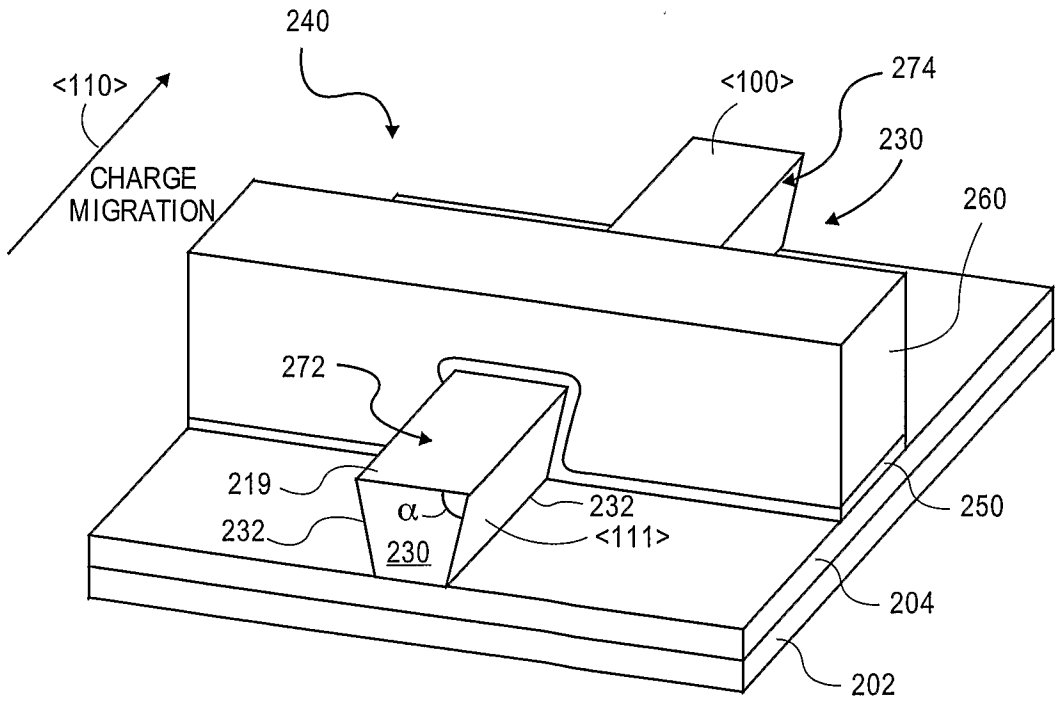
W2

FIG. 2E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α
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250
204
202

FIG. 2F

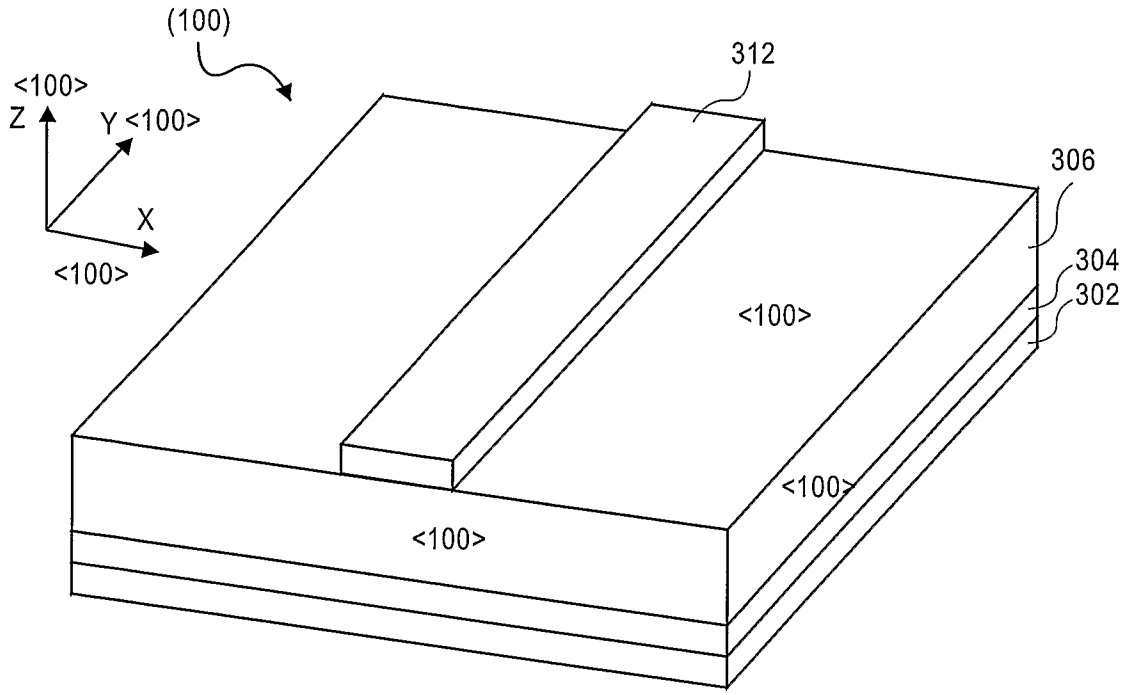
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FIG. 3A

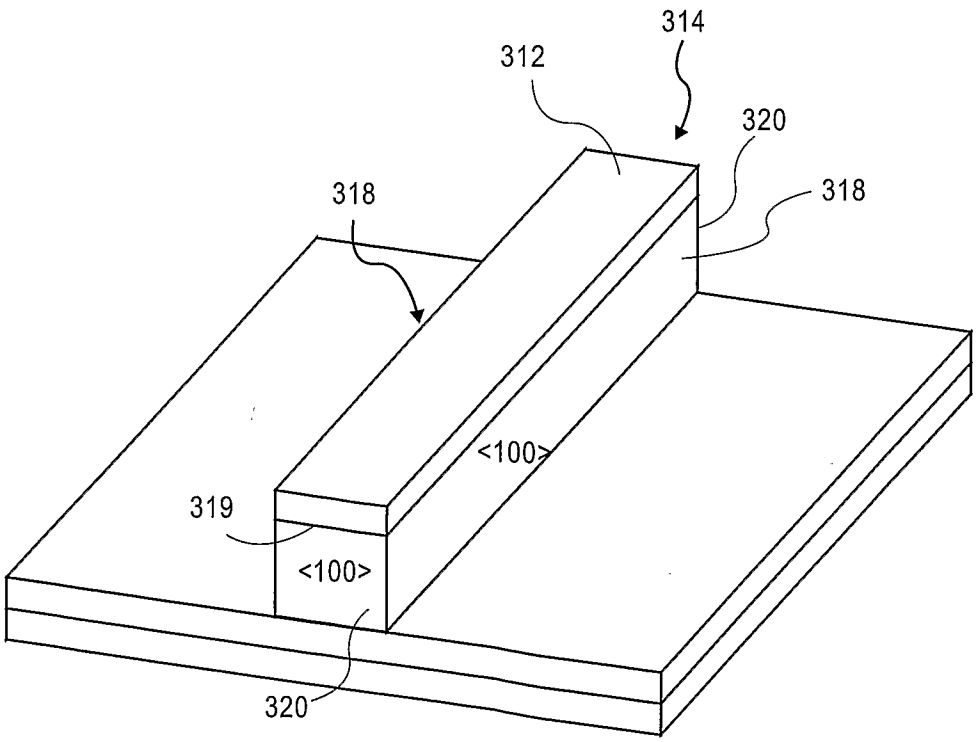
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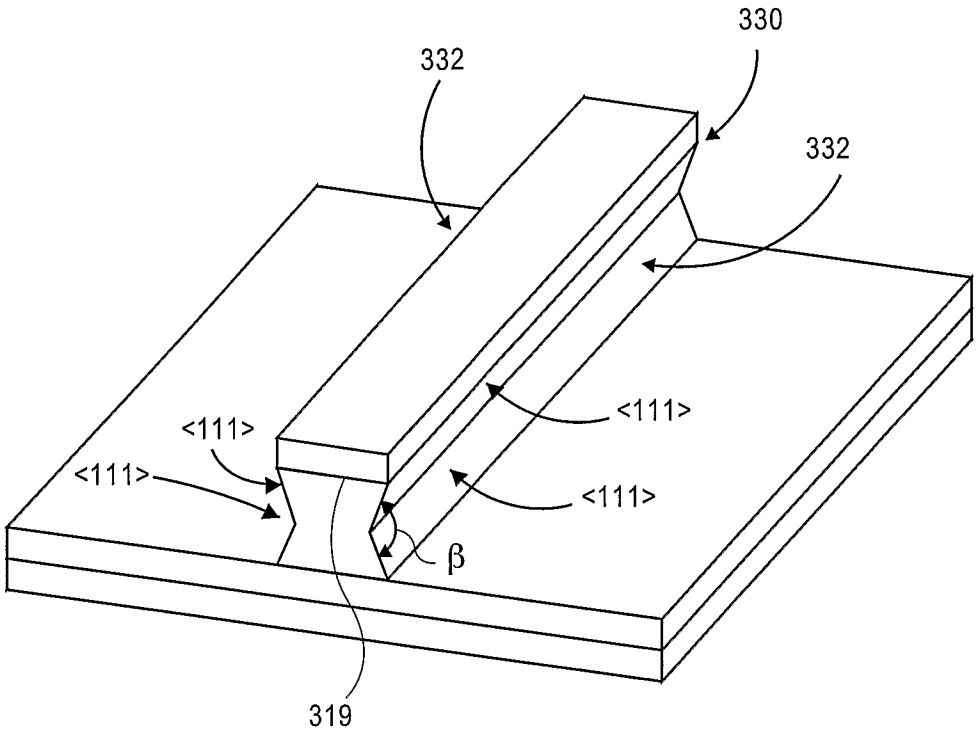
FIG. 3B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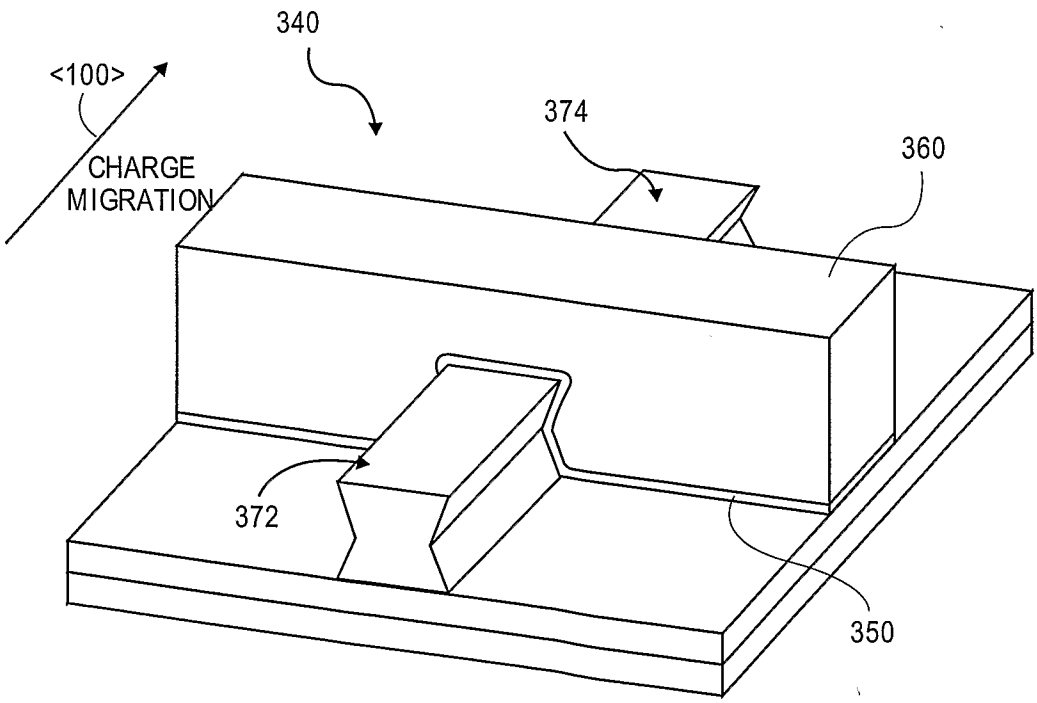
β
319

FIG. 3C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372
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FIG. 3D

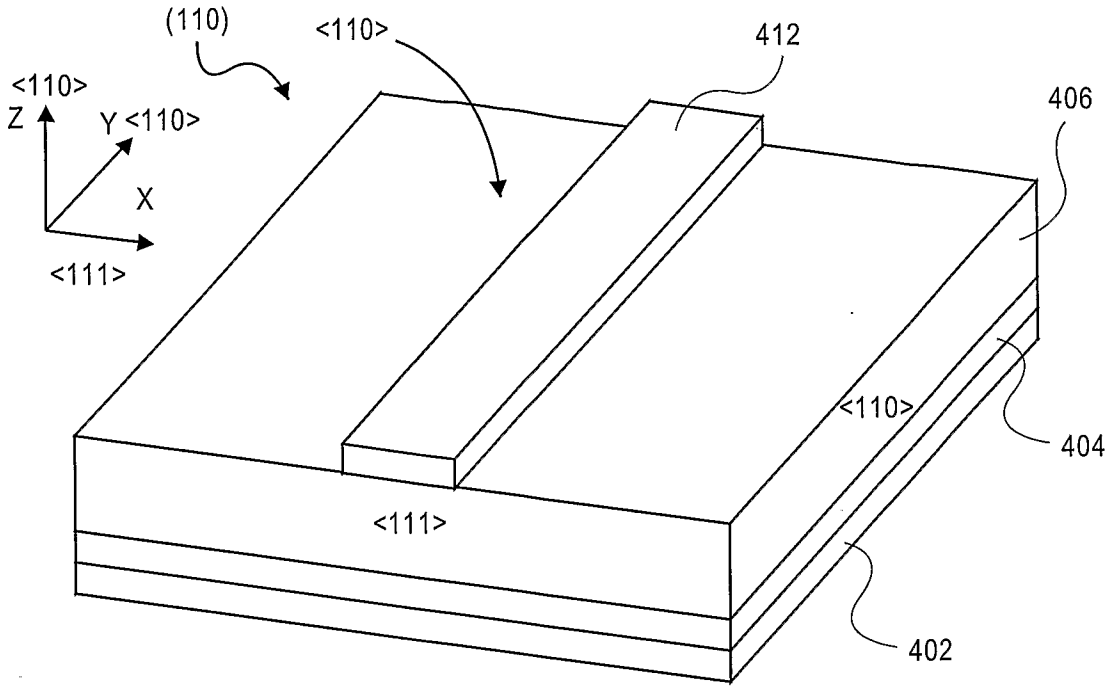
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FIG. 4A

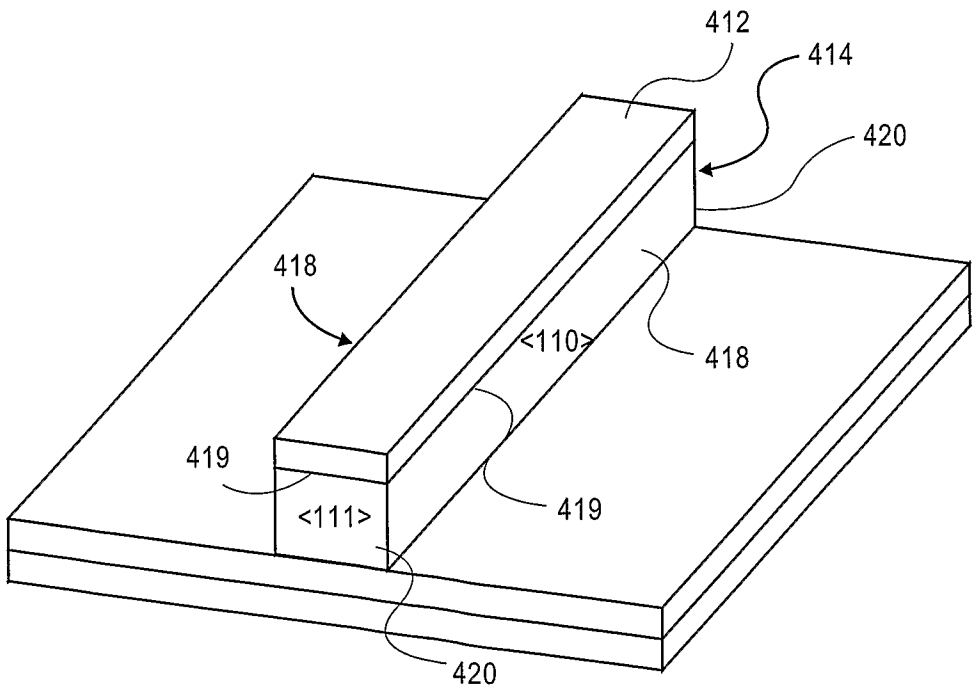
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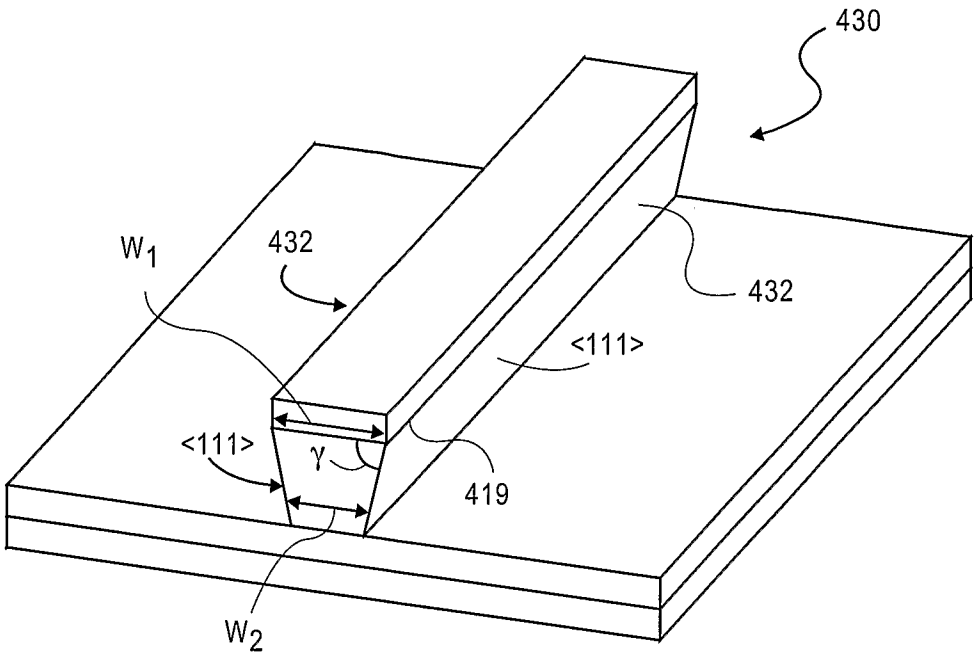
FIG. 4B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W1
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γ
419
W2

FIG. 4C

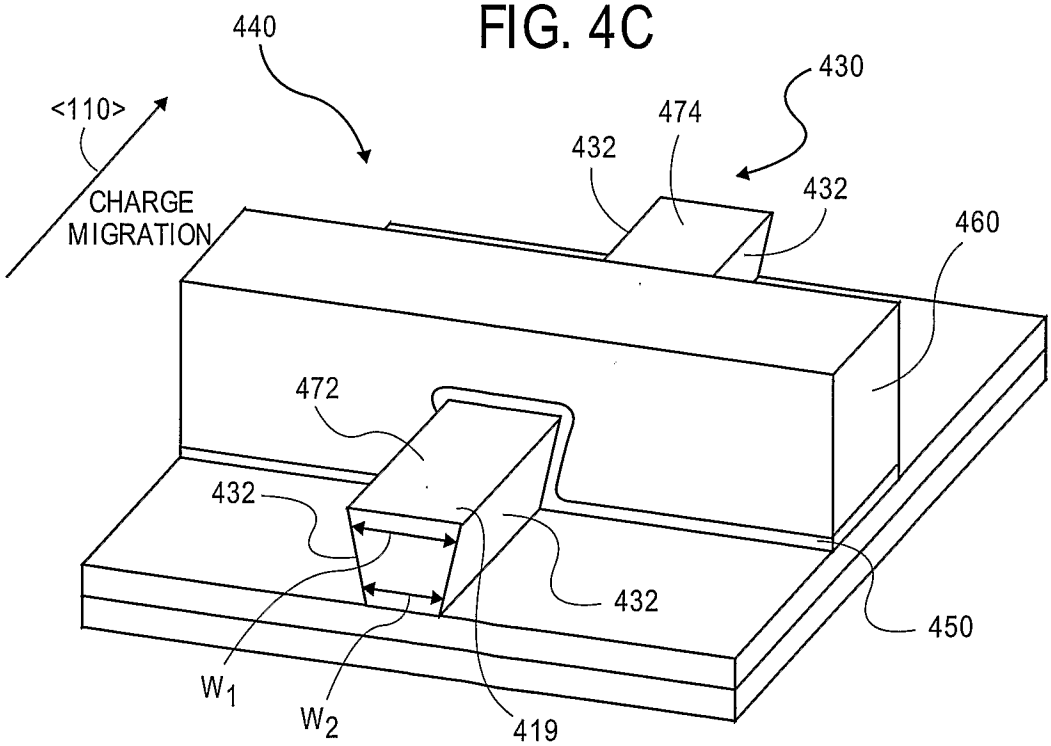
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FIG. 4D

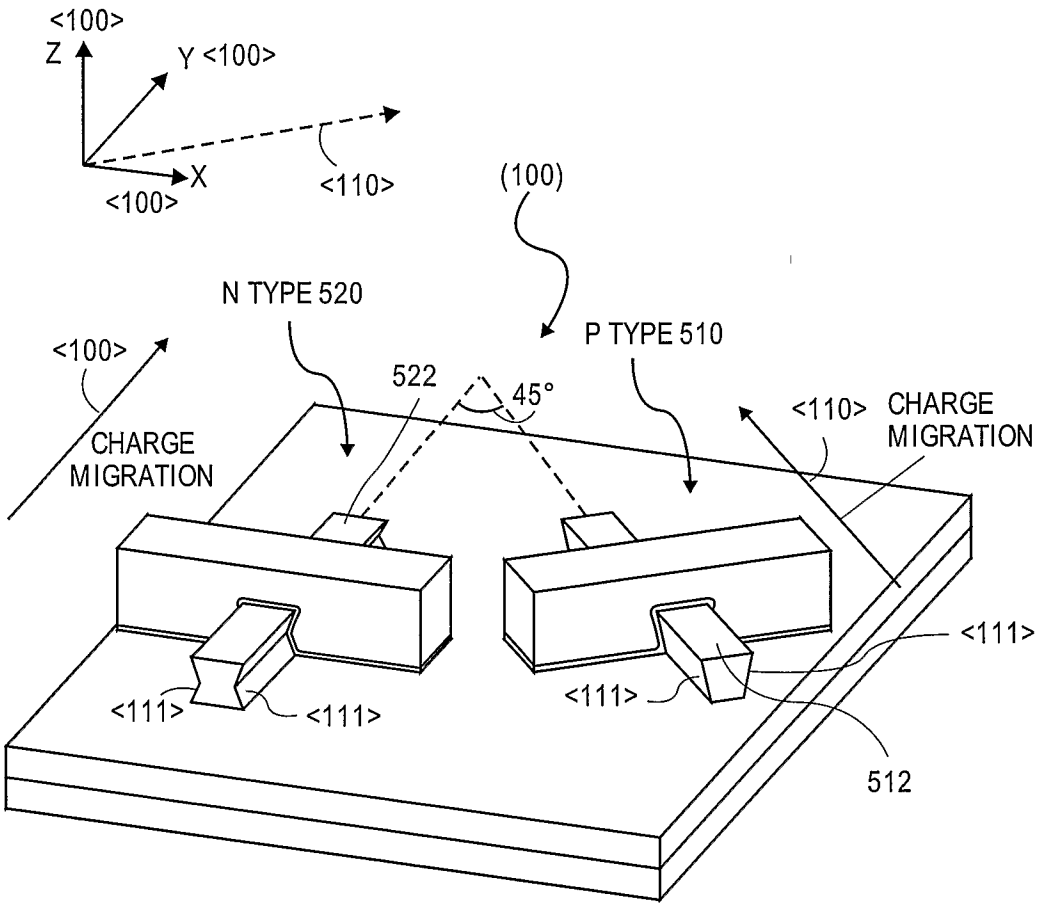
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FIG. 5