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(54) **RACETRACK MEMORY WITH
ELECTRIC-FIELD ASSISTED DOMAIN WALL
INJECTION FOR LOW-POWER WRITE
OPERATION**

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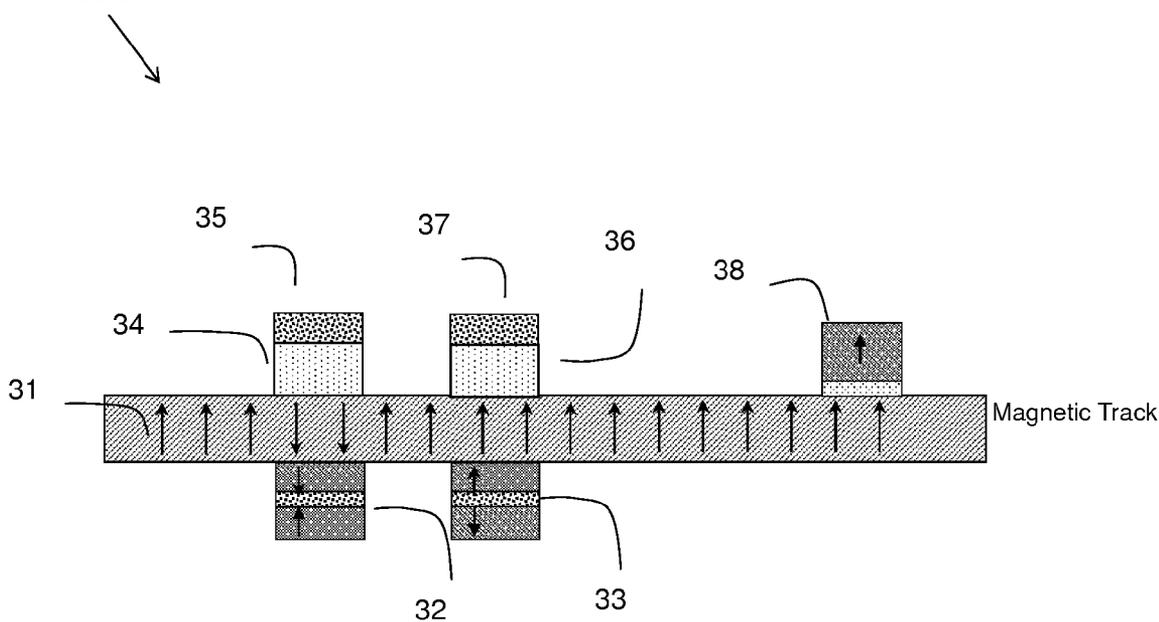
(57) **ABSTRACT**

Embodiments are directed to injecting domain walls in a magnetic racetrack memory. In some embodiments, a race-track comprising a nanowire is coupled with a gate in order to manipulate an anisotropy associated with the nanowire. The racetrack and gate is coupled with a pinning layer configured to establish a magnetization direction in the nanowire.

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300



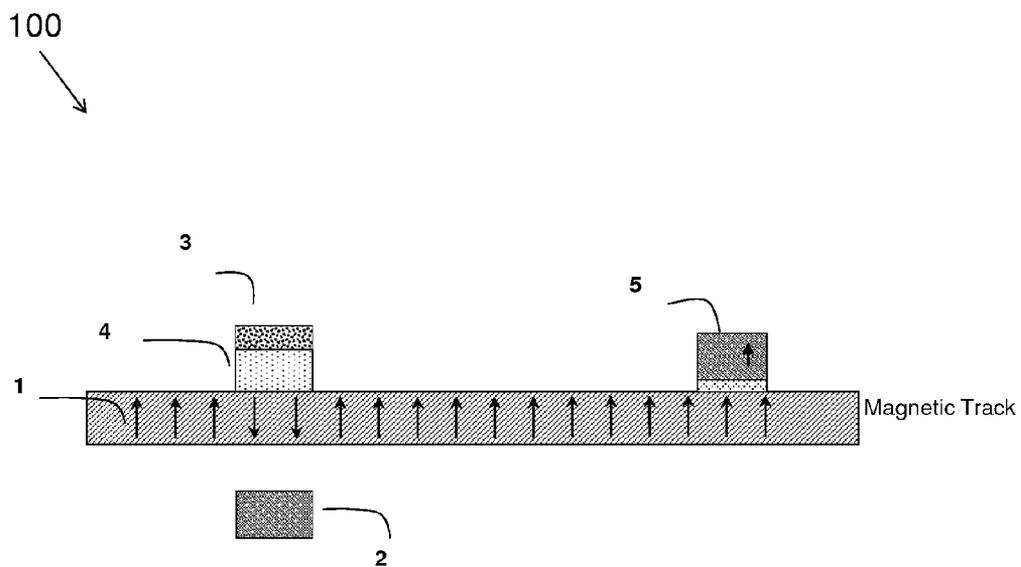


FIG. 1

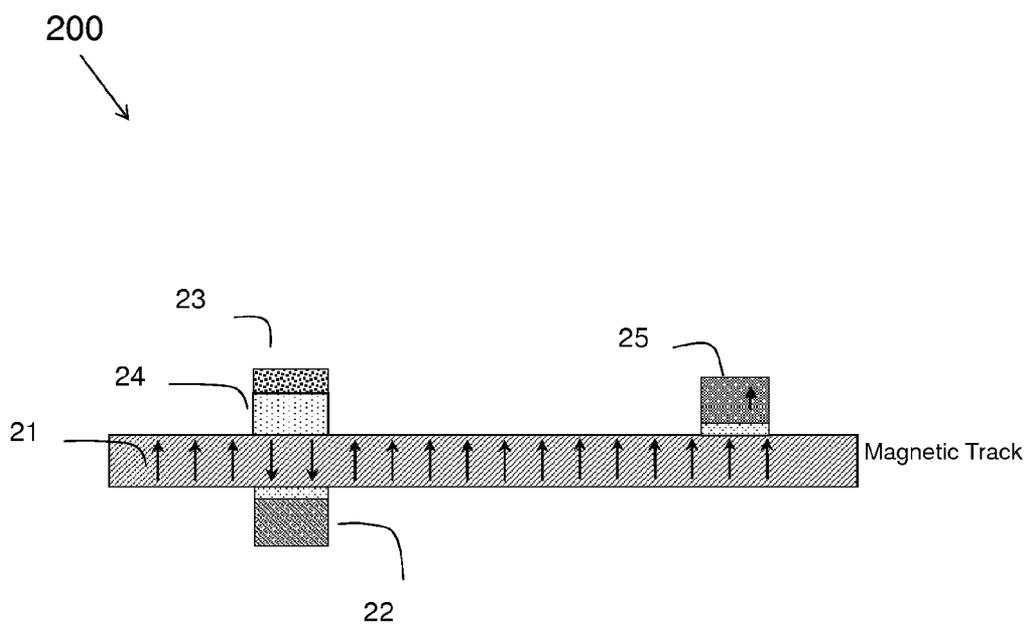


FIG. 2

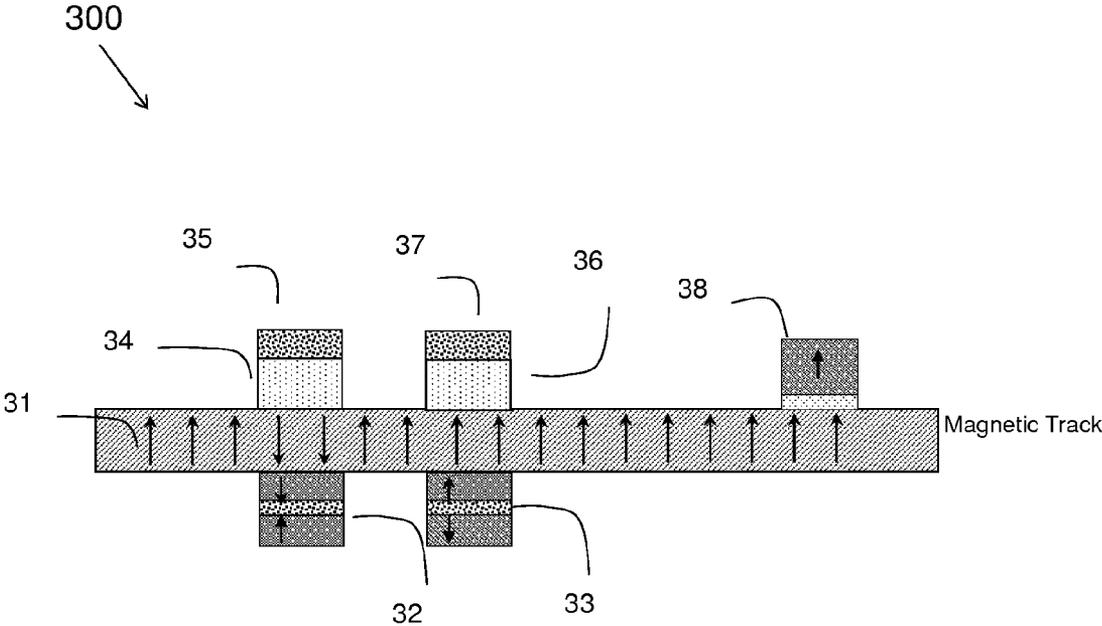


FIG. 3

400
↘

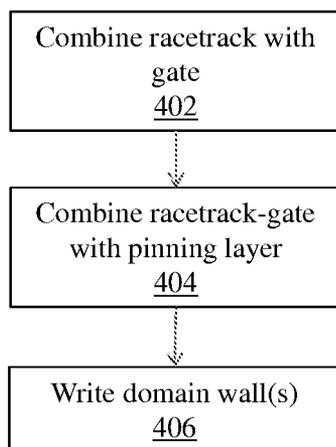


FIG. 4

**RACETRACK MEMORY WITH
ELECTRIC-FIELD ASSISTED DOMAIN WALL
INJECTION FOR LOW-POWER WRITE
OPERATION**

CROSS-REFERENCE TO RELATED
APPLICATION

[0001] This application is a continuation of U.S. patent application Ser. No. 13/835,254, filed Mar. 15, 2013, the disclosure of which is incorporated by reference herein in its entirety.

FIELD OF INVENTION

[0002] The present invention relates generally to computer memory technology, and more specifically, to an injection of a domain wall in a magnetic shift register memory.

DESCRIPTION OF RELATED ART

[0003] Magnetic shift register memories may make use of magnetic domains for purposes of storing data. Magnetic shift register memories require the injection of a domain wall along the length of a wire (e.g., a racetrack wire). Domain walls can be injected in a magnetic stripe via a local magnetic field at a location along the racetrack wire, or via current-induced spin-torque switching with a current injected from a reference layer via a metallic or insulating spacer at various locations along the wire. Both of these methods typically require large current densities and therefore are prone to large power dissipations.

BRIEF SUMMARY

[0004] Embodiments are directed to a method for injecting domain walls in a magnetic racetrack memory comprising: coupling a racetrack comprising a nanowire with a gate in order to manipulate an anisotropy associated with the nanowire, and coupling the racetrack and gate with a pinning layer configured to establish a magnetization direction in the nanowire.

[0005] Embodiments are directed to a magnetic domain wall shift register memory comprising: a magnetic nanowire, a dielectric layer configured to provide a surface anisotropy contribution to the nanowire, at least one antiferromagnet configured to induce an exchange bias locally on the nanowire, and a tunnel junction configured to provide a readout of a magnetic domain.

[0006] Embodiments are directed to a computer program product for injecting domain walls in a magnetic racetrack memory, the computer program product comprising a non-transitory computer readable storage medium having program code embodied therewith, the program code executable by a device to: couple a racetrack comprising a nanowire with a gate in order to manipulate an anisotropy associated with the nanowire, and couple the racetrack and gate with a pinning layer configured to establish a magnetization direction in the nanowire.

[0007] Additional features and advantages are realized through the techniques described herein. Other embodiments and aspects are described in detail herein. For a better understanding, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL
VIEWS OF THE DRAWINGS

[0008] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features and advantages are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 is a schematic diagram for an exemplary magnetic domain wall shift register memory device;

[0010] FIG. 2 is a schematic diagram for an exemplary magnetic domain wall shift register memory device;

[0011] FIG. 3 is a schematic diagram for an exemplary magnetic domain wall shift register memory device; and

[0012] FIG. 4 is a flow chart of an exemplary method of forming a magnetic domain wall shift register memory device, in accordance with another embodiment.

DETAILED DESCRIPTION

[0013] It is noted that various connections are set forth between elements in the following description and in the drawings (the contents of which are included herein by way of reference). It is noted that these connections in general and, unless specified otherwise, may be direct or indirect and that this specification is not intended to be limiting in this respect. In this regard, a coupling of entities may refer to either a direct or an indirect connection.

[0014] Methods, apparatuses, and systems are described for injecting domain walls in a magnetic racetrack memory. The memory may comprise a magnetic domain wall shift register. The injection of the domain wall may be based on an electrical control of surface anisotropy at one or more ferromagnetic metal/dielectric interfaces. Power dissipation may be minimized using one or more techniques described herein. In some embodiments, local anisotropy in a nanowire may be modulated via an electric field. Use of the electric field for write operations may reduce a write coercive field threshold when combined with an Oersted field, or the critical current when combined with a spin torque write technique.

[0015] Referring to FIG. 1, a schematic diagram is shown for an exemplary magnetic domain wall shift register memory device 100. The device 100 is shown in FIG. 1 as including a magnetic nanowire 1. The nanowire 1 may correspond to a ferromagnetic material. In some embodiments, the nanowire 1 may be composed of one or more materials or elements, such as for example cobalt, iron, etc.

[0016] Domain wall motion may be induced via, e.g., imposition of a charge current across the length of the nanowire 1 and/or driving a current through the nanowire. The device 100 may include a write line for the generation of an Oersted field, in order to write a magnetic domain.

[0017] The device 100 may include a nonmagnetic metal top electrode 3 and a dielectric layer 4 in contact with the nanowire 1. In some embodiments, the dielectric layer may have a thickness of approximately 1-10 nanometers. Application of an electric field across the combination of the nanowire 1, the dielectric layer 4, and the electrode 3 may change a carrier concentration, which in turn may contribute to the surface anisotropy of the nanowire 1.

[0018] The surface anisotropy contribution may be modulated by applying a bias between the nanowire 1 and the nonmagnetic top electrode 3, thereby modulating the threshold switching field, and hence the threshold current in an

Oersted write element **2**. The element **2** may be a copper wire carrying an electrical current, which generates an Oersted field. The direction and strength of the Oersted field can be adjusted by varying the sign and the amplitude of the current in portion **2**. The element **2** can provide for a preferred magnetization direction with respect to the nanowire **1** when the element **2** is adjacent to the nanowire **1**.

[0019] A tunnel junction **5** may be placed at different locations along the nanowire **1** and may be used to read out the magnetic state of the nanowire **1**. Such a magnetic tunnel junction may be comprised of a dielectric layer used as a barrier (in the 0.5 nm-3 nm thickness range) such as Al₂O₃, HfO₂, TiO₂, and MgO and a fixed layer or reference layer comprised of a ferromagnetic layer with an antiferromagnetic pinning layer such as FeMn or IrMn or a synthetic antiferromagnet, the free layer of the magnetic tunnel junction is comprised of portion **1** namely the ferromagnetic nanowire. A synthetic antiferromagnet used as a reference layer in the magnetic tunnel junction may be comprised of two ferromagnetic layers each comprised of Co/Pt or Co/Ni multilayers coupled antiferromagnetically via a thin Ru or Ir spacer. The magnetic domains may be moved within the nanowire **1** via application of a current in the nanowire **1**.

[0020] Turning now to FIG. **2**, a schematic diagram is shown for an exemplary magnetic domain wall shift register memory device **200**. The device **200** is shown in FIG. **2** as including a magnetic nanowire **21**. Domain wall motion may be induced via, e.g., imposition of a charge current across or electrical current through the length of the nanowire **21**. A tunnel junction from which a spin polarized-current is injected from a magnetic electrode to the nanowire **21** may be used so as to induce current-induced spin torque transfer switching in the nanowire **21** for the generation of a magnetic domain **22**. The device **200** may include a nonmagnetic metal top electrode **23** and a dielectric layer **24** in contact with the nanowire **21** contributing to the surface anisotropy of the nanowire **21**. The surface anisotropy contribution may be modulated by applying a bias between the nanowire **21** and the nonmagnetic top electrode **23**, thereby modulating the threshold switching currents necessary to induce a magnetic domain wall via spin torque switching from the magnetic tunnel junction **22**. A tunnel junction may be placed at different locations along the nanowire **21** and may be used to read out the magnetic state **25** of the nanowire **21**.

[0021] Turning now to FIG. **3**, a schematic diagram is shown for an exemplary magnetic domain wall shift register memory device **300**. The device **300** may correspond to a variation on the device **100**. The device **300** may include a magnetic nanowire racetrack **31**, two magnetic structures comprising a metallic antiferromagnetic layer and/or a synthetic antiferromagnet **32** and **33** placed along the nanowire **31**, non-magnetic metal structures **34** and **36** and dielectric structures **35** and **37** forming a gate, and a magnetic tunnel junction **38** for readout. The synthetic antiferromagnet may be comprised of two ferromagnetic layers each comprised of Co/Pt or Co/Ni multilayers coupled antiferromagnetically via a thin Ru or Ir spacer. The gate may be in direct contact with the nanowire **31** and adjacent to structures **32** and **33**. The structures **32** and **33** may be set so that their respective interfaces with the nanowire **31** are magnetized towards opposite directions. The gates (**34**, **35** and **36**, **37**) along with structures **32** and **33** may provide an electrical control of the magnetic state of the nanowire **31** with a first gate (e.g., **34**, **35**) allowing a write operation by setting the magnetization for the nanowire

31 in a first direction and a second gate (e.g., **36**, **37**) being used for erase operations by setting the nanowire **31** magnetization in a second direction (e.g., in a direction opposite to the first direction). The interface of the antiferromagnetic element/structures **32** and **33** with the nanowire **31** may be optimized so as to have a coercive field of the nanowire **31** larger than an offset field due to exchange coupling. By applying an electric field to a metal dielectric structure (e.g., **35** and/or **37**) a change the carrier concentration at the metal dielectric interface may be induced. The local surface anisotropy of the nanowire **31** may be modulated by the same technique and a variation of the coercive field of the nanowire **31** along a direction aligned with the direction of the local anisotropy, which may be aligned or perpendicular with an axis of the nanowire **31**, may be obtained.

[0022] Turning now to FIG. **4**, a flow chart of an exemplary method **400** in accordance with one or more embodiments is shown. The method **400** may be used to fabricate and use one or more devices, such as the devices **100**, **200**, and **300** described herein.

[0023] In block **402**, a racetrack may be combined with a gate. The combination of the racetrack and gate may be used to manipulate or control a surface anisotropy.

[0024] In block **404**, the racetrack-gate combination may be combined with a pinning layer (e.g., element **2** of FIG. **1**). The pinning layer may be used to establish a magnetization direction with respect to a nanowire associated with the racetrack.

[0025] In block **406**, one or more domain walls may be written. For example, such writing may occur via the use of an applied electric field in combination with a spin torque element or an Oersted field.

[0026] The method **400** is illustrative. In some embodiments, one or more of the blocks (or portions thereof) may be optional. In some embodiments, one or more blocks or operations not shown may be included. In some embodiments, the blocks or operations may execute in an order or sequence different from what is shown in FIG. **4**.

[0027] In some embodiments, various functions or acts may take place at a given location and/or in connection with the operation of one or more apparatuses or systems. In some embodiments, a portion of a given function or act may be performed at a first device or location, and the remainder of the function or act may be performed at one or more additional devices or locations.

[0028] As will be appreciated by one skilled in the art, embodiments may be implemented as a system, method or computer program product. Accordingly, embodiments may take the form of an entirely hardware embodiment, an entirely software embodiment (including firmware, resident software, micro-code, etc.) or an embodiment combining software and hardware aspects that may all generally be referred to herein as a "circuit," "module" or "system." Furthermore, embodiments may take the form of a computer program product embodied in one or more computer readable medium(s) having computer readable program code embodied thereon.

[0029] Any combination of one or more computer readable medium(s) may be utilized, such as one or more non-transitory computer readable mediums. The computer readable medium may be a computer readable storage medium. A computer readable storage medium may be, for example, but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any suitable combination of the foregoing. More

specific example (a non-exhaustive list) of the computer readable storage medium would include the following: an electrical connection having one or more wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), an optical fiber, a portable compact disc read-only memory (CD-ROM), an optical storage device, a magnetic storage device, or any suitable combination of the foregoing. In the context of this document, a computer readable storage medium may be any tangible medium that can contain, or store a program for use by or in connection with an instruction execution system, apparatus, or device.

[0030] Program code embodied on a computer readable medium may be transmitted using any appropriate medium, including but not limited to wireless, wireline, optical fiber cable, RF, etc., or any suitable combination of the foregoing.

[0031] Computer program code for carrying out operations may be written in any combination of one or more programming languages, including an object oriented programming language such as Java, Smalltalk, C++ or the like and conventional procedural programming languages, such as the "C" programming language or similar programming languages. The program code may execute entirely on the user's computer, partly on the user's computer, as a stand-alone software package, partly on the user's computer and partly on a remote computer or entirely on the remote computer or server. In the latter scenario, the remote computer may be connected to the user's computer through any type of network, including a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider).

[0032] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, element components, and/or groups thereof.

[0033] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other

claimed elements as specifically claimed. The present disclosure has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the disclosure. The embodiments were chosen and described in order to best explain the principles of the disclosure and the practical application, and to enable others of ordinary skill in the art to understand the disclosure for various embodiments with various modifications as are suited to the particular use contemplated.

[0034] The diagrams depicted herein are illustrative. There may be many variations to the diagram or the steps (or operations) described therein without departing from the spirit of the disclosure. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the disclosure.

[0035] It will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow.

What is claimed is:

- 1. A magnetic domain wall shift register memory comprising:
 - a magnetic nanowire;
 - a dielectric layer configured to provide a surface anisotropy contribution to the nanowire;
 - at least one antiferromagnet configured to induce an exchange bias locally on the nanowire; and
 - a tunnel junction configured to provide a readout of a magnetic domain.
- 2. The memory of claim 1, wherein the at least one antiferromagnet comprises a synthetic antiferromagnet.
- 3. The memory of claim 1, further comprising:
 - metal contacts configured to contact both ends of the nanowire to shift magnetic domains laterally.
- 4. The memory of claim 1, wherein an electric field is applied across the nanowire and the dielectric to write the magnetic domain.
- 5. The memory of claim 4, wherein the magnetic domain is written based on an application of an Oersted field.
- 6. The memory of claim 4, wherein the magnetic domain is written based on an application of a spin torque write technique.
- 7. The memory of claim 1, wherein a current is applied to the nanowire to provide the readout at the tunnel junction.

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