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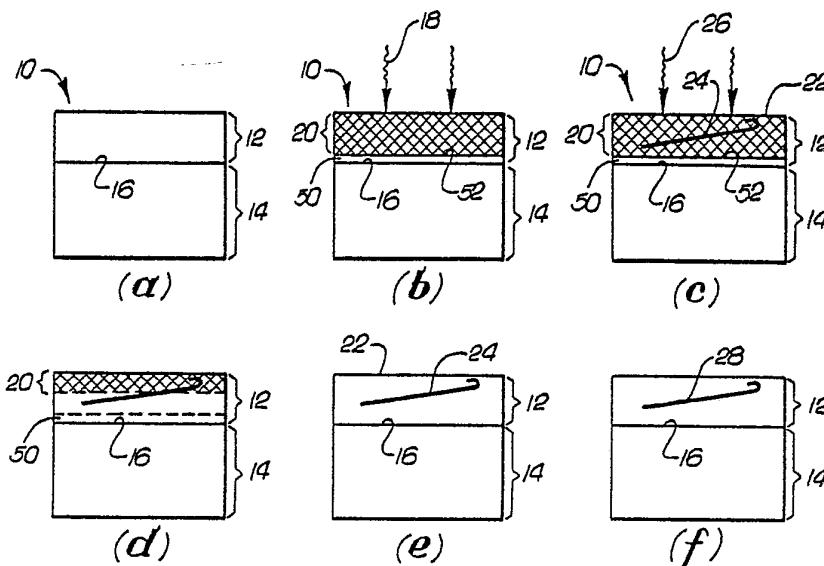
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(54) Title: SEMICONDUCTORS HAVING SHALLOW, HYPERABRUPT DOPED REGIONS, AND PROCESS FOR PREPARATION THEREOF USING ION IMPLANTED IMPURITIES

(57) Abstract

A method for producing hyperabrupt P^{\pm} or N^{\pm} regions (12) in a near-surface layer of a substantially defect free crystal (10), using solid phase epitaxy and transient annealing. The process for producing a hyperabrupt retrograde distribution of the dopant species begins with amorphizing the near-surface layer of a base crystal, and then implanting a steep retrograde distribution of the desired species into the amorphized layer, so that the retrograde distribution lies entirely within the amorphized layer, thereby avoiding channeling effects during implantation. The substantially defect-free structure of the base crystal is restored by annealing the implanted base crystal at a temperature sufficiently high to induce solid phase epitaxial regrowth

on the underlying nonamorphized crystal, but at a temperature sufficiently low to avoid significant diffusion of the implanted species. The implanted species is subsequently activated by a rapid thermal annealing process, at a temperature sufficiently high to activate the implanted species, but for a very short time so that long-range diffusion does not occur. In a preferred embodiment, the implanted species is boron, BF_2^+ , phosphorus, or arsenic in the top 0.20 micrometers of a substantially defect-free silicon base crystal, which may be in a bulk form or epitaxially deposited on an insulator substrate such as sapphire.



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SEMICONDUCTORS HAVING SHALLOW, HYPERABRUPT
DOPED REGIONS, AND PROCESS FOR PREPARATION
THEREOF USING ION IMPLANTED IMPURITIES

1 BACKGROUND OF THE INVENTION

 This invention relates generally to semiconductor
 devices, and, more specifically, to a semiconductor
 device having a very steep retrograde distribution of a
5 rapidly diffusing species in a near-surface layer of a
 substantially perfect base crystal.

 The proper operation of miniature electronic
 devices often depends significantly upon the ability to
 fabricate specialized forms of dopant layers within
10 crystals. As an example, the fabrication of submicro-
 meter CMOS integrated circuits using either bulk silicon
 or silicon-on-sapphire (SOS) substrates requires the
 fabrication of properly scaled submicrometer n- and p-
 channel MOS Field Effect Transistors (MOSFETs) with
15 ultralow source and drain resistances, and minimal
 short channel behavior. The fabrication of such MOSFETs
 in turn necessitates the fabrication of dopant layers
 with high junction gradients, shallow junction depths,
 and ultralow sheet resistances.

1 The formation of P^+ and N^+ doped source and drain
regions requires the formation of shallow, hyperabrupt
distributions of ions such as boron, phosphorus, or
5 In particular, the junctions of doped regions should lie
within less than about 0.2 micrometers of the surface
of the silicon crystal, and should include a retrograde
junction having a gradient on the order of the solubility
of the dopant species over a small distance, preferably
10 about 0.01 micrometers. Further, when fabrication of
the device is complete, the sheet resistance of the
doped junction layer should be less than about 100 ohms
per square, in turn requiring that the silicon base
crystal be substantially free of defects and that the
15 dopants be fully activated.

 The fabrication of shallow junctions having steep
concentration gradients, together with the requirement
of low sheet resistance, poses difficult fabrication
problems, so that such junctions have heretofore been
20 impossible to prepare. In typical prior approaches,
the dopant species was implanted into the surface of the
silicon crystal under known and controlled conditions
in an attempt to achieve the desired steep retrograde
distribution, but the implanted crystal was then be
25 heated to elevated temperature to activate the implanted
species and also to anneal the damage introduced by the
implantation procedure, inasmuch as such damage increases
the sheet resistance of the final device. This annealing
procedure causes diffusion of the implanted species,
30 which acts to reduce the steepness of the concentration
gradient at the junction, and to cause migration of the
junction to deeper depths within the crystal. Moreover,
the implantation procedure and the annealing step can

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1 result in channelling of the implanted species, so that
"tails" of high concentrations of the implanted species
can be found along particular crystallographic directions
in the base crystal following these procedures.

5 Channelling effects tend to destroy the uniformity of
the junction, also reducing the gradient and migrating
the junction to deeper depths within the crystal.

Thus, in prior attempts to produce the necessary
shallow junctions with steep concentration gradients, in
10 a crystal having a low sheet resistance, the dopant
ions were first implanted and then the crystal was
annealed at a temperature of about 900-950°C for about
30-60 minutes. Although the implantation procedure
produces the desired dopant distribution to a first
15 approximation, the distribution is imperfect because of
the channelling tails and broadening due to the subsequent
annealing procedure, as the junction migrates to deeper
depths within the crystal and the sharpness of the
concentration gradient at the junction is reduced.
20 The resulting deep junctions can cause detrimental short
channel behavior in submicrometer n- and p- channel
MOSFETs. The annealing procedure which causes the
modification of the junction cannot be omitted, because
the annealing process is required to activate the
25 implanted species and to reduce the defect density in
the base crystal for a sufficiently low sheet resistivity.
For the case of SOS devices, the problem is further
aggravated by the high defect density in the silicon
film, which reduces dopant activation and enhances
30 lateral diffusion under the gate of p-channel MOSFETs.

Thus, the fabricator of devices must reduce the
defect density of the underlying base crystal to achieve
the necessary low resistivities, but the conventional

1 implanting and annealing procedure results in channelling
of the implanted species and also broadening and
deepening of the implanted junction. If the implanted
species did not diffuse within the base crystal, the
5 annealing treatment would not adversely modify the
junction characteristics. Unfortunately, however, the
dopant species of principal interest such as boron,
phosphorus, and arsenic do diffuse rapidly within
silicon base crystals at typical annealing and activation
10 temperatures, and it has not been possible to prepare
the desired junctions by prior procedures.

Thus, there has been proposed no fabrication
procedure for producing hyperabrupt, shallow junctions
of such dopants in base crystals, to yield a device
15 having a low sheet resistivity. Accordingly, there
exists a need for such a fabrication procedure. The
process should allow the preparation of shallow, steep
retrograde junctions of rapidly diffusing dopant species
in base crystals, with the desired junction preserved
20 through a treatment to reduce the defect concentration
of the base crystal so that the sheet resistivity of
the completed device is low. The fabrication procedure
should be compatible with existing technology for
producing microcircuits, and in particular should be
25 compatible with further fabrication steps to add other
components onto the chip. The present invention fulfills
this need, and further provides relates advantages.

SUMMARY OF THE INVENTION

30 The present invention provides a crystal having a
shallow, steep distribution of a rapidly diffusing
species, and a process for its preparation. The
fabricated device exhibits a very low sheet resistivity,

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1 which may be five times lower than the sheet resist-
 ivities obtained by other techniques. Channelling and
 tailing effects during implanting and annealing are
 avoided, thereby preserving the uniformity and steep
5 gradient of the junction. The process is fully
 compatible with existing semiconductor fabrication
 technology, and indeed is less costly because furnace
 annealing times and temperatures are reduced.

 In accordance with the invention, a process for
10 producing a controlled distribution of an activated,
 rapidly diffusing, implanted species within the near-
 surface layer of a base crystal comprises the steps of
 altering the near-surface layer of the base crystal
 from its normal structure to reduce the diffusivity and
15 implant channelling of the implanted species, thereby
 forming a treated layer; implanting the implanted dopant
 species within the treated layer in the desired controlled
 distribution; reverting the base crystal of the treated
 region to its normal crystalline structure; and activating
20 the implanted species, thereby leaving the base crystal
 with the controlled distribution of the implanted
 species in an activated form, and with the base crystal
 substantially free of defects. More specifically, a
 steep retrograde distribution is achieved by amorphizing
25 the near surface layer of the base crystal to produce
 an amorphized layer; implanting a steep retrograde
 distribution to lie substantially entirely within the
 amorphized layer, the step of implanting to occur at a
 temperature of the base crystal whereat the implanted
30 species is essentially diffusionally immobile in the
 amorphized layer; annealing the base crystal at a first
 annealing temperature sufficiently high to achieve

1 solid phase epitaxial growth in the amorphized layer on
the crystalline portion of the base crystal, whereby
the amorphized layer is recrystallized, the first
annealing temperature being sufficiently low that the
5 implanted species is substantially diffusionally immobile
in the recrystallizing layer; and annealing the base
crystal at a second annealing temperature greater than
the first annealing temperature, for a time sufficient
to activate the implanted species but not to permit
10 large scale diffusion of the implanted species.

In a preferred embodiment, the silicon base
crystal is amorphized to a depth of about 0.20 micro-
meters by implanting silicon (Si^+) or germanium (Ge^+)
ions, the base crystal being held at liquid nitrogen
15 temperature. The silicon ions are implanted in a two-
step process, first at an energy of about 100KeV with a
dose of 2×10^{15} ions per square centimeter, and,
second, at an energy of about 55 KeV with a dose of
about 2×10^{15} ions per square centimeter. The dose
20 current in each case is held below 0.2 microamps per
square centimeter to prevent substrate heating.
(Corresponding implantation values for germanium ions
are, first, an energy of about 350 KeV with a dose of
 2×10^{15} ions per square centimeter, and, second, an
25 energy of about 100 KeV with a dose of about 2×10^{15}
ions per square centimeter.) Boron, BF_2^+ , phosphorus,
or arsenic is then implanted under conditions such that
the dopant retrograde distribution profile lies entirely
within the amorphized layer, or below about 0.20
30 micrometers depth. The dosage level of the dopant is
chosen to be close to its solid solubility at 1000°C.
The substrate is held at a temperature low enough to
prevent heating by the ion beam, preferably liquid

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1 nitrogen temperature. The implanted base crystal is
then annealed at a temperature of from about 550°C to
about 650°C, preferably about 600°C for 30 minutes, to
achieve complete solid phase epitaxial growth of the
5 amorphized layer on the underlying crystalline portion
of the base crystal, thereby recrystallizing the
amorphized layer to the low defect density required to
achieve low sheet resistivities. The implanted crystal
is then annealed a second time at a temperature of from
10 about 1000°C to about 1150°C, preferably about 1100°C
for about 1 second, to achieve activation of the
implanted species. During this very brief high
temperature annealing step, the implanted species is
substituted into crystalline lattice sites, but does
15 not have time to diffuse more than about one lattice
spacing. Thus, the two annealing steps result in
restoration of a substantially defect-free base crystal
by recrystallization of the amorphized layer, and
activation of the implanted species, without broadening
20 or migration of the profile of the implanted species at
the junction. The two-step annealing process is
preferably accomplished in a transient annealing system
using a bank of high power tungsten halogen arc lamps
with a quartz diffuser, for producing a uniform intensity
25 of optical radiation that is absorbed by the crystal.

After the annealing steps are complete, the
processed component wafer is cooled down to about 500°C
within the heating apparatus and then is removed and
placed on a cold surface to cool it rapidly but without
30 causing wafer breakage or defect production. The wafer
may then be further processed into device structures.

The present invention also extends to a crystal
or wafer having a hyperabrupt junction therein comprising
a base crystal substantially free of defects; and a

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1 hyperabrupt retrograde distribution of an activated
species contained in a near surface layer of the base
crystal, the layer having a depth of no more than about
0.20 micrometers, the gradient of the retrograde
5 distribution being at least as great as the difference
between the maximum solubility of the species and a
substantially zero level over a distance of less than
about 0.10 micrometers. The preferred base crystal is
silicon, and the preferred activated species are boron,
10 BF_2^+ , phosphorus, or arsenic, all of which are rapidly
diffusing species in silicon at the temperatures required
for their activation in a silicon crystal.

It will now be appreciated that the present
invention represents a significant and important advance
15 in the preparation of microcircuit device structures.
High concentration gradient, hyperabrupt retrograde
junctions can be produced in the near-surface layers of
crystals, from dopant species which are rapidly diffusing
in the base crystal. After the dopant species is placed
20 into a near surface amorphized layer of the base crystal,
in the desired concentration distribution, this
distribution is preserved and a substantially defect-
free base crystal structure is produced by a two step
annealing process, which also activates the dopant
25 species. The resulting wafer has a high gradient, near
surface retrograde distribution of the dopant species
in a substantially defect free, low resistivity base
crystal. The process for producing this structure is
fully compatible with other device fabrication technology,
30 and actually results in lower cost because of the
reduced furnace capacity requirements. Other features
and advantages of the invention will become more apparent
from the following detailed description, taken in
conjunction with the accompanying drawings, which
35 illustrate, by way of example, the principles of the
invention.

1 BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a series of side sectional views of a base crystal illustrating the changes in its structure during processing;

5 FIGURE 2 is a graph illustrating a two step annealing procedure;

FIGURE 3 is a schematic side sectional view of a transient annealing system; and

10 FIGURE 4 is a side sectional view of an integrated circuit structure having self-aligned MOSFET devices, prepared in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

15 In one embodiment prepared in accordance with the present invention, a silicon on sapphire wafer 10 such as shown in FIGURE 1(a) is used as the starting point. The silicon on sapphire wafer 10 comprises a silicon layer 12 epitaxially deposited on the surface of a sapphire substrate 14. Procedures for preparing such a wafer 10 are known in the art. See U.S. Patent Nos. 20 3,508,962 and 3,546,036, whose disclosures are herein incorporated by reference. Briefly, the sapphire substrate 14 is preferably on the order of about 0.25-0.40 millimeters in thickness and has a surface 25 crystallographic orientation of within about 1 degree of ($\bar{1}102$) (hexagonal Miller indices notation). This crystallographic orientation of the sapphire substrate 14 is necessary for the subsequent epitaxial growth of the silicon layer 12 having a preferred crystallographic 30 orientation of (100) (cubic Miller indices notation).

The silicon layer 12 is deposited on the surface of the sapphire substrate 14, preferably by chemical vapor deposition. The chemical vapor deposition of the

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1 epitaxial silicon layer 12 is preferably performed by
the chemical decomposition of silane (SiH_4) in
an appropriate reactor at approximately 910°C . In the
preferred embodiment, the epitaxial growth is performed
5 to achieve a silicon epitaxial layer 12 having a maximum
thickness of about 0.25 micrometers with a growth rate
range of from 0.3 to about 2.4 micrometers per minute,
preferably 2.4 micrometers per minute. This preferred
growth rate minimizes the defect density in the silicon
10 layer 12 at a silicon-sapphire interface 16. Such
wafers 10 may be obtained commercially from the Crystal
Products Division of Union Carbide, Inc., 8888 Balboa
Avenue, San Diego, California 92123.

The silicon on sapphire wafer 10 is utilized
15 herein as the starting material for a preferred embodiment
of the present invention, with the silicon layer 12
serving as the base crystal for preparation of the
doped junction prepared in accordance with the invention.
However, the present invention is more broadly applicable
20 to preparation of a wide variety of doped junctions in
base crystals, such as, for example, bulk silicon,
gallium arsenide, silicon on alpha-aluminum oxide (as
disclosed in U.S. Patent No. 3,393,088), silicon on
spinel insulators (as disclosed in U.S. Patent No.
25 3,414,434), silicon on chrysoberyl (as disclosed in
U.S. Patent No. 3,475,209), and IIb-VIa and III-V
semiconductor compounds on insulator substrates (as
disclosed in U.S. Patent No. 3,664,866), all of the
disclosures of the listed patents being incorporated
30 herein by reference. Moreover, the base crystal need
not be pure, but may be a compound or previously doped
with other species. However, to achieve the preferred
embodiment having minimum resistivity, the base crystal

1 is preferably of very high purity. Nonetheless, the principles of the present invention are applicable to impure base crystals to achieve desired dopant profile concentrations therein.

5 In accordance with the present invention, the base crystal, herein the silicon layer 12, is first treated by amorphizing to modify its normal crystalline structure to an amorphous structure, which reduces the diffusivity and implant channelling of a subsequently
10 implanted species. Referring to FIGURE 1(b), amorphizing is accomplished by implanting ions 18, preferably Si^+ or Ge^+ ions, into the wafer 10 to amorphize the silicon layer 12. Where the wafer 10 is the illustrated SOS material, the amorphizing implantation may be conducted
15 at ambient or lower temperatures, but the amorphizing implantation should be conducted at reduced temperatures such as liquid nitrogen temperature when bulk silicon is used. The amorphizing ion implantation is preferably conducted in two steps involving two different sets of
20 implantation conditions. For Si^+ , in the first step the preferred implantation energy is about 100 KeV with a dose of about 2×10^{15} ions per square centimeter, and, in the second step, the preferred implantation energy is about 55 KeV with a dose of about 2×10^{15}
25 ions per square centimeter. For Ge^+ , in the first step the preferred implantation energy is about 350 KeV with a dose of 2×10^{15} ions per square centimeter, and, in the second step, the preferred implantation energy is about 100 KeV with a dose of about 2×10^{15} ions per
30 square centimeter. For both species, the dosage current is maintained below about 0.2 microamps per square centimeter, also chosen to prevent substrate heating, which could prematurely anneal the amorphized layer.

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1 Amorphization under these conditions for a time of
about 60 minutes produces an amorphized layer 20 having
a depth of about 0.20 micrometers. Thus, in this
preferred embodiment the depth of the amorphized layer
5 20 is somewhat less than the thickness of the silicon
layer 12, but the amorphized layer 20 could be of
substantially equal thickness to that of the silicon
layer 12. If the amorphization is conducted on a bulk
silicon crystal, there is no substrate of different
10 composition, and the implantation depth may be chosen
as any convenient value.

In performing the amorphization, it is strongly
preferred that the implantation energy and ion dose be
sufficiently low so as not to exceed the damage density
15 threshold of the sapphire substrate 14. If this
threshold were exceeded during formation of the amorphous
layer 20, the portion of the sapphire substrate 14
adjacent the interface 16 may become damaged. Such
damage is believed to produce a mobile species containing
20 aluminum in the sapphire substrate 14, which can later
diffuse as a contaminant into and throughout the silicon
layer 12 during annealing treatments, with the result
that the resistivity of the completed device is
substantially increased. The implantation conditions
25 stated previously are sufficient to avoid damage to the
near-interface region of the sapphire substrate 14.
Where the starting material is pure bulk silicon, this
problem area does not arise. For other composite
starting materials, such as those mentioned previously,
30 the same principle of avoiding damage to the underlying
substrate is to be applied to avoid possible contamination
of the amorphized base crystal.

Next, a desired dopant species 26 is implanted
into the amorphized layer 20 in the desired distribution,
35 using implantation conditions which prevent modification
of the amorphized layer 20. In the preferred embodiment,

1 the desired distribution is a steep retrograde distribution of the implanted dopant species, the term
"retrograde distribution" indicating that the concentration of the dopant species near the interface 16 is
5 less than the concentration nearer to the base crystal surface 22. A retrograde distribution is illustrated by the retrograde distribution curve 24 in FIGURE 1(c). It is important that the desired distribution be
10 implanted entirely within the amorphized layer 20, to avoid channeling and so that the characteristics of the distribution are preserved through the later processing steps.

In this preferred embodiment, the dopant species 26 is preferably selected from the group consisting of
15 boron, BF_2^+ , phosphorus, and arsenic. Techniques for implanting such species are known in the art. When implanted under the conditions indicated below, the peak of the distribution 24 is within about .005 to about .010 micrometers of the crystal surface 22, and
20 the maximum concentration of dopant species can be near the limit of solid solubility. For implanted boron, for example, the implanted concentration is about 3 to 5×10^{20} atoms per cubic centimeter, with the concentration falling to the range of about 10^{16} to about 10^{17}
25 atoms per cubic centimeter over a distance of about .020 micrometers further into the crystal base from the peak. In the preferred embodiment, it is desired that the gradient or slope of the retrograde distribution 24 be as great as possible, and therefore the maximum
30 dopant concentration is chosen to be close to the maximum solubility of the dopant species in the base crystal at a second annealing temperature, whose selection will be described in more detail below. The following table presents the preferred implantation
35 conditions for each of the preferred dopant species.

1	<u>Ions</u>	<u>Implantation Energy in KeV</u>	<u>Dose In Ions Per Square Centimeter</u>
	Boron	10	$2-4 \times 10^{15}$
	BF_2^+	45	$2-4 \times 10^{15}$
5	Phosphorus	55	$2-4 \times 10^{15}$
	Arsenic	100	$2-4 \times 10^{15}$

10 Dose current to be less than about 0.2 microamps per square centimeter.

As indicated previously, it is important that the entire dopant distribution 24 be contained within the amorphized layer 20. In typical ion implantation treatments into a nonamorphized, crystalline layer, the implanted species is channelled along particular crystallographic orientations of the base crystal to produce "tails" along the channelled crystallographic directions. The tails produce spikes or protrusions from the distribution into deeper layers of the base crystal, so that the front of the distribution 24 becomes irregular along the channelled crystallographic directions. This irregularity is highly undesirable in producing a sharp demarcation at the junction interface along the distribution 24. By contrast, an amorphized layer does not contain preferred crystallographic orientations or direction to allow channelling of the implanted species during implantation, and therefore the spacial uniformity and sharp front of the distribution 24 are maintained. Although thermally activated diffusion of the implanted species is greater in an amorphized layer than in a crystalline layer at any particular temperature, during implantation the wafer 10 is held at liquid nitrogen temperatures to

1 avoid the possibility of substantial thermally activated
diffusion. Thus, properly performed implantation of
the dopant species 26 into an amorphized base crystal 20
at low temperatures results in a sharply defined
5 distribution, in this case the retrograde distribution 24.

Next, it is necessary to restore the crystallinity
of the amorphized layer 20 and to activate the implanted
species 26. The electrical resistivity of the amorphized
layer 20 is much greater than that of the same layer
10 when in a crystalline form, such as the initially
deposited epitaxial silicon layer 12. As illustrated
in FIGURES 1(d) and 1(e), the amorphized layer 20 may be
recrystallized back to epitaxial, fully crystalline
layer 12 by annealing the wafer 10. Annealing is
15 accomplished by heating the wafer 10 to a temperature
sufficiently high to achieve solid state epitaxial
growth in the amorphized layer 20 on the crystalline
portion of the underlying base crystal. As used herein,
the term "crystalline portion of the base crystal"
20 may refer to epitaxial growth on a non-amorphised,
crystalline portion of the silicon layer 12, or it may
refer to epitaxial growth on the underlying sapphire
substrate 14. In the embodiment described herein,
because only the near surface region 20 of the silicon
25 layer 12 was amorphized, the epitaxial recrystallization
of the amorphized layer 20 occurs on the underlying
nonamorphized crystalline silicon layer 50, and
constitutes upward epitaxial growth from an interface
52 between the amorphized layer 20 and the crystalline
30 silicon layer 50. FIGURE 1(d) illustrates the annealing
operation at an intermediate stage, wherein the
recrystallization has initiated at the interface 52
and moved toward the surface 22 through the amorphized
layer 20. As the recrystallization progresses, the
35 amorphized layer 20 is consumed and converted to its
crystalline form 12, leaving the silicon layer 50 and

1 the sapphire substrate 14 unchanged. Upon completion
of this recrystallization annealing treatment as
illustrated in FIGURE 1(e), the wafer 10 is again fully
crystalline, having the sapphire substrate 14, the
5 substantially defect free silicon epitaxial layer 12,
and the retrograde distribution 24 of implanted dopant
species lying within the substantially defect free
silicon epitaxial layer 12.

The first annealing temperature used in this
10 recrystallization annealing step is chosen to be
sufficiently high to recrystallize the amorphous region
20, but sufficiently low so that the implanted species
26 is substantially immobile by thermally activated
diffusion in both the amorphized layer 20 and the
15 silicon layer 12. Since the preferred dopant species
26 are generally rapidly diffusing in the amorphous
layer 20 and the silicon layer 12, it is important that
this first annealing temperature not be set at too high
a level. It has been found that this first annealing
20 temperature is preferably from about 550°C to about
650°C, most preferably 600°C for a period of time of
about 30 minutes.

The implanted species is then electrically
activated by annealing the base crystal at a second
25 annealing temperature greater than the first annealing
temperature and sufficiently high to cause electrical
activation of the implanted dopant species. When the
dopant species is implanted, the ions come to rest at
random locations in relation to the silicon atoms in the
30 amorphous layer 20. In the first or recrystallization
anneal, the silicon atoms assume a crystallographic
lattice in forming the crystalline silicon layer 12.
However, the implanted dopant atoms remain substantially

1 in their original implanted positions, and thence in a
random, undefined relationship to the lattice points of
the silicon crystal 12. For proper operation of the
subsequently produced device, the implanted dopant
5 species 26 must be substituted onto silicon lattice
points in place of silicon atoms. This substitution is
essentially a thermal diffusional process wherein the
dopant species ions diffuse one atomic lattice spacing
or less. Thus, to achieve electrical activation the
10 implanted species 26 must be thermally activated to a
sufficiently high energy that the atoms can substitu-
tionally jump into the silicon lattice sites.
However, the implanted dopant species 26 must not be
thermally energized so much that it moves substantially
15 more than one atomic lattice spacing, as such larger
scale diffusional movement would alter the desired
retrograde distribution 24 by broadening the distribution
and causing it to migrate to greater depths within the
silicon layer 12.

20 Preferably, activation is achieved by a rapid
transient anneal of the wafer 10 using optical radiation,
to produce an activated distribution 28, as illustrated
in FIGURE 1(f). The activated distribution 28 is
essentially identical with the implanted distribution
25 24 in shape and location within the silicon layer 24,
but the atoms in the distribution 28 may be displaced
by a silicon lattice spacing or less to lie on the
silicon crystal lattice points. Activation is achieved
by heating the wafer 10 to a very high temperature for
30 a very short time by any suitable technique. Preferably,
the selected annealing technique allows the combining of
the first and second annealing steps in a single
apparatus, although the two annealing steps themselves
remain uniquely defined within the apparatus. FIGURE 2
35 illustrates a preferred "waveform" for the annealing

1 process. Although the first annealing and the second
annealing are shown as continuous, they may be made
intermittent and broken into two distinct portions by
an intermittent cooling to a lower temperature, although
5 intermittent cooling is not preferred because of the
possibility of inducing crystal defects into the wafer
10 by the creation of thermal strains.

Annealing is preferably performed by a transient
anneal furnace 30 illustrated in FIGURE 3. The furnace
10 30 consists of two banks of high power arc lamps 32,
such as tungsten, mercury or quartz halogen lamps of
about one kilowatt power level, with a quartz diffuser
34 placed between the arc lamps 32 and a closed chamber
36. The chamber 36 contains a support 38, upon which
15 the wafer 10 rests during the annealing treatment.
Both of the annealing steps may be accomplished in the
furnace 30, with the arc lamps 23 adjusted to a first
power level to achieve the first annealing temperature,
and then quickly readjusted to a second, higher power
20 level for a very short time to achieve the second
annealing step. Both annealing steps are preferably
accomplished in a flowing inert atmosphere such as
argon or nitrogen gas.

For the preferred dopant species 26, the second
25 annealing is preferably accomplished in the range of
about 1000-1150°C, most preferably 1100°C for about 1
second. This very high temperature, very short time
annealing treatment achieves activation of the dopant
species 26, but the time of exposure at the high
30 temperature is not sufficiently great for thermally
activated diffusion to occur over long ranges of more
than about one lattice spacing.

1 The two-step annealing process using optical
radiation of the present invention is to be contrasted
with the single step approach of the prior art. In the
prior approaches, it was attempted to anneal implantation
5 damage from an implanted region at the same time that
the implanted dopant species was electrically activated.
To achieve the electrical activation, the selected
annealing temperatures were so high that the entire
implanted distribution was broadened and diffused to
10 greater depths within the base crystal. By contrast,
in the present invention the two step annealing process
is utilized in recognition of the two separate functions
performed by annealing. In the first annealing step of
the present invention, the substantially defect free
15 crystalline structure of the silicon layer 12 is restored
by recrystallization of the amorphized layer 20. This
thermal annealing restores the low resistivity of the
substantially defect free silicon layer 12, but is
conducted at a sufficiently low temperature that
20 thermally activated diffusion of the implanted species
26 cannot occur. However, such very low annealing
temperatures cannot electrically activate the implanted
species 26. The second annealing step is conducted at
a sufficiently high temperature to achieve this electrical
25 activation, but the second annealing step is so brief
that the activated dopant species cannot diffusionally
migrate distances substantially greater than one lattice
spacing of the silicon crystal, so that the implanted
distribution 24 neither broadens nor migrates to greater
30 depths within the base crystal. It is to be noted that
the desired annealing profile such as that illustrated
in FIGURE 2 can be achieved by other, carefully
controlled techniques such as electron beam heating
using the approach described herein.

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1 After the two step annealing procedure is completed,
the wafers 10 are cooled down to about 500° at a rate of
about 10°C per minute in the controlled atmosphere of
the chamber 36. The wafers 10 are then removed and
5 placed on a cold surface to rapidly cool them to ambient
temperature. However, the wafers 10 are not quenched
at a high rate which might break the wafer 10, or
produce high thermal strains which could induce defects
in the wafer 10, which would increase the electrical
10 resistivity of the wafer 10.

Hyperabrupt adjunctions having structure and
characteristics previously unobtainable have been
produced in accordance with the present invention.
Such a wafer comprises a silicon base crystal, either
15 in bulk form or on a substrate, which is substantially
free of defects in the electronic sense, and a hyperabrupt
retrograde distribution of an activated species contained
in the near surface region of the base crystal, wherein
the near surface region has a depth of no more than
20 about 0.20 micrometers. The implanted species are
selected from those previously mentioned, boron, BF_2^+ ,
phosphorus, or arsenic. The gradient of the retrograde
distribution is determined by the implanted profile,
and is at least as great as the difference between the
25 maximum solubility of the species and the zero level,
this difference to be obtained over a distance of less
than about 0.10 micrometers in depth of the crystal.
The peak of the distribution is at a depth as low as
about 0.005 to 0.010 micrometers, and the retrograde
30 gradient is as high as the difference between the
maximum solid solubility of the dopant species and a
level of substantially zero (i.e., a decrease of four
orders of magnitude) over a distance of 0.100 micro-
meters or less, and typically over a distance of 0.20

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1 micrometers. Such a wafer has a sheet conductivity of
less than about 100 ohms per square, and in particular,
sheet resistivities as low as about 60 ohms per square
have been obtained. Such shallow junction depths and
5 low sheet resistivities have not been previously
obtainable by conventional techniques.

In most instances, the wafers produced in accordance
with the present invention are not used in their as-
fabricated form in devices. Instead, the fabricated
10 wafers as described herein are used as the starting
point for the fabrication of FETS and other devices, to
form integrated circuits. The process described herein
may also be used as an intermediate subprocess in a
more complex device fabrication procedure, as will be
15 described next.

The process described herein has been used
successfully in fabricating self-aligned integrated
circuit devices. The basic approach to preparing such
devices is known in the art and is described in United
20 States Patents 3,472,712; 3,615,934; and 3,507,709,
whose disclosures are herein incorporated by reference.
A preferred form of self-aligned device 60 prepared in
accordance with the present invention is illustrated in
FIGURE 4. A base crystal 62 upon which the device is
25 fabricated may be either pure bulk silicon or silicon
on sapphire. A layer 64 of SiO_2 is thermally grown on
the base crystal to a thickness of about 0.02 micrometers.
An N^+ doped polysilicon contact 66 is then deposited
onto the SiO_2 layer 64 as an electrical contact to the
30 SiO_2 gate layer 64. Next, a mask 68 is applied so as
to leave two openings 70 therethrough, the openings 70
being adjacent to, but laterally displaced from, the
contact 66.

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1 The N+ source region 72 and drain region 73 are
formed with a shallow, hyperabrupt junction, preferably
by a slight modification of the previously described
process. The process is modified only to the extent of
5 changing the amorphizing and implanting conditions to
account for the presence of the layer 64, which generally
requires slightly higher implantation voltages. The
source 72 and drain 73 are first amorphized by a two-
step implantation of Si⁺ ions, first at an energy of
10 140 KeV and dose of 2×10^{15} ions per square centimeter
and second at an energy of 25 KeV and dose of 2×10^{15}
ions per square centimeter. The amorphized layer so
produced is about 0.200 micrometers in depth, below an
interface 74 between the SiO₂ layer 64 and the base
15 crystal 72.

Next, a dopant species is implanted in a retrograde
distribution 76, the preferred dopant species being
boron, BF₂⁺, phosphorus or arsenic. The preferred
implanted conditions are listed in the following table.

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<u>Ions</u>	<u>Implantation Energy in KeV</u>	<u>Dose in Ions Per Square Centimeter</u>
Boron	20	$2-4 \times 10^{15}$
25 BF ₂ ⁺	53	$2-4 \times 10^{15}$
Phosphorus	62	$2-4 \times 10^{15}$
Arsenic	120	$2-4 \times 10^{15}$

30 Dose current to be less than about 0.2 microamps per
square centimeter.

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1 It will be noted that the implantation energies are
adjusted to be slightly higher than those disclosed
previously, to allow implantation through the SiO₂ layer
64. As implanted, the peak of the distribution 76 is
5 about 0.025 micrometers below the upper surface of the
SiO₂ layer 64, or about 0.005 micrometers below the
interface 74. The concentration of the implated dopant
species falls about four orders of magnitude over a depth
of about .020 micrometers. This combination of a shallow,
10 hyperabrupt dopant distribution has heretofore been
unobtainable, but is critical to the development of
devices having submicron gate lengths. The mask 70 is
removed by standard procedures. The device 60 is next
annealed by the two-step process described previously,
15 preferably at 600°C for 30 minutes and at 1100°C for 1
second. Finally, electrical contacts are applied. These
device fabrication steps are readily conducted interme-
diate in the fabrication of integrated circuits involving
many steps, and are fully compatible with such
20 conventional technology.

 The present invention thus provides an important
advance in the technology of fabricating integrated
circuit devices. Controlled distributions of rapidly
diffusing implanted species can be produced in a
25 substantially defect-free base crystal. In particular,
steep, hyperabrupt retrograde junctions can be produced in
substantially defect free silicon base crystals, either in
their bulk form or as epitaxially deposited on substrates.

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1 Although a particular embodiment of the invention has been
described for purposes of illustration, various modifi-
cations may be made without departing from the spirit and
scope of the invention. Accordingly, the present inven-
5 tion is not to be limited except as by the appended
claims.

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CLAIMSWhat is Claimed is:

- 1 1. A process for preparing a shallow, hyperabrupt
interface between an undoped layer and a layer doped
with a rapidly diffusing, activated species, in a
crystalline near-surface layer of a base crystal,
5 comprising the steps of:
 amorphizing the near-surface layer of the
base crystal to produce an amorphized layer of the
underlying base crystal;
 implanting a steep retrograde distribution of
10 a rapidly diffusing implanted species into the amorphized
layer, the retrograde distribution residing substantially
entirely within the amorphized region, said step of
implanting to occur at a temperature of the base crystal
whereat the implanted species is essentially diffusionally
15 immobile in the amorphized layer;
 annealing the base crystal at a first annealing
temperature sufficiently high to achieve solid phase
epitaxial growth in the amorphized layer on the
crystalline portion of the base crystal, whereby the
20 amorphized layer is recrystallized, the first annealing
temperature being sufficiently low that the implanted
species is substantially diffusionally immobile in the
recrystallizing layer; and
 annealing the base crystal at a second
25 annealing temperature greater than the first annealing
temperature, for a time sufficient to activate the
implanted species but not to permit large scale diffusion
of the implanted species, thereby producing a shallow,
hyperabrupt interface in the crystalline near-surface
30 region of the base crystal.

- 1 2. The process of Claim 1, wherein the base
crystal is silicon.
- 1 3. The process of Claim 1, wherein the implanted
species is selected from the group consisting of boron,
 BF_2^+ , phosphorus, and arsenic.
- 1 4. The process of Claim 1, wherein the maximum
concentration of the implanted species is about the
maximum solubility of the implanted species at the
second annealing temperature.
- 1 5. The process of Claim 1, wherein the amorphized
layer is about 0.20 micrometers in thickness.
- 1 6. The process of Claim 1, wherein the first
annealing temperature is from about 550°C to about
650°C.
- 1 7. The process of Claim 1, wherein the second
annealing temperature is from about 1000°C to about
1150°C.
- 1 8. A process for producing a controlled distri-
bution of an activated, rapidly diffusing, implanted
species within the near-surface layer of a base crystal,
comprising the steps of:
- 5 altering the near-surface layer of the base
crystal from its normal structure to reduce the
diffusivity and implant channelling of the implanted
species, thereby forming a treated layer;

implanting the implanted species within the
10 treated layer in the desired controlled distribution;
reverting the base crystal of the treated
layer to its normal crystalline structure; and
activating the implanted species, thereby
leaving the base crystal with the controlled distribution
15 of the implanted species in an activated form.

1 9. The process of Claim 8, wherein said step of
altering includes amorphizing the near-surface layer.

1 10. The process of Claim 8, wherein the controlled
distribution is a hyperabrupt retrograde distribution.

1 11. The process of Claim 8, wherein the step of
reverting includes heating the base crystal at a first
annealing temperature to cause solid phase epitaxial
growth of the treated layer.

1 12. The process of Claim 8, wherein the step of
activating includes heating the base crystal to a second
annealing temperature.

1 13. A process for producing a hyperabrupt retrograde
distribution of an implanted species in a silicon base
crystal, comprising the steps of:

5 amorphizing a depth of about 0.20 micrometers
of the silicon crystal;

implanting the dopant species selected from
the group consisting of boron, BF_2^+ , phosphorus, and
arsenic so that a retrograde distribution of the dopant
species lies entirely within the amorphized layer;

10 annealing the implanted base crystal at a
temperature of from about 550°C to about 750°C to
achieve solid phase epitaxial growth; and

 annealing the implanted base crystal at a
temperature of from about 1000°C to about 1150°C to
15 achieve activation of the implanted species.

1 14. The process of Claim 13, wherein the first
annealing is conducted at a temperature of about 600°C
for a time of about 30 minutes.

1 15. The process of Claim 13, wherein the second
annealing is conducted at a temperature of about 1100°C
for a time of about 1 second.

1 16. The process of Claim 13, wherein said
amorphizing step is accomplished by implanting Si⁺
ions.

1 17. A wafer having a hyperabrupt junction therein,
comprising:

 a base crystal substantially free of defects;
and

5 a hyperabrupt retrograde distribution of an
activated species contained in a near-surface layer of
the base crystal, the layer having a depth of no more
than about 0.20 micrometers, the gradient of the
retrograde distribution being at least as great as the
10 difference between the maximum solubility of the species
and a substantially zero level over a distance of less
than about 0.10 micrometers.

1 18. The wafer of Claim 17, wherein the sheet
resistivity is less than about 100 ohms per square.

- 1 19. The wafer of Claim 17, wherein the base
crystal is silicon.
- 1 20. The wafer of Claim 17, wherein the dopant
species is selected from the group consisting of boron,
phosphorus, and arsenic.
- 1 21. The wafer of Claim 17, wherein the hyperabrupt
junction is contained within a self-aligned integrated
circuit device.
- 1 22. The wafer of Claim 17, further including a
layer of SiO₂ on the base crystal.
- 1 23. The wafer of Claim 17, wherein the maximum
value of the concentration of the activated species is
located at a distance of about 0.005 micrometers below
the surface of the base crystal.

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Fig. 1

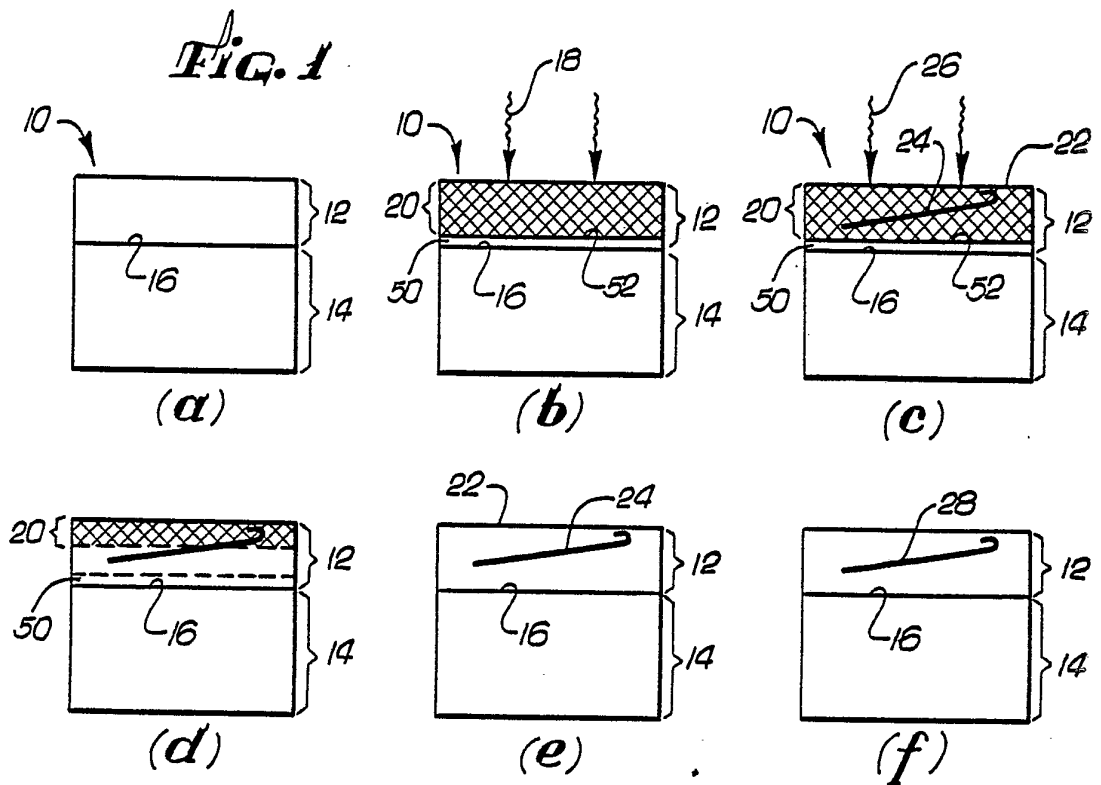


Fig. 2

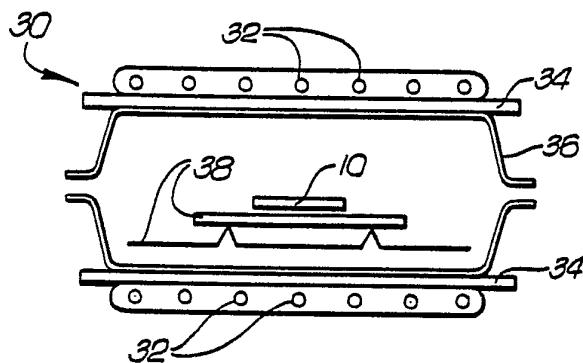
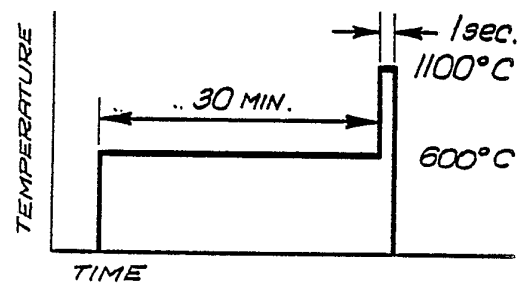


Fig. 3

Fig. 4

