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[45] **Nov. 27, 1973**

[54] **FLUID DENSITY DIGITAL COMPUTER**

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[52] **U.S. Cl.** ..... **235/92 MT,** 235/151.3, 73/32, 235/92 CP, 235/92 R

[51] **Int. Cl.** **G06f 15/56**

[58] **Field of Search** ..... 235/92 MT, 92 CP, 235/151.3, 151.35; 73/32

[56] **References Cited**

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Primary Examiner—Thomas A. Robinson
Assistant Examiner—Joseph M. Thesz, Jr.
Attorney—C. Cornell Remsen, Jr. et al. and A. Donald Stolzy

[57] **ABSTRACT**

Apparatus for producing a digital output from a storage register directly proportional to fluid density. A count down counter is preset to

$$STT_o/R$$

where S, T_o, T and R are constants. Constants R and S may be found empirically from a simple vibration densitometer test. Constant T is more or less arbitrary. The pulse output of the densitometer is then employed to cause the counter to count down for periodic time invariant gating intervals. The number in the counter at the end of each such interval is then entered in the storage register, this number being directly proportional to density. The system of the disclosure can be employed to reduce analog computer error to an insignificant magnitude.

13 Claims, 7 Drawing Figures

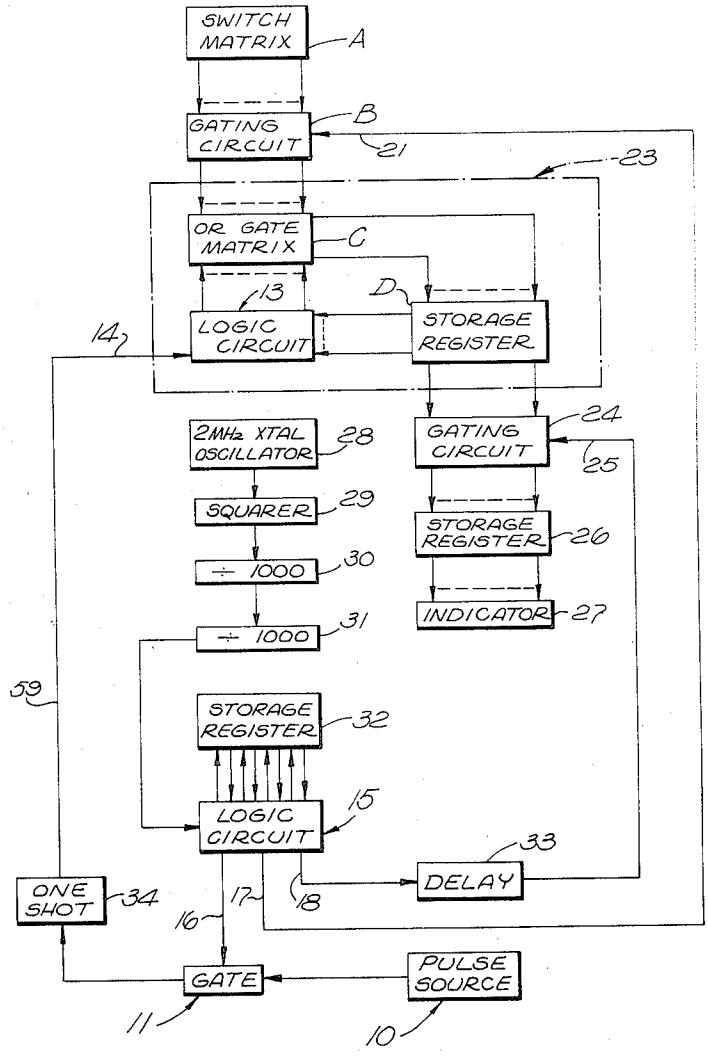
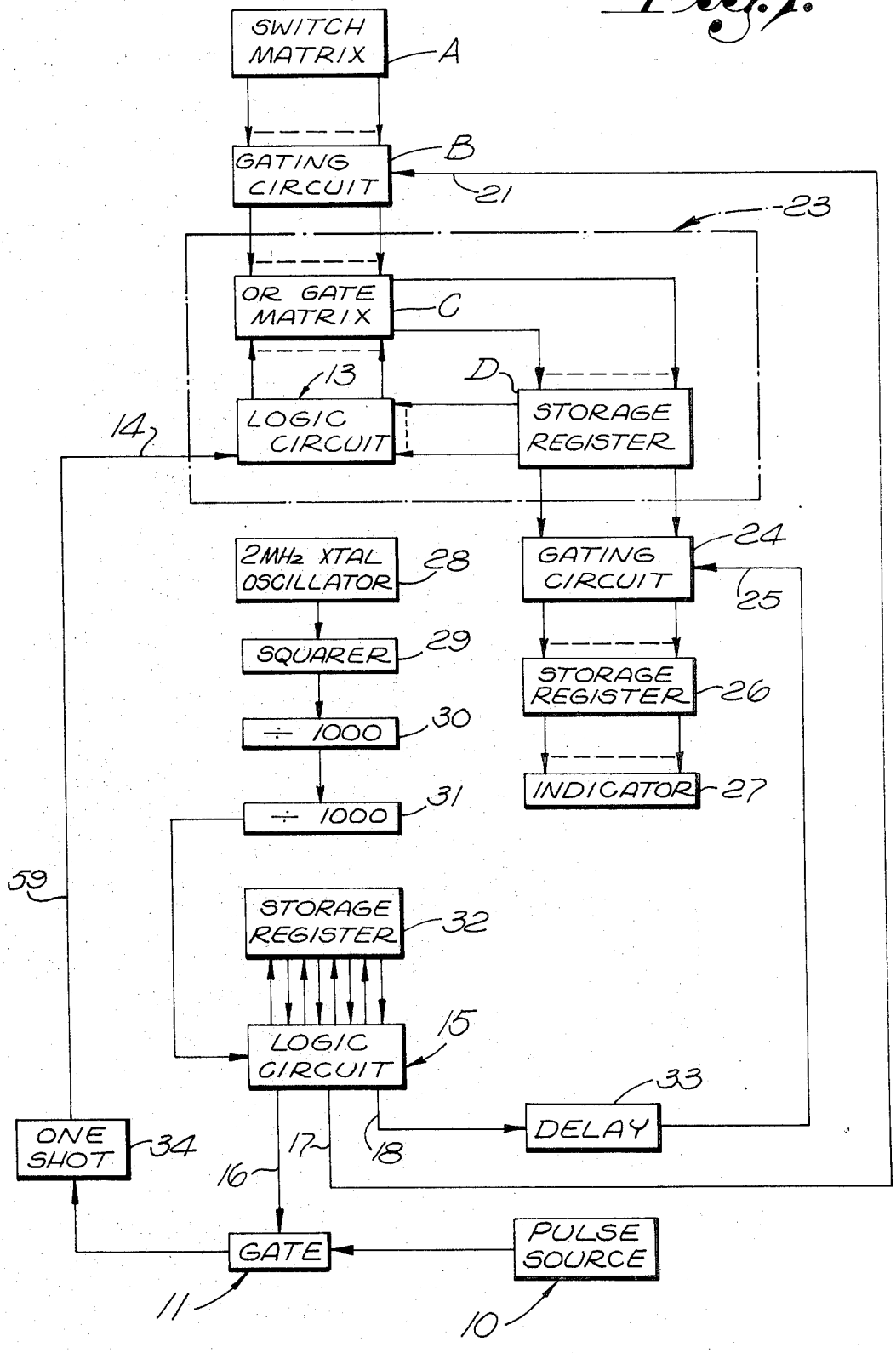


Fig. 1.


SWITCH MATRIX
A
GATING CIRCUIT
B
21
23
OR GATE MATRIX
C
13
D
LOGIC CIRCUIT
STORAGE REGISTER
14
2MH2 XTAL OSCILLATOR
28
GATING CIRCUIT
24
25
SQUARER
29
STORAGE REGISTER
26
÷ 1000
30
INDICATOR
27
÷ 1000
31
59
STORAGE REGISTER
32
LOGIC CIRCUIT
15
33
DELAY
ONE SHOT
34
17
16
18
GATE
PULSE SOURCE
11
10

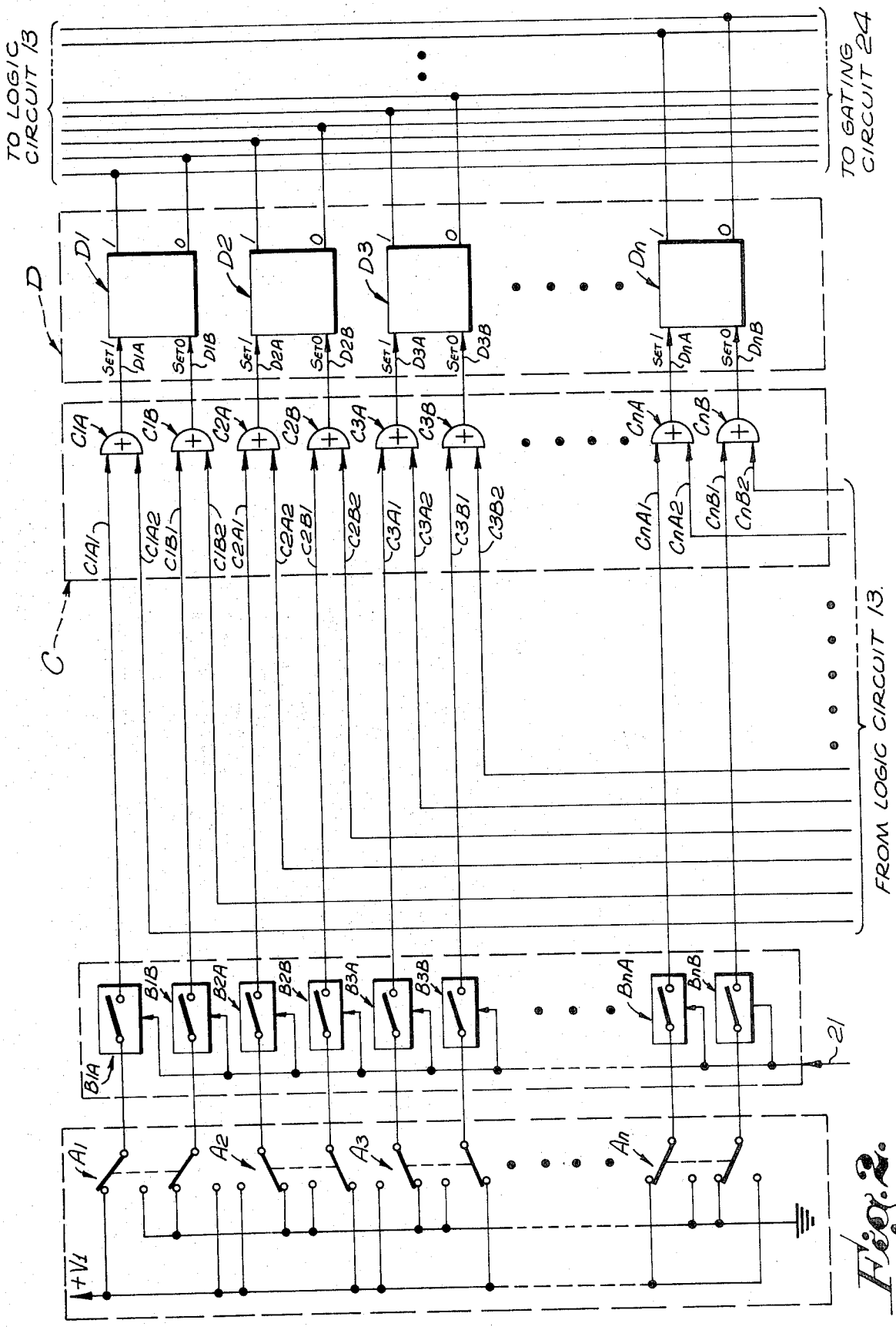

TO LOGIC CIRCUIT 13
TO GATING CIRCUIT 24
FROM LOGIC CIRCUIT 13
D
C
D1
D2
D3
Dn
SET 1
SET 0
D1A
D1B
D2A
D2B
D3A
D3B
DnA
DnB
C1A
C1B
C2A
C2B
C3A
C3B
CnA
CnB
C1A1
C1A2
C1B1
C1B2
C2A1
C2A2
C2B1
C2B2
C3A1
C3A2
C3B1
C3B2
CnA1
CnA2
CnB1
CnB2
B1A
B1B
B2A
B2B
B3A
B3B
BnA
BnB
21
A1
A2
A3
An
+V1

Fig. 2.

COUNT	X	Y	Z
7	1	1	1
6	0	1	1
5	1	0	1
4	0	0	1
3	1	1	0
2	0	1	0
1	1	0	0
0	0	0	0

Fig. 3.

Fig. 5.

COUNT	M	N
3	1	1
0	0	0
1	1	0
2	0	1

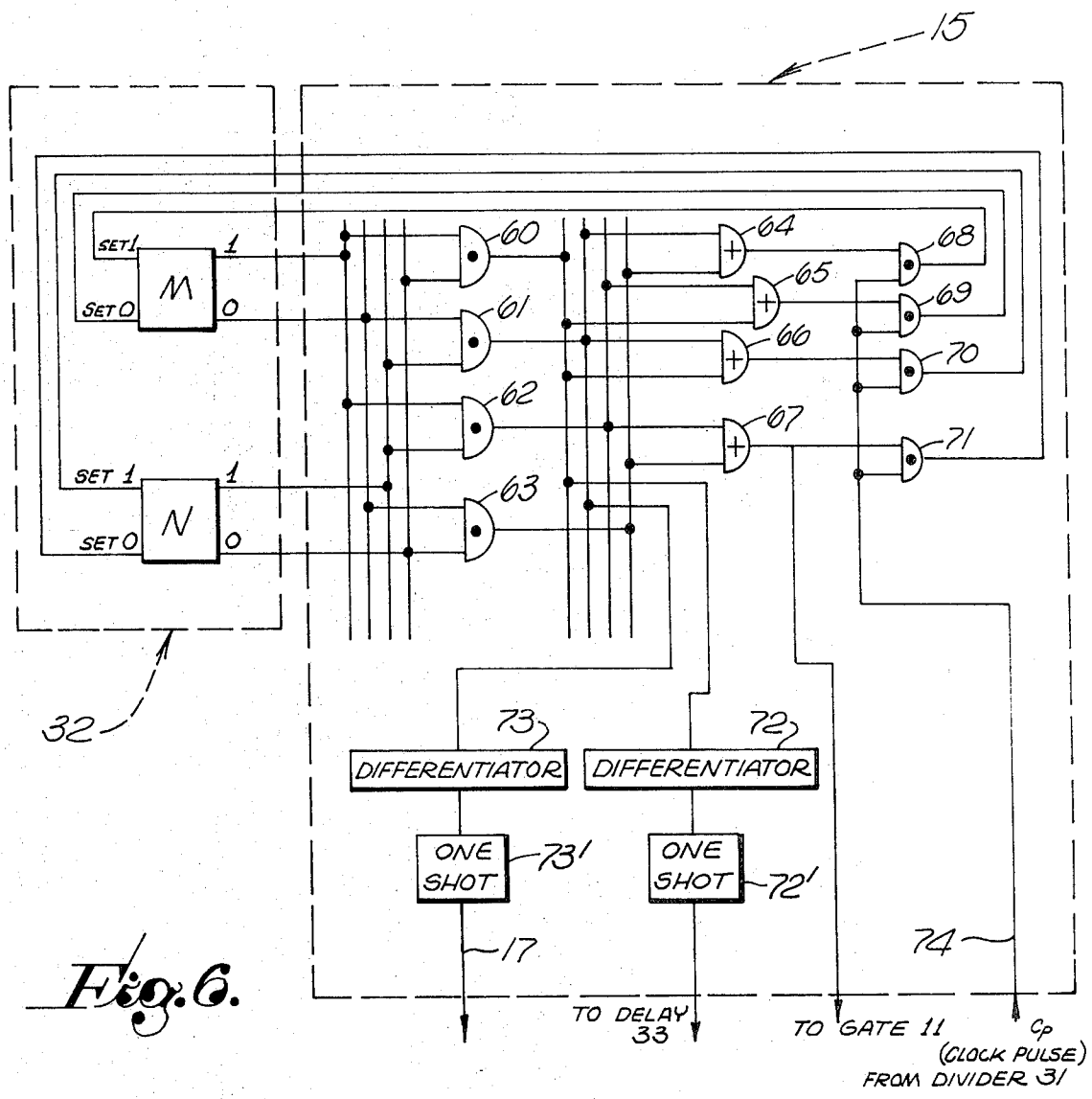


Fig. 6.

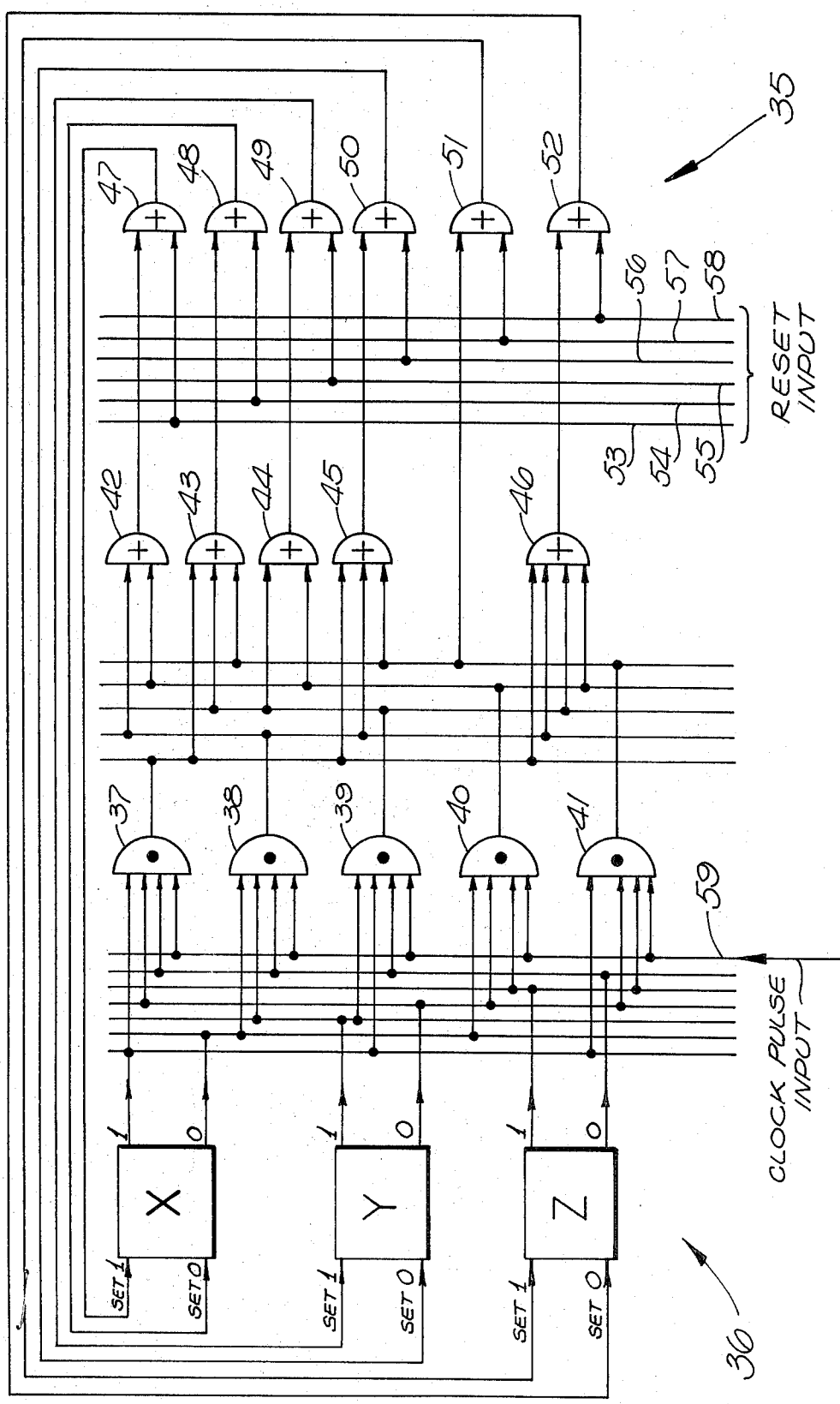

35
47
48
49
50
51
52
56
57
58
RESET INPUT
53
54
55
42
43
44
45
46
37
38
39
40
41
59
CLOCK PULSE INPUT
1
0
X
Y
Z
SET 1
SET 0
36

Fig. 4.

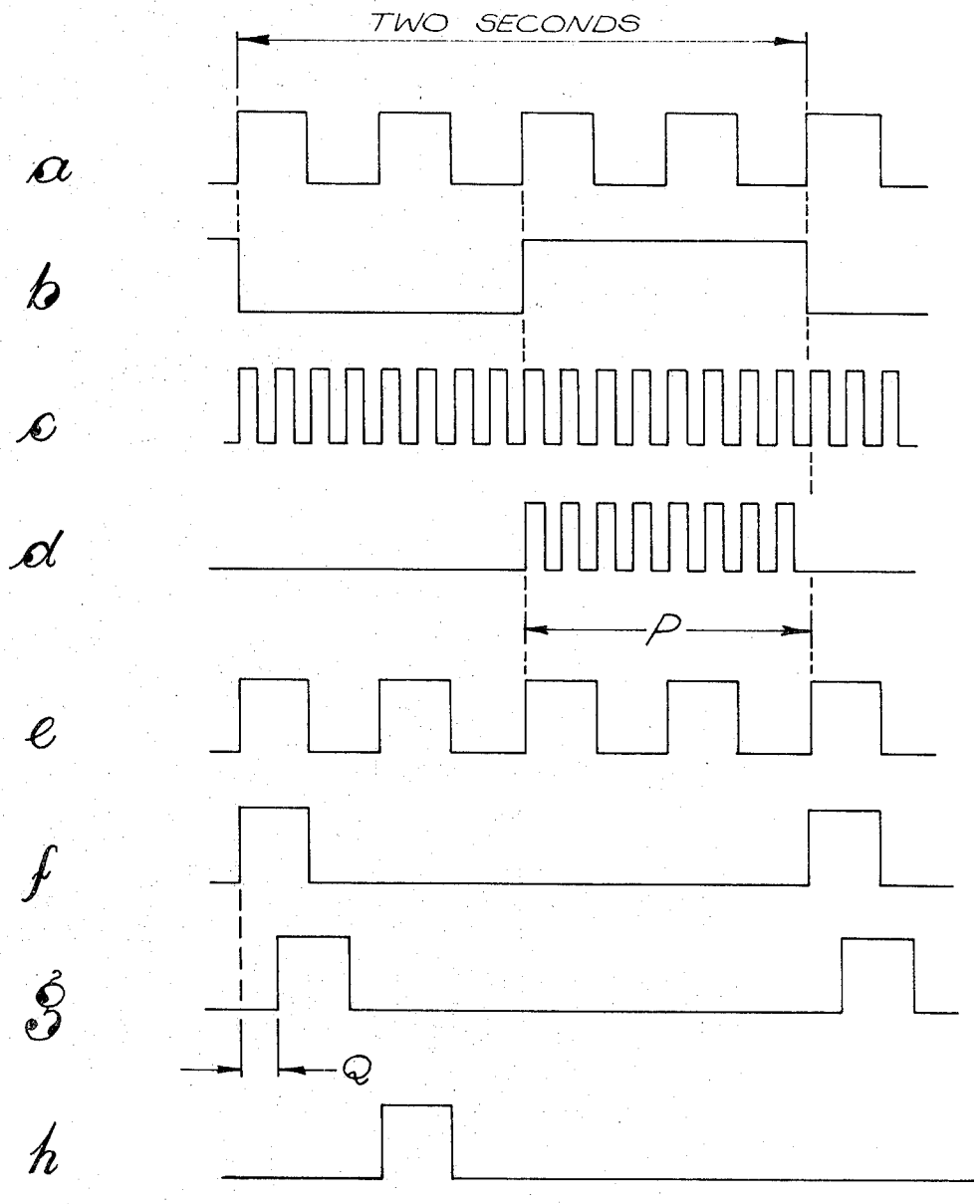


Fig. 7.

FLUID DENSITY DIGITAL COMPUTER

BACKGROUND OF THE INVENTION

This invention relates to apparatus for producing an output directly proportional to the density of a fluid, and more particularly, to a digital computer for use with fluid densitometer components.

In the past it has been the practice to compute fluid density from the output of vibration densitometer apparatus by the use of analog computers. There are, therefore, added inaccuracies because analog computers introduce certain finite errors which cannot be eliminated.

SUMMARY OF THE INVENTION

In accordance with the system of the present invention, the above-described and other disadvantages of the prior art are overcome by entering a predetermined number in the main register of a count down counter and using the densitometer output pulses to cause the counter to count down. The number remaining in the main register after a fixed counting interval is then proportional to the fluid density.

The above-described and other advantages of the present invention will be better understood from the following detailed description when considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings which are to be regarded as merely illustrative:

FIG. 1 is a block diagram of one embodiment of the present invention;

FIG. 2 is a schematic diagram of several of the blocks shown in FIG. 1;

FIG. 3 is a truth table for a count down counter;

FIG. 4 is a detailed block diagram of a count down counter;

FIG. 5 is a truth table for a storage register shown in FIG. 1;

FIG. 6 is a detailed block diagram of a storage register and logic circuit shown in FIG. 1; and

FIG. 7 is a graph of a group of waveforms characteristic of the operation of the invention shown in FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A pulse source **10** is shown in FIG. 1 connected to a gate **11**. Pulse source **10** may, if desired, be identical to all structures shown in FIG. 7 of U. S. Pat. No. 3,677,067, with the exception of linearization circuit **109** and indicator **110**. The output of a tracking filter **91** also illustrated in this patent may then be connected as an input to gate **11** herein.

The output of pulse source **10** herein has a pulse repetition frequency *f*. The vibration densitometer probe disclosed in U. S. Pat. No. 3,677,067 is immersed in a fluid. The density *d* of this fluid over a reasonable range can then be determined from the equation

$$d = -Rf + S$$

The terms R and S are generally positive constants which can be determined empirically from an instrument by measuring *f* twice with the probe in two different respective fluids of known densities. (See the said patent).

Something about certain structures disclosed herein is discussed in the material immediately following. The importance of some of this discussion may be apparent only from subsequent explanations.

A main storage register D is illustrated in FIG. **1**. As will be described, a predetermined number V is entered in storage register D periodically. This number is

$$V = STT_o/R$$

where T_o is the time width of pulses on an output lead **16** of a logic circuit **15** shown in FIG. **1**, and T is an arbitrary constant. For the apparatus shown in FIG. **1**, T may be equal to unity.

A logic circuit is provided at **13**. Logic circuit **13** has an input **14** which receives pulses when gate **11** is open, at a rate in the general case T*f*. However, gate **11** does not modify *f* at the output of source **10** in FIG. **1**. Thus, in the specific case of FIG. **1**, $Tf = f$ because $T = 1$.

Logic circuit **15** impresses gating pulses on gate **11** over lead **16**. Each of these gating pulses have the same time width. This time width is large in comparison to the reciprocal of *Tf*.

Logic circuit **15** also has output leads **17** and **18**. The pulses on output leads **16**, **17** and **18** may be further identified herein as pulses *pg*, *pr* and *pc*, respectively, having pulse repetition frequencies *fg*, *fr* and *fc*, respectively, where $fg = fr = fc$.

In FIG. **1**, the said predetermined number V is periodically entered in storage register D. The magnitude of the predetermined number may be selected or changed by operating certain switches, to be described, which are located in a switch matrix A. The switches in matrix A are either connected from a positive potential V1 or ground. The outputs of the switches are sampled and impressed upon storage register D periodically. A sampling gate is, thus, impressed upon a gating circuit B over a lead **21** for this purpose.

Gating circuit B is connected from matrix A to an OR gate matrix C. The output of OR gate matrix C is then impressed upon storage register D.

Once the said predetermined number V has been entered into storage register D, logic circuit **13** then controls the register D to count down. The output of logic circuit **13** is, thus, impressed upon storage register D through OR gate matrix C. Logic circuit **13** receives pulses to count at input **14**. Logic circuit **13** receives other inputs from storage register D.

From the foregoing, it will be appreciated that matrix C with logic circuit **13** and storage register D form a count down counter. This counter may be entirely conventional, if desired. The count down counter is indicated at **23**.

The output of storage register D is also sampled periodically by a gating circuit **24** which may be of the same type as gating circuit B. Gating circuit **24** receives pulses to cause it to sample the output of register D over a lead **25**. The output of gating circuit **24** is impressed upon a storage register **26**. The output of the storage register **26** is impressed upon an indicator **27**.

If desired, indicator **27** may be binary coded decimal.

All of the structures D, **13**, A, B, C, **24**, **26** and **27** may be entirely conventional by themselves, although the combination thereof is new.

Alternatively, indicator **27** may simply be a row of lamps each connected from the 1 output of each of the flip-flops in storage register **26**.

Pulses are supplied to leads **21** and **25**, and to input **14** responsive to the outputs of logic circuit **15**. Logic circuit **15** operates from a 2 megahertz crystal oscillator **28**. A squarer **29**, a divide-by-one thousand divider **30**, and a divide-by-one thousand divider **31** are connected in succession in that order from oscillator **28** to logic circuit **15**. Logic circuit **15** and a storage register **32** connected therewith operate, more or less, as a counter. Logic circuit output lead **18** is connected to lead **25** through a delay **33**. Logic circuit output lead **17** is connected to lead **21**. Logic circuit output lead **16** is connected to the gate **11**. The output of pulse source **10** is also connected to gate **11**. The output of gate **11** is connected to input **14** through a one-shot multivibrator **34**.

As shown in FIG. **2**, the purpose of the switch matrix A is to set, periodically, the flip-flops in storage register D to selected states. Switch matrix A includes double-pole, double-throw switches A1, A2, A3 . . . An.

Gating circuit B includes swiches B1A, B2A, B3A . . . BnA connected respectively from the upper poles of switches A. Gating circuit B also includes switches B1B, B2B, B3B . . . BnB connected respectively from the lower poles of the switches A. Lead **21** is connected to each of the switches B to operate the same. The switches B may be entirely conventional electronic switches, if desired.

OR gate matrix C includes OR gates C1A, C2A, C3A . . . CnA having inputs C1A1, C2A1, C3A1 . . . CnA1, respectively. OR gates C1A, C2A, C3A . . . CnA also have input leads C1A2, C2A2, C3A2 . . . CnA2, respectively.

OR gate matrix C also includes OR gates C1B, C2B, C3B . . . CnB which have inputs C1B1, C2B1, C3B1 . . . CnB1, respectively. The OR gates C1B, C2B, C3B . . . CnB also have inputs C1B2, C2B2, C3B2 . . . CnB2, respectively. The OR gate inputs C1A1, C2A1, C3A1 . . . CnA1 are connected respectively from switches B1A, B2A, B3A . . . BnA. The OR gate inputs C1B1, C2B1, C3B1 . . . CnB1 are connected respectively from switches B1B, B2B, B3B . . . BnB.

The OR gate inputs C1A2, C2A2, C3A2 . . . CnA2, and the OR gate inputs C1B2, C2B2, C3B2 . . . CnB2 are respectively connected from corresponding outputs of logic circuit **13**.

Storage register D includes flip-flops D1, D2, D3 . . . Dn. Flip-flops D1, D2, D3 . . . Dn have set 1 inputs D1A, D2A, D3A . . . DnA respectively connected from the outputs of OR gates C1A, C2A, C3A . . . CnA, respectively. Flip-flops D1, D2, D3 . . . Dn also have set 0 inputs D1B, D2B, D3B . . . DnB respectively connected from the outputs of OR gates C1B, C2B, C3B . . . CnB, respectively.

As will be noted in FIG. **2**, the outputs of flip-flops D are connected both to logic circuit **13** and to gating circuit **24**.

A truth table for a typical count down counter is shown in FIG. **3**. A counter **35** therefor is shown in FIG. **4**. The counter of FIG. **4** has a storage register **36** including only three flip-flops X, Y and Z. With the logic shown, the counter is adapted to count down only from **1, 2, 3, 4** or **5**.

In FIG. **4**, counter **35** includes AND gates **37, 38, 39, 40** and **41**. Counter **35** also includes OR gates **42, 43, 44, 45** and **46**. In FIG. **4**, counter **35** also includes OR gates **47, 48, 49, 50, 51** and **52**. OR gates **47–52** receive inputs over leads **53-58** from a reset input. That is, for the counter to count down, there must first be a number entered over the leads **53–58**. That is the purpose of the OR gates **47–52**. That is, the OR gates **47–52** not only permit the control of the flip-flops X, Y and Z, according to the count down logic, the OR gates **47–52** also permit the entry of a number in the register **36**. In general, the reset input on leads **53–58** will be supplied at a time different from the time that clock pulses are supplied to each of the AND gates **37–41** over a lead **59**. Thus, the OR gates **47–52** perform precisely the same function as OR gates C in FIG. **2**.

As stated previously, in general, register **32** and logic circuit **15**, shown in FIG. **1**, form a counter. The logic of this counter is illustrated in FIG. **5**.

Register **32** and logic circuit **15** are again shown in FIG. **6**. As shown in FIG. **6**, register **32** includes only two flip-flops M and N. Logic circuit **15** has four AND gates **60, 61, 62** and **63**. Logic circuit **15** has four OR gates **64, 65, 66** and **67**. Logic circuit **15** also has four AND gates **68, 69, 70** and **71**.

If the input to logic circuit **15** from divider **31** is considered to be a clock pulse Cp, the logic of the gates in logic circuit **15** may be expressed as follows, the clock pulse input to logic circuit **15** from divider **31** being applied over a lead **74**. The logic of gate **60** is $M\overline{N}$. The logic of gate **61** is $\overline{M}N$. The logic of gate **62** is MN. The logic of gate **63** is $\overline{M}\overline{N}$. The logic of gate **64** is $\overline{M}N + M\overline{N}$. The logic of gate **65** is $M\overline{N} + MN$. The logic of gate **66** is $M\overline{N} + \overline{M}N$. The logic of gate **67** is $MN + M\overline{N}$.

The logic of gate **68** is Cp $(\overline{M}N + \overline{M}\overline{N})$. The logic of gate **69** is Cp $(M\overline{N} + MN)$. The logic of gate **70** is Cp $(M\overline{N} + \overline{M}N)$. The logic of gate **71** is Cp $(MN + \overline{M}\overline{N})$.

A differentiator **72** and a one-shot **72'** are connected from AND gate **60** to delay **33**. A differentiator **73** and a one-shot **73'** are connected from AND gate **60** to lead **17**.

The output of divider **31** may be as illustrated at (*a*) and (*e*) in FIG. **7**.

The mark-to-space ratio of the waveform of (*a*) in FIG. **7** may be unity, if desired. However, this is by no means critical. The period of the waveform of (a) in FIG. **7** may be one-half second, if desired. However, again, this period is not critical.

The waveform appearing on the output lead **16** of logic circuit **15** shown in FIG. **1** is illustrated at (b) in FIG. **7**. This waveform appears on the output lead in FIG. **6** labeled **74**.

Pulse source **10** in FIG. **1** may produce output pulses as indicated at (c) in FIG. **7**. However, the pulse repetition frequency of the pulses (c) in FIG. **7** has been greatly reduced for clarity. Actually, the pulse repetition frequency of the output pulses of source **10** may vary about 4.0 kilohertz, if desired.

The pulses appearing on the output lead labeled "to delay **33**" in FIG. **6** are illustrated at (f) in FIG. **7**.

The output of delay **33** is indicated at (g) in FIG. **7**. The pulses at (g) in FIG. **7** may, thus, be delayed relative to the pulses (f) in FIG. **7** by a time Q, if desired. The pulses appearing upon the output lead **17** of logic circuit **15** in FIGS. **1** and **6** are illustrated at (h) in FIG. **7**.

Delay **33**, in some cases, may be eliminated entirely. Delay **33** may be any conventional delay, if desired.

The pulses (g) and (h) in FIG. **7** may be much narrower than shown, as desired. Further, in some cases, the pulses of (g) and (h) in FIG. **7** may occur simultaneously. Although it is not absolutely required, in some

cases, preferably the leading edge of the pulses (g) in FIG. 7 do not occur prior to the trailing edges of the pulses (b) in FIG. 7, the leading edges of the pulses (h) do not occur prior to the trailing edges of pulses (g), and the leading edges of the pulses (b) do not occur prior to the trailing edges of the pulses (h).

From the foregoing, it will be appreciated that the outputs of logic circuit 13 are disconnected from OR gate matrix C except during receipt of a pulse from the output of one-shot multivibrator 34 in FIG. 1. For example, in FIG. 4, gates 37–41 produce no output except during receipt of pulses over lead 59.

The word "indicate" as used herein in any of its grammatical forms hereby is defined to include, but not be limited to, an indication which either is visual or is not visual. Moreover, the output of storage register 26 may be employed for process control without the use of any indicator such as indicator 27.

The phrase "utilization means" as used herein is hereby defined to include an indicator, a process controller or otherwise.

Although a symbol has been used consistently in the drawings to represent OR gates, it is to be understood that this symbol includes, but is not limited to, a wire OR gate. Thus, one or more or all of the symbols employed herein to represent an OR gate may or may not be a wire OR gate, as desired.

The phrase "OR gate" as used herein is hereby defined to include a NOR gate with or without an inverter, as necessary or desirable.

What is claimed is:

1. A digital control system comprising: densitometer apparatus for producing output pulses at a pulse repetition frequency f approximately proportional to the density d of a fluid such that

$$d = -RF + S$$

where R and S are constants; a main storage register; reset means to enter a predetermined number into said main register periodically, said predetermined number being equal to V, where

$$V = \mathrm{STT}_o/R$$

T_o is the time width of a pulse *pg*, and T is a constant; a gate; synchronization means, logic means connected to and from said main register and from said gate to cause the count stored in said main register to be reduced by one upon receipt thereby of each output pulse of said gate; an output storage register; a gating circuit connected from said synchronization means and said main storage register to said output storage register, said gate being connected from said densitometer apparatus, said synchronization means being constructed to impress pulses *pg* on said gate to cause said gate to pass densitometer apparatus pulses to said logic means at a rate equal to Tf, said synchronization means holding said gate open periodically for periods large in comparison to the reciprocal of Tf, said synchronization means impressing a pulse pr periodically on said reset means to cause reset means to enter said predetermined number in said main register at a time which precedes the first output pulse of said gate after it is opened, said synchronization means being connected to said gating circuit to supply a pulse *pc* thereto to cause the number stored in said main register to be transferred into said output storage register after said gate is closed; and utilization means connected from said output storage register.

2. The invention as defined in claim 1, wherein said synchronization means generates said pulses pg, pr and pc in synchronism.

3. The invention as defined in claim 2, wherein said pulses *pg*, *pr* and pc have pulse repetition frequencies *fg*, *fr* and *fc*, respectively, where $fg = fr = fc$, all of said pulses, *pg*, *pr* and *pc* occurring during mutually exclusive intervals of time, each pulse immediately succeeding a pulse *pr* being a pulse *pg*, each pulse immediately succeeding a pulse *pg* being a pulse *pc*.

4. The invention as defined in claim 3, wherein the pulse width of each of said pulses *pg* is invariant with time.

5. The invention as defined in claim 4, wherein said predetermined number is invariant with time.

6. The invention as defined in claim 5, wherein said reset means is manually adjustable to change said predetermined number.

7. The invention as defined in claim 6, wherein first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2, C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA being connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

8. The invention as defined in claim 7, wherein said utilization means includes means to indicate the magnitude of the number stored in said storage register.

9. The invention as defined in claim 2, wherein said first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively,

said OR gates C1A C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2, C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA being connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

10. The invention as defined in claim **3,** wheein first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2, C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA being connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

11. The invention as defined in claim **4,** wherein first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2, C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA being connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

12. The invention as defined in claim **5,** wherein first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2 C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA being connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

13. The invention as defined in claim **1,** wherein first and second sets of OR gates are provided, said first set of OR gates including OR gates C1A, C2A, C3A . . . CnA, said second set of OR gates including OR gates C1B, C2B, C3B . . . CnB, said main storage register having first and second sets of inputs, said first set of main register inputs being D1A, D2A, D3A . . . DnA, said second set of main register inputs being D1B, D2B, D3B . . . DnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB being connected to corresponding respective main register inputs D1A, D2A, D3A . . . DnA and D1B, D2B, D3B . . . DnB, said reset means having a first set of output devices B1A, B2A, B3A . . . BnA, said reset means also having a second set of output devices B1B, B2B, B3B . . . BnB, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB having first inputs C1A1, C2A1, C3A1 . . . CnA1 and C1B1, C2B1, C3B1 . . . CnB1, respectively, said OR gates C1A, C2A, C3A . . . CnA and C1B, C2B, C3B . . . CnB also having second inputs C1A2, C2A2, C3A2 . . . CnA2 and C1B2, C2B2, C3B2 . . . CnB2, respectively, said output devices B1A, B2A, B3A . . . BnA connected to said first inputs C1A1, C2A1, C3A1 . . . CnA1, respectively, said logic circuit having corresponding respective different outputs connected to said OR gate second inputs.

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