

May 27, 1969

B. H. CARLISLE ET AL.

3,446,985

ELECTRICAL CONTROL CIRCUIT FOR CYCLICALLY OPERATING APPARATUS

Filed Oct. 31, 1966

Sheet 1 of 3

Fig. 1

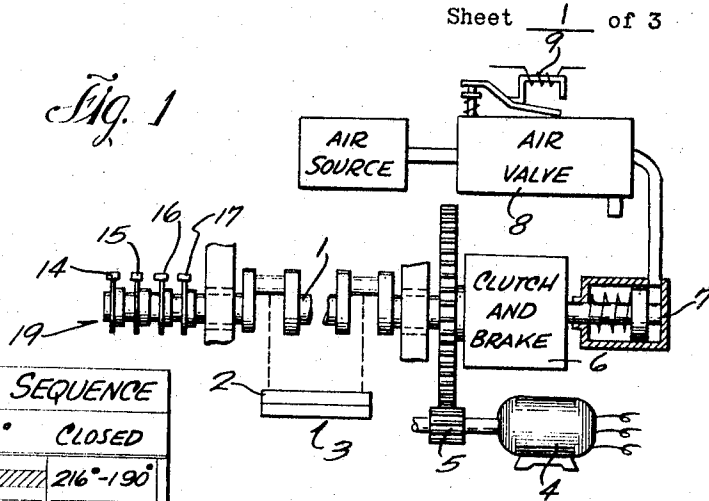


Fig. 3

CAM LIMIT SWITCH SEQUENCE				
SWITCH	90°	180°	270°	CLOSED
LSI 14	///	///	///	216°-190°
LSI 15		///	///	140°-360°
LSI 16		///	///	140°-360°
LSI 17			///	220°-250°

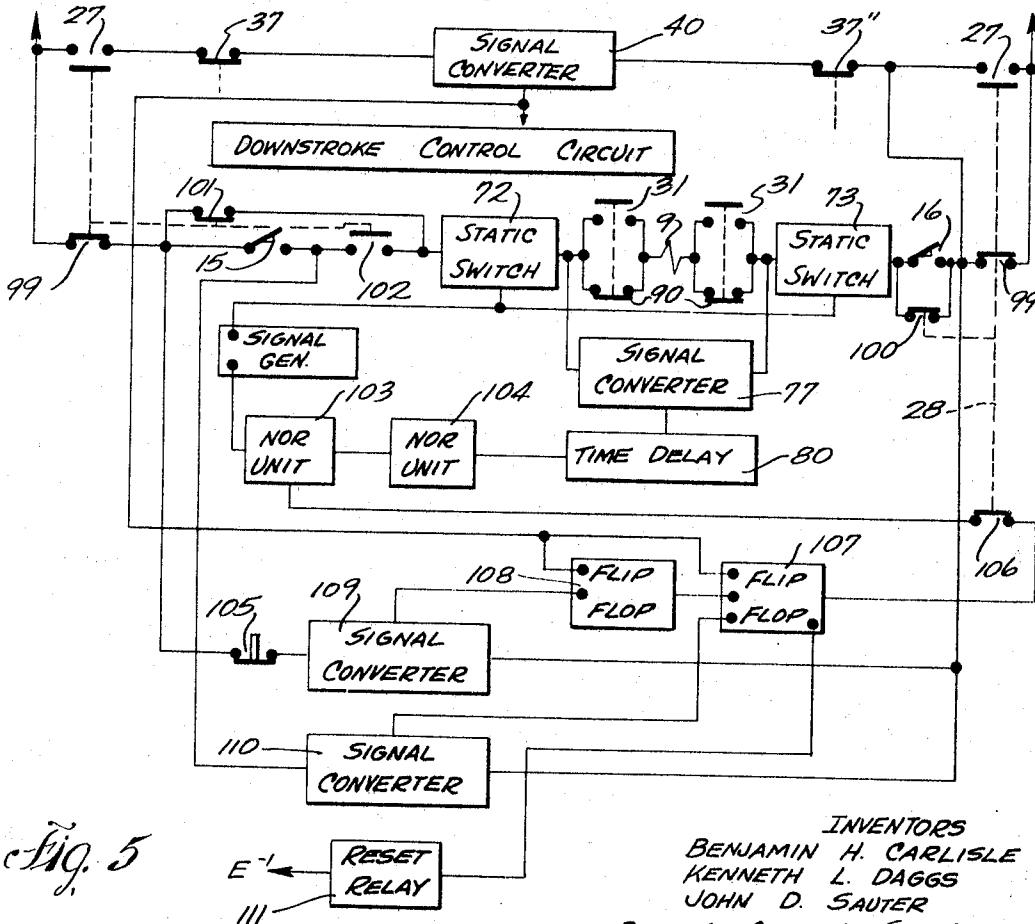


Fig. 5

INVENTORS
 BENJAMIN H. CARLISLE
 KENNETH L. DAGGS
 JOHN D. SAUTER
 BY Andrew & Starke
 ATTORNEYS.

May 27, 1969

B. H. CARLISLE ET AL

3,446,985

ELECTRICAL CONTROL CIRCUIT FOR CYCLICALLY OPERATING APPARATUS

Filed Oct. 31, 1966

Sheet 2 of 3

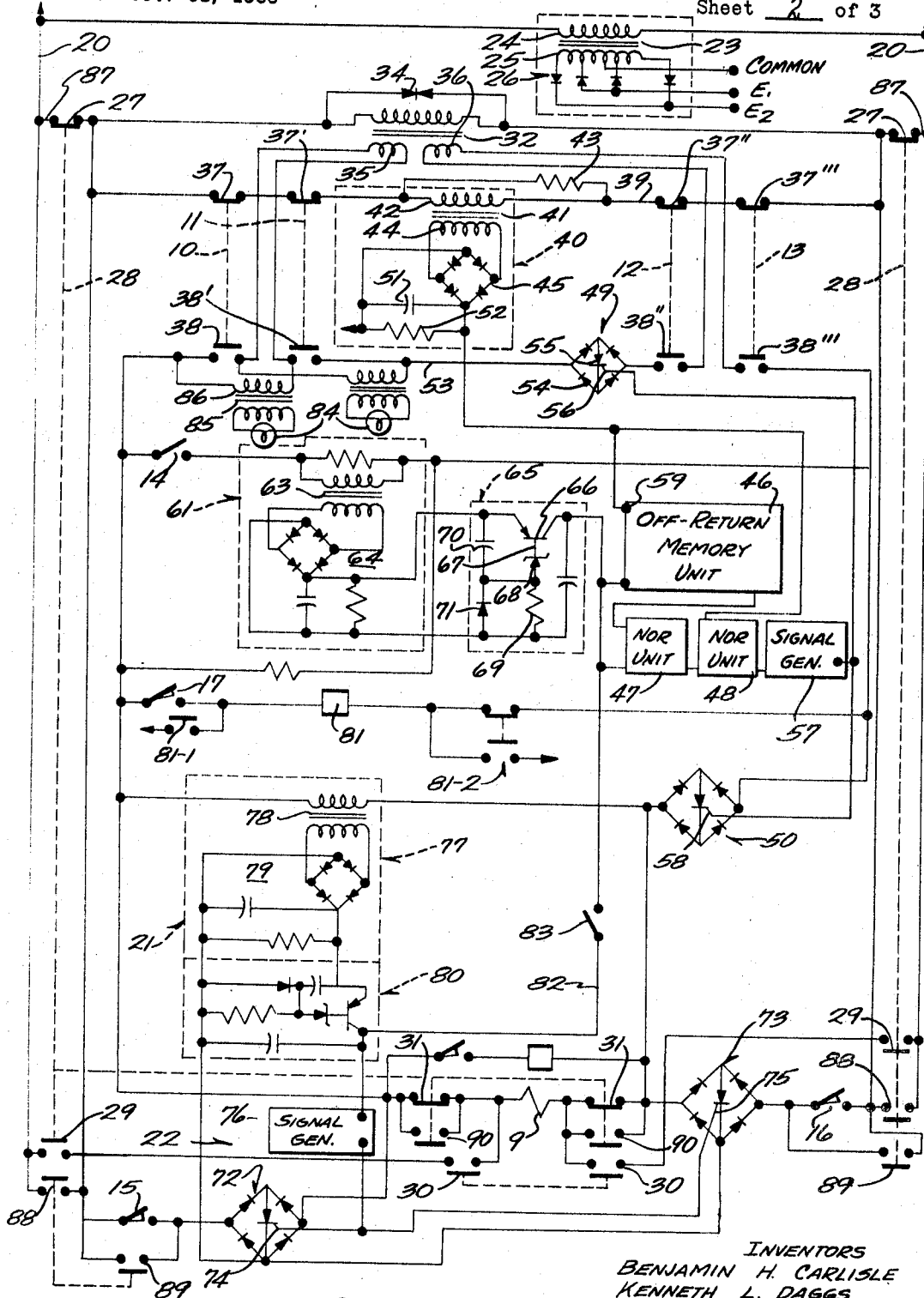


Fig. 2

INVENTORS
BENJAMIN H. CARLISLE
KENNETH L. DAGGS
JOHN D. SAUTER

BY *Andrew & Starks*
ATTORNEYS.

May 27, 1969

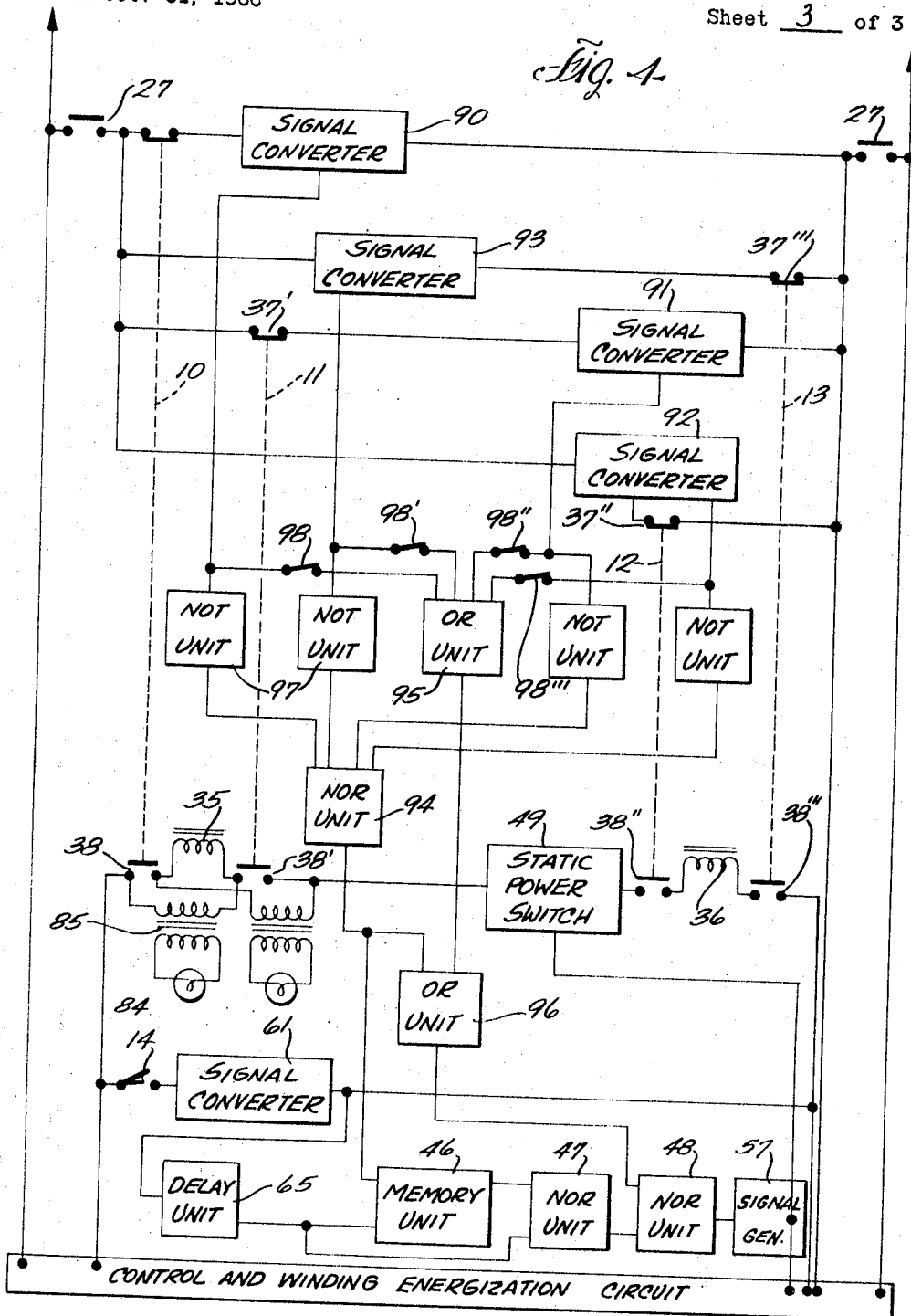
B. H. CARLISLE ET AL

3,446,985

ELECTRICAL CONTROL CIRCUIT FOR CYCLICALLY OPERATING APPARATUS

Filed Oct. 31, 1966

Sheet 3 of 3



INVENTORS
 BENJAMIN H. CARLISLE
 KENNETH L. DAGGS
 JOHN D. SAUTER

BY *Andrew & Starke*
 ATTORNEYS

1

2

3,446,985

ELECTRICAL CONTROL CIRCUIT FOR CYCLICALLY OPERATING APPARATUS

Benjamin H. Carlisle, South Euclid, Kenneth L. Daggs, Euclid, and John D. Sauter, Lyndhurst, Ohio, assignors to The Clark Controller Company, Cleveland, Ohio, a corporation of Ohio

Filed Oct. 31, 1966, Ser. No. 590,637

Int. Cl. H02b 1/24

U.S. Cl. 307—113

30 Claims

ABSTRACT OF THE DISCLOSURE

This disclosure relates to a press control having a solid state anti-repeat control incorporating push button switches and press actuated limit switches. The control circuit includes a split loop with a pair of secondaries connected to push button switches in the two sides of the loop. Diode bridges each having a silicon controlled rectifier are connected to the press winding and between the push button switches and the secondaries. An off-return memory unit in combination with "Nor" circuits provides a trigger to the controlled rectifiers during the downstroke. The memory unit is reset by the press actuate switches.

This invention relates to an electrical control circuit for actuating a cyclically operating apparatus and in particular to such a control circuit for safe operation of a punch press or the like.

In many applications of cyclically operating apparatus, the control operators may be subjected to a dangerous condition as a result of mechanically moving components during a portion of the cycle of operation. For example, punch presses and the like normally require the operating personnel to place their hands and arms in the vicinity of the press dies to feed and remove work members between the press dies, and the like. If the control equipment should malfunction for any reason causing the press to operate with the arms or other components within the dies or if the operator negligently places his hands in between the dies during the downstroke or die closure cycle, a highly potentially dangerous situation occurs.

A highly satisfactory relay control circuit preventing malfunctioning or operation of the press by the operators in a dangerous manner is disclosed in U.S. Patent 3,183,377. As more fully disclosed therein, the control circuit for the punch press or other apparatus includes mechanically actuated push button switches requiring the operator to hold his hands on the push buttons during the dangerous period of the cycle of a punch press and a plurality of sequentially actuated relays interlocked with each other to require cyclical actuation of the push buttons to insure the manual operation of the switches. As disclosed in the above patent, the circuit includes other highly desirable features such as short circuit protection, detection of limit switch malfunction and the like. A key operated switch means is preferably included to permit disconnection of one or more of the operating push button stations, establish a continuous run mode of operation and the like.

The present invention is particularly directed to an improved and novel control solid state or static anti-repeat control circuit incorporating manually actuated mechanical switches or the like and limit switches operated by the apparatus. The logic circuitry for controlling the power circuitry is completely isolated from the power circuitry while maintaining of the power current under direct control of such switches.

The circuit of the present invention provides a com-

pletely ungrounded control and energizing circuit for the drive means during the potentially dangerous operating period of the cycle. Further, in accordance with the present invention, the circuit employs a split loop type circuit with power being supplied to the opposite sides of switches in the loop whereby malfunction due to grounds can only arise by grounding to both sides of the loop.

Although the circuit may be applied to any apparatus, it is particularly useful as a press control and is described herein applied to a press having an electromagnetic control winding for controlling the movement of a press die.

Generally, in accordance with the present invention, the drive control winding is connected to alternate power circuits, one for operation during the downstroke of the press and the other for operation during the upstroke of the press. For added reliability such circuits are simultaneously closed during the die closure period; that is, during the actual working period of the press.

The downstroke or working stroke control and power circuit includes a pair of power sources such as two secondaries of a main input transformer. The secondaries are interconnected by manually operated push button switches having normally open contacts and the drive control winding in series. Static power switches are inserted between the windings and between the normally open push button switches and the drive control winding. The static power switches are triggered devices which normally prevent energization of the drive control winding unless they receive a signal indicating an anti-repeat operation. In a preferred circuit, an off-return memory unit in combination with static switching devices such as "Nor" circuits provides a trigger or an "on" signal to the static switches in the downstroke power circuit. The memory unit is actuated by a first static signal converter connected to the power lines through the normally closed contacts of the operator actuated switches. The memory unit also obtains a signal from a second signal converter connected in circuit by a press operated limit switch which is closed during the greater portion of the cycle and momentarily opened immediately following the downstroke and during the initial portion of the upstroke. The signal converters each have isolation transformers connected in the downstroke power circuit and low voltage secondary windings connected as the input means of the logic circuit.

The static off-return memory unit remembers which of its two inputs was last actuated from the logic circuit signal converters and maintains a related output as long as a signal is applied to such input and until the corresponding signal is removed and a signal applied to the other input. In the normal sequencing, the release of the operator push buttons actuates the first signal converter and sends a reset signal to the memory unit. This changes the output state from that set by the actuation of the limit switch during the upstroke cycle. The resetting of the memory unit again establishes an output signal to the static switches thereby conditioning them for operation.

To insure the operation of the circuit and to check the operation of the limit switch, a further limit switch is actuated shortly after the cyclically opening and reclosing of the first resetting limit switch. This limit switch connects a fault relay or similar device directly across the circuit in the downstroke power circuit of the normally open push button contacts, the secondaries and the static switch and normally open contacts have not been opened or the memory unit reset by actuation of the first limit switch. Voltage applied to the control relay will stop the press in the upstroke.

The upstroke power circuit includes the usual limit switches connected in series with a pair of static power

switches to the opposite side of the main winding. A signal converter is connected to the circuit to be energized as a result of the triggering of the first static switches in the downstroke power cycle and provides a timed output to the triggers of the upstroke power switches or static relays. The third converter provides a turn-on signal conditioning the circuit of the upstroke power circuit which however will not be completed until the upstroke limit switches are actuated by the press itself, preferably just prior to completion of the downstroke cycle. The latter provides slight overlap between the downstroke and the upstroke power circuits to increase the reliability of operation.

The standard circuit can be operated under "hopping" conditions wherein the operator by releasing the push buttons after the die closure and reclosing them before the press completes the full cycle can maintain continuous cyclical operation of the press. Feedback signal means can be readily provided between the memory unit and the running or the downstroke portion of the cycle to prevent "hopping" if desired. In such a case, a first cycle must terminate before the operator initiates a further cycle. Further, the circuit can be provided of course with an overrunning continuous switching circuit whereby it will continuously cycle itself independent of the operation of the operator.

The circuit can also be provided with short circuit protection and indication as well as permitting dummy plug operation.

The drawings furnished herewith show preferred circuitry incorporating the subject matter of the present invention in which the above advantages and features are clearly disclosed as well as others which will be clear from the following description.

In the drawings:

FIG. 1 is a diagrammatic illustration of a press adapted to be controlled in accordance with the present invention;

FIG. 2 is a schematic circuit diagram showing the basic circuitry forming the subject matter of the present invention;

FIG. 3 is a diagrammatic illustration of limit switch conditions during any one cycle of a press unit as shown in FIG. 1;

FIG. 4 is a similar view schematically showing modifications and additions to portions of the circuit to provide push button and short circuit protection and indication; and

FIG. 5 is a schematic circuit showing modifications to provide a continuous run with top stop mode of operation.

Referring to the drawings and particularly to FIG. 1, an air clutch type press drive mechanism is diagrammatically illustrated for purposes of disclosing one possible type of mechanism to which the present invention particularly provides a highly satisfactory control. In the illustrated embodiment of the invention, the press drive mechanism includes a crank shaft 1 mounted to reciprocate a press ram 2 forming a part of a set of dies 3. A motor 4 is connected through a suitable gear train 5 to drive a clutch and brake unit 6 which in turn is coupled to the crank shaft 1. A spring loaded piston cylinder unit 7 is provided to bias the clutch and brake unit 6 into a normally set condition; disengaging the gear train 5 from the crank shaft 1 and applying a positive braking force to the crank shaft. An electromagnetically actuated air valve 8 selectively connects an air source to the piston cylinder unit 7. The electromagnetic air valve 8 includes a control winding 9 which is connected in a control circuit forming the subject matter of the present invention. The winding 9 is normally de-energized and the air valve 8 is then set to exhaust the piston cylinder unit 7. When the winding 9 is energized, the air valve 8 is actuated to apply air to the piston cylinder unit 7, overcoming the force of the spring loading and thereby releasing the brake and completing the clutch connection between the gear train 5 and the crank shaft 1. The resulting rotation of the crank

shaft 1 moves the press ram to close and open the dies 3.

As more fully described in connection with FIG. 2, the illustrated embodiment of the invention is adapted to be operated by a pair of operators and is provided with four push button switch units 10, 11, 12 and 13. The push button units are paired to the right and left side of the press unit with the operators correspondingly stationed to the opposite sides of the entrance to the press unit for removing and inserting workpieces.

The pairs of push button switch units 10-13 are provided to the opposite sides thereof and the operators must hold their hands on such units during the downstroke because of the control circuitry shown in FIG. 2. The production line may have the work moving through the press to the next work station. Additional operators may then be stationed to the opposite side of the press and provided with similar push button switches.

Four cam operated limit switches 14, 15, 16 and 17 are actuated by the press and connected in the control circuit to provide an upstroke circuit and certain check functions. The switches are shown as mounted adjacent operating cams 19 connected to an end of the shaft 1 for simplicity of illustration. The switch conditions during each revolution or cycle of the press are graphically illustrated in FIG. 3.

Referring particularly to FIG. 2, input power to the circuit and particularly for operating of the winding 9 is from a pair of A.C. power lines 20. Connected to the A.C. power lines 20 is a pair of parallel circuits for operating of the winding 9 and consisting of a downstroke power circuit 21 incorporating the structure of switch units 10 through 13 and an upstroke power circuit 22. The latter controls the operation of the press during the ram upstroke independently of the push button switch units 10 through 13 to free the operator's hands for other tasks.

The circuits 21 and 22 include solid state logic circuitry and a logic power transformer 23 is provided having a primary winding 24 connected directly to the power lines 20 and a tapped secondary 25 connected to a suitable diode rectifying circuit 26 providing a pair of low voltage direct current or D.C. outputs for proper biasing of the various solid state components employed in the logic circuitry. The connection of the bias power to the several components is not illustrated in the drawing as such detail will be clear to those skilled in the art and would unduly complicate and confuse the description of the control circuit as such. Of significance however is the fact that the logic power transformer 23 is connected directly to the power lines 20 independent of the connection of the circuits 21 and 22 which are connected thereto by a selector switch 27. This is a safety feature to eliminate any false operation of the circuit due to transient interlock as hereinafter discussed.

The power circuits 21 and 22 are connected to the A.C. power lines 20 by a pair of normally open run contacts 27 of a key operated selector switch 28.

The selector switch 28 also has an inch position at which the run contacts 27 are open and a pair of inch contacts 29 which may be closed to directly connect the winding 9 to the A.C. power lines 20 in series with a pair of manually operable inch button switches 30 to the opposite sides of the winding 9. The latter are manually operated and thus require the operator to place his hands on inch button switches whenever it is desired to move the press slightly. Such is normally employed during the set-up of the press unit and may also be employed if it is necessary to remove the logic control circuitry for maintenance and the like.

Run contacts 31 are also interconnected to the opposite sides of the winding 9 in a paralleled connection to the downstroke power circuit and the upstroke power circuit.

The downstroke power circuit 21 includes a transformer 32 having a primary winding 33 connected to the A.C. power lines 20 between run contacts 27. Selenium rectifiers 34 are connected across the primary winding

33 to provide transient and surge protection by eliminating such spurious signals from the logic circuit. The transformer 32 includes a pair of secondary windings 35 and 36 connected in the downstroke power circuit 21, particularly through the manually operated push button switch units 10-13.

Each of the push button switch units 10-13 is similarly constructed. Switch unit 10 includes a set of normally closed contacts 37 and a set of normally open contacts 38 interconnected in the downstroke power circuit. The contacts of the other switches are identified by similar primed numbers.

The normally closed contacts 37 are series connected in an anti-repeat sensing branch 39 to the opposite side of a signal converter 40. The switch units 10-13 are paired as previously described requiring each operator to employ both hands and the switch units of each pair are connected in circuit on opposite sides of the signal converter 40, as shown.

The illustrated signal converter 40 includes a transformer 41 having the primary winding 42 connected in series with the normally closed contacts 37 of the push button switch units 10-13. A resistor 43 is paralleled with the primary winding 42 to insure sufficient current to actuate the switching structure. The secondary winding 44 of the transformer 41 is connected to a full wave bridge rectifier circuit 45 to provide an output signal which is connected to an interlock memory circuit 46 and to one of a pair of "Nor" circuits 47 and 48. The actuation of circuits 46-48 controls a pair of solid state switches 49 and 50 connected in the downstroke power circuit 21 in series with the winding 9 and the normally open contacts 38-38'.

A capacitor 51 and a resistor 52 are connected in parallel across the D.C. lines of rectifier 45 to provide a slightly filtered D.C. output. The output is only partially filtered to minimize the time constant and permit rapid operation of the circuit components.

The first downstroke solid state power switch 49 is shown connected in an input power switching branch 53 including the normally open contacts 38-38' of push button switches 10-13, inclusive, disposed to the opposite sides of the switch 49 in the illustrated embodiment of the invention. The secondary windings 35 and 36 of the transformer 32 are inserted in the switch branch 53 between the normally open contacts, one to each side of the switch 49. When and only when all of the normally open contacts 38-38' are closed and the switches 49 and 50 are closed, the power is supplied to the winding 9.

Each of the switches 49 and 50 is similarly constructed as a solid state rectifying circuit including four diodes 54 connected in a bridge configuration and having A.C. terminals connected in series with the normally open push button contacts and a thyristor 55 connected across the D.C. terminals. In accordance with well known theory the thyristor is normally nonconducting. A proper signal must be applied to a gate element 56 with the anode of thyristor 55 positive in order to initiate conduction through the thyristor which will then continue to conduct until such time as the current through it drops below the holding current.

The gate 56 is connected by a gate line to a pulse generator 57 which in turn is actuated by the "Nor" circuit unit 48. The pulse generator 57 may be of any suitable variety adapted to establish relatively high frequency repetitive pulse signals; for example, a unijunction oscillator driving an output transistor may be used with a pulse transformer coupling the output of the gate line 57.

The switch 50 corresponds to the switch 49 and has its gate 58 similarly connected to the output of the logic "Nor" unit 48.

The one side of the switch branch 53 is connected in series with the solid state switch 50 to the one side of the winding 9 through the run contacts 31 of the selector switch 28. The opposite side of the switching branch 53

is connected to the main winding 9 in series with the run contacts 31 of the selector switch 28.

Thus, the switches 49 and 50 are controlled from the same source to establish a complete circuit during the downstroke cycle by proper operation of the memory unit 46 and the "Nor" units 47 and 48. The memory unit 46 is schematically shown in block diagram as an off-return memory having a pair of input terminals 59 and 60, one of which is connected to the signal converter 40 and the other of which is connected to a signal converter 61 controlled by the operation of the press and particularly the check limit switch 14. The off-return type memory unit 46 includes an internal unit reset device which will always establish a selected output upon initial application of power at the memory output line or terminal. The off-return memory unit 46 operates under first input received, first served basis. As long as an input signal is maintained at any given input, the output therefore remains the same irrespective of provision of a signal at the other input.

The memory unit thus serves the function of retaining memory as to the last input signal received and maintains a related output as long as the input signal is held or until not only is such input removed but a signal is applied to the opposite input.

As the press unit goes through a cycle, the limit switch 14 is actuated and creates a signal which is fed to the "Nor" circuit 47 and removes the signal from the gates of the thyristors of the switches 49 and 50. The only way such gates can again be energized is by releasing of the push button switches 10-13 to close the contacts 37-37', actuate the signal converter 40 and apply a signal to a off-return memory unit 46 and the "Nor" circuit 48. Further, such action must occur after the press responsive signal of converter 61 has been removed.

The press related signal is established by connection of limit switch 14 in series with signal converter 61 across branch circuit 53 including the pair of secondary windings 35 and 36 and the normally open contacts 38-38'. The signal converter 61 corresponds to the previously described signal converter 40 and includes a transformer 63 and a full wave rectifier-filter 64 producing a slightly filtered pulsating D.C. power. The filtered D.C. output of this branch of the circuit is connected through a solid state timing unit or circuit 65 to provide a signal to the input of the memory unit 46 and the "Nor" circuit 47.

The time delay unit 65 is a special solid state circuit which has been found to provide highly satisfactory response in the circuit.

The timing circuit or unit 65 includes a transistor 66 having its emitter to collector circuit connected in series to the output of the D.C. filtered power supply. The base 67 of the transistor is connected to the return lead by a Zener diode 68 in series with a base resistor 69. A capacitor 70 in series with a blocking diode 71 is connected across the D.C. power lines and thus across the input circuit of the transistor 66. The junction of the capacitor 70 and diode 71 is connected by a lead 72 to the junction of the Zener diode 68 and the resistor 69. The capacitor is connected across the Zener diode 68 in series with the base to emitter junction of transistor 66. Until the capacitor 70 charges to a selected level sufficient to overcome the Zener voltage and the voltage drop in the transistor junction, the transistor 66 is biased off. However, when the voltage rises above this level, the Zener diode 68 breaks down and the transistor conducts providing a delayed output signal to the memory unit 46 and "Nor" circuit 47.

The output of the memory unit 46 and of the time delay circuit or unit 65 are connected as a pair of inputs to the first "Nor" circuit or unit 47, the output of which is connected as the second input to the second "Nor" circuit or unit 48, the other or first input of unit 48 being connected to converter 40. The "Nor" circuits are

both shown in block diagram by the conventional industrial symbol.

Each of the "Nor" circuits is a well known logic device normally employing a transistor with suitable bias and with a pair of inputs. The output is at one state when there is an absence of signals at both inputs and in an opposite state whenever there is a signal at either one or both of the inputs. The "Nor" circuit is employed to detect the simultaneous occurrence of different signals at the two inputs. The logic can be stated: only if there is an input signal at neither of the input terminals will the output at the output terminal change from one selected level to a different selected level.

The operation of the circuit during the downstroke cycle may this be summarized as follows: The downstroke is initiated by the operator simultaneously depressing all of the related push button switch units 10-13. The opening of the normally closed contacts changes the state of the static converter 40 to a zero output level and thus correspondingly changes the one input at the memory unit 46 and at the second "Nor" unit 48. The output of the memory unit 46 goes to a zero output as a result of the signal from the converter 61, which simultaneously supplies a corresponding signal to the first "Nor" unit 47. The output of the first "Nor" unit 47 is at zero at this time as a result of the application of the signal from the static converter 61. Both inputs of the "Nor" circuit are therefore at a zero level and its output changes from zero to the selected trigger output. As a result power is applied to the gates 56 and 58 of the two static switches 49 and 50. Closing of the first static switch 49 completes the circuit between the push button contact 38 and connects the two secondaries 35 and 36 in series and the firing of the second static switch 50 completes the downstroke power circuit to the winding 9. The secondaries 35 and 36 therefore supply power to the winding 9 as long as the push buttons are held depressed to hold the contacts 38-38''' closed. If they are released at any time during the downstroke, the contacts 38-38''' directly open the circuit to the winding.

In this illustrated embodiment of the invention, the pair of limit switches 15 and 16 are closed to complete the upstroke power circuit 22 prior to the completion of the downstroke and during the initial die closure.

The upstroke power circuit 22 includes a pair of static switches 72 and 73 corresponding to the previously described static switches 49 and 50 in the downstroke circuit. Switches 72 and 73 are connected to the opposite sides of the winding 9 and between the respective limit switches 15 and 16 and the run contacts 31 on the opposite side of the winding 9. The gates 74 and 75 of switches 72 and 73 are interconnected to a common signal generator 76 which in turn derives power from a third converter 77 connected in parallel with the winding 9 and the run contacts 31. The converter 77 corresponds to converters 40 and 61 and includes the transformer 78 and rectifier-filter network 79. A time delay circuit 80 corresponding to circuit 65 is connected across the output of the converter 77 to provide a delayed time signal to the gates 74 and 75 of the silicon controlled rectifiers in converters 72 and 73. The upstroke power static switches 72 and 73 are triggered to a conducting state during the downstroke cycle and a gate signal is maintained during the complete downstroke cycle. Consequently, when the limit switches 15 and 16 are closed, a power path is completed through the limit switches 15 and 16, the static switches 72 and 73, the run contacts 31 and the winding 9. This also supplies power to the converter 77.

Immediately following the downstroke cycle, the press actuates the reset limit switch 14 to open the limit switch for a few degrees of the cycle and then closes the switch again. The opening of the switch removes power from the signal converter 61 and thus removes the signal through the time delay circuit 65 from the memory unit 46 and from the "Nor" unit 47.

At the start of the cycle and during the downstroke the output of the "Nor" unit 47 is held at a logic one level as a result of the input signal applied from the memory unit 46 and from the static converter 61. Thus, just prior to start of the cycle, the input signal to the memory unit 46 from converter 40 establishes a corresponding logic one output at the input to the "Nor" circuit 47, which then has a related logic one output. After removal of such converter signal the memory unit 46 maintains such state until the signal from the converter 61 is applied to the memory unit 46 at which time it is set to a logic zero output. The "Nor" unit 47 remains at the logic one level because the set signal to the memory unit 46 is simultaneously applied to the "Nor" unit 47. When limit switch 14 opens, the output changes to a logic zero. This does not change the memory unit 46 which remains at logic zero output but does change the "Nor" unit 47 to a logic one output as both of its inputs are now at logic zero.

The application of the logic one output of unit 47 to the second "Nor" unit 48 changes the output thereof to a logic zero; removing power from the gates 56 and 58 of the power switches 49 and 50. The static switches 49 and 50 are now open circuited and the downstroke power circuit to winding 9 and to converter 77 is open. The winding 9 is now energized only as a result of the closing of the limit switches 15 and 16 and when they are opened the winding 9 is de-energized even if the run buttons have not been released.

Even though limit switch 14 may be again closed, the open switches 49 and 50 prevent formation and application of a signal to the memory unit 46. The only way in which the static switches 49 and 50 in the downstroke circuit can be again triggered to the close circuit condition is through resetting of the memory unit 46 by releasing of the push button switch units 10-13 to close the normally closed contacts 37-37''' and energize the signal converter 40 to apply a reset signal to the memory unit 46.

The control rectifiers of the power switches 49 and 50 may be triggered by a high voltage transient applied to the gate as a result of the change in voltage with time characteristic of such devices. The time delay circuit 65 insures proper sequencing and further prevents transients such as noise which may appear at the output of the static converter 61 from being passed into the logic circuit.

The time delay circuit 80 in the upstroke firing circuit protects the circuit from the static switches 72 and 73 being "locked in" as a result of the breakdown of the thyristors in the circuit with a change of voltage and time characteristic which may be established in the event of power failure, emergency stop or the like during the upstroke cycle.

The illustrated embodiment of the invention further is shown with a fault relay 81 connected in series with the fault checking limit switch 17 directly across the normally open push button branch circuit 53 including the normally open push button contacts 38-38''' and the one static switch 49. Switch 17 is closed shortly after completion of the downstroke cycle. The relay is connected to be energized if the static switches 49 and 50 in the downstroke power cycle have not been de-energized or opened by the limit switch 14 opening. The contacts of the fault relay 81 are connected in the main power supply to disconnect the power from the circuit and stop the press in the upstroke cycle in the event of energization thereof. This requires that the circuit of limit switch 14 function properly to reset the static switches to the open state in each cycle.

The known "hopping" of a press can be accomplished with this invention by releasing of the push button switch units 10-13 following the closing of the limit switches 15 and 16 and leaving them open until after the fault relay limit switch 17 has been closed and reopened normally at about 270°. The operators need not wait until the completion of the cycle but can reclose or reactuate the switches prior to the completion of the cycle to insure im-

mediate initiation of the second cycle. The push button units 10-13 cannot be reactivated until the opening of the fault limit switch 17 because the static power switches would be reset and the fault relay 81 energized.

Further, the buttons can be held closed however during the complete stroke without indication of any fault. In this instance, the reset limit switch operates to open the static power switches.

Further, the illustrated circuit includes a means to prevent "hopping" operation. A signal line 82 is connected to the output of converter 77 for the upstroke static power switches and to the memory unit 46.

In the illustrated embodiment of the invention, a manually operated switch 83 is shown in the line to permit selective provision of "hop" prevention. Normally the circuit will either be wired for "hop" prevention or such wiring is completely eliminated. The switch illustration is provided for convenience of illustrating the concept in a single circuit.

Whenever the winding 9 is energized, the signal converter 77 is energized and an output signal impressed on the gates of the silicon controlled rectifiers in the upstroke static switches 72 and 73 and simultaneously to the memory unit 46. This holds the memory unit 46 in the set state and prevents resetting as a result of opening and closing of limit switch 14. Consequently, if the push button units 10-13 are released, the signal converter 40 is energized and applies a signal to the memory unit. However, the memory unit 46 as previously noted is responsive to a first received and first served basis and consequently the signal from the converter 40 has no effect until such time as the signal from the line 82 is removed. This can only occur after the upstroke limit switches 15 and 16 have opened.

In the present invention, dummy plug indicating lights 84 are provided for indicating when one of the pair of switch units 10 and 12 or 11 and 13 is dummy plugged. It may be desired to dummy plug at least one station; for example, switches 10 and 12 might be dummy plugged. In this condition the contacts 37 and 37' and 38 and 38' are held closed through the usual dummy plug. In essence these two circuits are then disconnected from the circuit and the press is controlled during the power downstroke cycle completely by the other pair of switch units 11 and 13. The indication is visually displayed by the continued illumination of the appropriate lamp 84 associated with the switch unit 10, as follows.

Switch unit 10 is described in detail with the corresponding elements for switch unit 11 identified by corresponding prime numbers. The indicating lamp 84 is connected in circuit through a suitable step-down transformer 85 having a primary winding 86 connected in parallel with the normally open contacts 38 of push button switch unit 10 and the secondary winding 35 of the power transformer 85.

The lamp 84 is of a high impedance variety and consequently does not provide an effective short circuit across the normally open contacts 38. Consequently, the winding 9 cannot be energized with a single run button switch unit; for example, only switch 11 or 13, even though the other switch units 10 and 12 are dummy plugged.

Additional stations are generally provided where dummy plugs are used. In a four button control having four stations, four contacts will be provided to either side of the static converter 40 and the switch 49. The normally open contacts of the additional two stations would be connected to the winding 36 as now shown for units 12 and 13 and dummy plug indicators similarly connected to such contacts and winding 36.

In summary, in the illustrated embodiment of the invention, the control circuitry essentially eliminates all conventional electromagnetic relays while maintaining the mechanical pilot devices such as the push button switch unit and the press operated cam limit switches.

Thus, the control of the present invention reliably

responds over a wide ambient temperature range and a wide range of press speeds. A commercial design covered a range of 5 to 135 cycles or revolutions per minute. The control circuitry and particularly the logic and downstroke control is controlled by the highly desirable anti-repeat actuation of the push button controls and employs a completely ungrounded system; thereby minimizing any danger of malfunctioning or operation of energization of the winding due to an accidental ground.

The fault relay 81 shown in the illustrated embodiment of the invention is preferably employed as a result of the past development of fault checking circuitry and the customer acceptance occasioned thereby. If desired, suitable reliability control of the static components may eliminate the necessity of such relay. The fault relay 81 will stop the device in the upstroke cycle and further cannot be reset until the fault is cleared.

In addition to the above the circuit may be further modified to establish a continuous run condition by provision of an appropriate selector switch 28 having continuous run contacts as shown in FIG. 3.

In the continuous run connection, the downstroke power transformer 32 is not connected to power lines 20 through the run contacts 27 which are disconnected as by removal of leads 87 between the respective contacts 27 and lines 20. Continuous run contacts 88 are provided in parallel with the normal connection run contacts 27 and thus similarly supply power. Further, a set of interlocked run contacts 89 are connected in parallel with the limit switches 15 and 16 and a third set of continuous run contacts 90 connected in parallel with the run contacts 31 to the opposite sides to the winding 9. Consequently, with the key operated selector switch 28 in the continuous run position, a power circuit is established to supply the winding 9 through the upstroke static power switches 72 and 73. Power is supplied through the continuous run contacts 88 to the push button circuitry of the downstroke power cycle directly through the downstroke power transformer 32. Thus, initial actuation of switch units 10-13 will operate in the same manner as previously described to trigger the downstroke switches 49 and 50 and therethrough the upstroke power switches into conduction and establishing the above continuous run circuitry. As long as the continuous run contacts 88, 89 and 90 are closed, power continues to flow through the power switches 72 and 73 to hold the winding energized independently of the push button switch units 10-13.

In this mode of operation the material will be automatically fed into and removed from the press such that it can safely run continuously after its initial operation is started.

The circuit of FIG. 4 discloses modifications made to the circuit of FIG. 3 to provide run button and short circuit protection and indication. The several logic elements are shown by approximately labeled block symbols for simplicity and clarity of explanation in view of the showing in the previous embodiments and the standard or known design of such other components.

Referring particularly to FIG. 4, each of the push button switch units 10-13 and particularly the normally closed contacts 37-37' are connected in separate parallel circuit with separate converters 90, 91, 92 and 93 in the respective parallel branches. The output of each of the several converters 90-93 is similarly connected to control the memory unit 46 and the "Nor" units 47 and 48 through a solid state interlock circuit including a four input "Nor" unit 94 interconnected to the input of the line to the memory units and to the "Nor" unit 48. The circuit further includes a pair of "or" units 95 and 96 connected in circuit to the second "Nor" circuit.

Each of the static converters 90-93 is similarly connected in circuit and consequently that for switch unit 10 is described in detail. The output of the static converter 90 is connected in series with a "not" unit 97 to one of the inputs of the four input "Nor" units 94. The output of the

"Nor" unit 94 is connected to the reset input of the memory unit 46 and to one input of the "or" unit 96. The static converter 90 further has its output connected through a normally closed manually operated dummy plug switch 98 as an input to the "or" unit 95 which is provided with four inputs, one for each of the static converters 90-93. The output of the "or" unit 95 is connected as a second input to the "or" unit 96, the output of which is connected as an input to the "Nor" unit 48 for controlling of the downstroke power static switches 49 and 50.

With all of the push buttons connected to control the circuit, the switches 1, 2, 3 and 4 will be closed. Under these conditions with the push buttons released, the converter simultaneously applies signals to the corresponding "not" circuits which remove the signal from the "Nor" circuit 94. Consequently the "Nor" circuit will have zeroes at all related inputs and a logic one is applied via the output line to the memory unit 96 and to the "or" unit 95. The "or" unit operates in response to any one input to establish an output to the other "or" unit 96 which will also have received a signal from the "Nor" unit 94 and consequently provide a signal to the "Nor" unit 48.

When the push button switches 10-13 are actuated, the converters 90-93 are de-energized, the outputs removed from the "not" units 97 and the "or" unit 95. The "not" units now operate to remove the signal from the "Nor" unit 94 and therefore from the memory unit and the "or" unit 48, as in the previous embodiments. Thus, without dummy plugs provided the circuit operates generally in the same manner as that set forth with respect to FIG. 3.

If a switch unit 10-13 is dummy plugged, the corresponding indicating lamps 84 are continuously illuminated to indicate such condition. Further, the related switches 98-98''' must be opened to remove the converter circuit from the "or" unit 95. If the related selector switches 98-98''' are left closed, the converter output which is maintained transmits signals to the "or" unit 95 establishing a logic one to the second "or" unit 96 which in turn establishes a logic one to the "Nor" unit 48 and positively prevents setting of the "Nor" unit in a condition to energize the static switches 49 and 50. With the circuit dummy plugged, the normally closed contacts 37-37''' of the related dummy plug switch unit remain closed to maintain the converter output signal. The selector switches 98-98''' permit effective removal of such signal. Although the signal is maintained at the "not" unit 97, there is no change in the operation as only one of the circuits has to transmit a signal to properly actuate the "Nor" unit 94.

This same circuit provides protection against shorted contacts which would permit operation by the operator depressing only one of the switches. Thus, assume the contacts of switch unit 10 are shorted due to an accident or the like. The circuit could not become energized until the other switch units 11-13 are actuated. Operation thereof would complete the circuit to the winding 9. It however creates an unsafe condition since the one hand of one operator is free. However, in the illustrated circuit, the closed contacts of the shorted switch unit 10 provide a signal to the "or" unit 95 through the selector switch 98 to prevent energization of the static relays 49 and 50 as previously described. Consequently, the circuit will not function and the press will not operate.

If the operator should actuate the push button with the sorted contact, the press operates in the normal manner as heretofore briefly discussed. Since the operator has actuated both of the push button switches, a safe condition is established and consequently there is no reason to prevent operation of the press.

The circuit can be further provided with a continuous run with top stop mode, as shown in FIG. 5 wherein only the modification to FIG. 2 is shown for purposes of simplicity of illustration.

In FIG. 5, continuous run contacts 99 are connected similar to that of contacts 88 shown in FIG. 2. Contacts 100 bridge the limit switch 16. Continuous run contacts 101 bridge the limit switch 15 and a set of run contacts 102 which open the inner side of the circuit between the limit switch and contacts 101. Contacts 101 provide power to the winding 9 in continuous mode while leaving switch 15 operating as hereinafter described.

The signal inverter 77 for controlling static switches 72 and 73 is connected thereto through a pair of "Nor" units 103 and 104. The input from the static converter 77 to the first "Nor" unit 104 establishes a logic zero to the "Nor" unit 103 which however remains at a logic zero output unless a logic zero input is supplied thereto. The second input is connected into the circuit to be selectively controlled through a top stop switch 105 for continuous mode operation or through limit switch 15 for a top stop mode of operation when switch 105 is opened. The second input of the "Nor" unit 103 is connected through a set of continuous run contacts 106 forming a part of the selector switch 28 to the output of a flip-flop logic unit 107 which has its input connected in circuit to the top stop switch 105 through a second flip-flop logic unit 108 and to limit switch 15.

The top stop push button switch 105 connects a signal converter 109 to the power lines in series with run contacts 99 of selector switch 28, as shown. The output of the signal converter 109 is connected to flip-flop unit 108 having its output connected to the flip-flop unit 107. The flip limit switch 15 similarly connects a converter 110 to the power lines 20 in series with contacts 99. The converter 110 has its output connected to flip-flop unit 107.

Both of the flip-flop units 107 and 108 have inputs connected in common to the main signal converters 40 associated with the normally closed push button contacts 37 and 37''. The output of the signal converter 40 is used to reset the flip-flop unit such that the push button units must be actuated to initiate a continuous mode operation.

This provides as in the previously described embodiments energization of the static switches which as a result of the closed continuous run contacts a power path through the static switches and the associated signal converter. Further, the signal established through the top stop switch 105 energizes the associated signal converter 109 to trigger the flip-flop units 107 and 108 and establish a zero input to the "Nor" unit 103. As a result, the output of the "Nor" unit 103 is a logic one to hold a positive trigger signal on the static switches 72 and 73 such that there is continued energization of the winding 9.

When the top stop switch 105 is opened, the signal converter 109 is de-energized and cannot energize or actuate the flip-flop units 108 and 107 to provide the necessary logic zero signal to the "Nor" unit 103 and consequently the static switches 72 and 73 will not be actuated.

The winding 9 is energized through the downstroke power circuit as shown in FIG. 3 until limit switch 15 closes. The closing of the limit switch 15 generates a signal through the signal converter 110 which actuates the second flip-flop unit 107. It thus provides an alternate trigger signal during the upstroke period when the limit switch 15 is held closed. At the top of the stroke, the switch 15 opens, removes power from the signal converter 40. The flip-flop unit 107 is directly reset by the signal from signal converter 40; thereby removing power from the static switches 72 and 73 to stop the press at the top of its stroke or cycle.

Additionally, a reset relay may be interconnected as shown between the logic power supply, shown in FIG. 3 and the flip-flop unit 107 to provide loss of voltage reset.

The present invention thus provides a highly reliable and safe control for a press unit or the like wherein the several functional requirements and operating modes may be provided.

Various modes of carrying out the invention are contemplated as being within the scope of the following

claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention.

We claim:

1. In a machine control circuit for a manually controlled machine and employing manually operated switches, each switch having normally closed and normally open contacts, a pair of switches being provided for each operator, the improvement in the circuit connection of a machine drive control means to a power source means through said switches comprising,
 - a solid state signal converter means having an input means connected in a branch circuit with said normally closed contacts and having an output means,
 - a partial cycle power circuit loop including in series connection a first static switch connected between a pair of power connection means and the normally open contacts of said manually operated switches for the same operator with the drive control means in series with a second static switch connected across said normally open contacts and said first static switch, said static switches each having a signal input means to close the static switches,
 - a machine actuated limit switch, said limit switch being actuated during a cycle of the machine,
 - a second solid state signal converter means having an input means connected in series with said machine actuated limit switch and having an output means,
 - a solid state memory unit having a pair of input means, one of said pairs of input means being connected to the output means of the first solid state signal converter means and the second of said pairs of input means being connected to the output means of said second signal converter means,
 - a solid state switching means having a plurality of input means connected to the output means of the memory unit and to the output means of the first and second signal converter means and having an output means connected to the signal input means of said first and second static switches whereby said manually operated switches must be actuated from the normal position to actuate the control means and released prior to a subsequent actuation of the control means.
2. The machine control circuit of claim 1 wherein said memory unit is an off-return memory unit such that said static switches are turned off by a power failure and remain off until said memory unit is reset by return of the manually operated switches to the normal position.
3. The machine control circuit of claim 1 wherein said power connection means includes a transformer having a pair of secondary windings connected one to each side of said first static switch to provide alternating current power for energizing said control means,
 - said static switches including triggered means and conducting a half cycle of said alternating current power when triggered and,
 - said solid state switching means having a pulse generator controlled by said memory unit to produce a pulse train having a repetition rate substantially greater than the frequency of said alternating current power.
4. The machine control circuit of claim 1 having a time delay means connected to the output of the second converter means and the input of the memory unit and the solid state switching means.
5. The machine control circuit of claim 1 having a fault sensing means selectively connected across the portion of the circuit including the power connection means and the first static switch to sense the state of said static switches.
6. The machine control circuit of claim 1 including a fault sensing means, a fault check limit switch actuated by the machine and connected in series with the fault sensing means across the circuit loop in parallel with the drive control means and the second static switch, said fault check limit switch being closed only after said first

named limit switch has been operated for a selected period.

7. The machine control of claim 1 wherein said first limit switch is opened for a few degrees at the end of the cycle of the power circuit loop and when closed to turn off said static switches, a fault check limit switch, a fault relay means connected in series with said limit switch across the loop circuit in parallel with drive control means and the second static switch, said fault check limit switch being closed for a few degrees of the cycle and after said first limit switch has been opened and closed.

8. The machine control circuit of claim 1 wherein each of said signal converters includes an isolation transformer having a separate secondary and a full wave rectifier connected to the secondary, a resistor-capacitive filter network to produce a partially filtered direct current signal connected to the memory unit, and a time delay unit connected between the second signal converter and the memory unit and the switching means.

9. The machine control of claim 1 wherein each of said converter means includes a transformer having a primary winding connected in an input power circuit by the corresponding switches and having a secondary winding and a rectifying means connected to the secondary winding to provide a low voltage direct current control signal, and

said memory unit and said switching means being solid state logic devices responding to the direct current voltage levels at the respective input means.

10. The machine control of claim 9 wherein said memory unit is an off-return memory unit and said switching means includes a pair of "Nor" logic units, a first of said "Nor" logic units having a pair of input means connected respectively to output means of the second converter means and to the memory unit, and the second of said "Nor" logic units having a pair of input means connected respectively to output means of the first "Nor" unit and the first converter means, said second "Nor" logic unit having output means connected to the first and second static switches.

11. The machine control of claim 9 having dummy plug indicating means connected across one of said secondaries in series with a set of normally open contacts of the manually operated switches, said indicating means including impedance means sufficient to prevent a current flow therethrough of magnitude sufficient to energize said drive control means.

12. The machine control of claim 11 wherein said indicating means are high impedance lamps.

13. The machine control of claim 1 wherein each of said signal converter means includes a transformer-rectifier assembly to provide a pulsating direct current signal when the corresponding switches are closed to apply power to the assembly,

a time delay unit connected to the output of the second signal converter means,

said static switches are triggered devices adapted to conduct once triggered until the current decreases there-through and drops below a minimum holding current level,

said memory unit is an off-return memory unit, said switching means includes a pair of "Nor" logic units, the first of the "Nor" logic units having a pair of input means connected respectively to the output means of the memory unit and said time delay unit and the second "Nor" logic unit having a pair of input means connected to output means of the first signal converter means and the first "Nor" logic unit, and

a pulse generator having an input means connected to output means of the second "Nor" logic unit and having an output means connected to the first and second static switches.

14. The machine control of claim 1 having a second

15

partial cycle circuit loop including said drive control means and third and fourth static switches connected one each to the opposite sides of the control means and a pair of machine actuated limit switches connected one each in series with the last named static switches and a power connection means, said third and fourth switches each having signal input means to close the switches, and a third solid state signal converter means having an input means connected in circuit to be energized whenever the drive control means is energized and an output means connected to the signal input means of the third and fourth static switches.

15. The machine control of claim 14 having means connecting the output of said third signal converter means to said memory unit to prevent setting of the memory unit during the period said second and third limit switches are held closed.

16. The machine control of claim 14 wherein said second and third limit switches are closed prior to actuation of the first limit switch.

17. The machine control of claim 14 having selector switch means connected between a main power supply means and the two circuit loops and including continuous run contacts connected to establish an automatic recycling of the machine in response to initial establishment of the first power circuit loop.

18. The machine control circuit of claim 14 including a selector switch means having "run" contacts connected to supply power to said circuit loops and having "continuous run with top stop" contacts to supply power to said circuit loops and to bypass said pair of limit switches, top stop control switching means being connected between said third signal converter means and said third and fourth static switches and circuit means selectively connecting said switching means to receive a continuous holding signal through continuous run contacts and through the run contacts and one of said pair of limit switches.

19. The machine control circuit of claim 18 wherein said top stop control switching means includes a first stop signal converter connected in circuit through a stop control switch and said continuous run contacts, a second stop signal converter connected in circuit through a limit switch and the continuous run contacts, a pair of flip-flop logic units having reset input means connected to the first signal converter means, the first flip-flop unit having a second input means connected to the first stop signal converter and the second flip-flop unit having a second input means connected to the first flip-flop unit and a third input means connected to the second stop signal converter, said second flip-flop unit having an output means, a pair of "Nor" logic units, the first of the "Nor" logic units being connected to the third signal converter means and the second of the "Nor" logic units being connected to the first "Nor" logic unit and to said second flip-flop unit.

20. The machine control circuit of claim 14 having a time delay means connected between said third signal converter and the third and fourth static power switches.

21. The machine control circuit of claim 1 wherein individual signal-converters are provided for each of the normally closed contacts of said manually operated switches, logic circuit means interconnect the outputs of said individual signal converters to produce a pair of output means connected to the memory unit and to the solid state switching to prevent operation of said static switches if both sets of contacts of any one manually operated switch are closed, and having switch means to selectively disconnect the signal converters from one of said pair of output means to permit operation of said static switches with both sets of contacts of a manually operated switch closed.

22. The machine control circuit of claim 21 having dummy plug indicating means connected in circuit with the power connection means and a related set of normally open contacts of a manually operated switch.

16

23. The machine control circuit of claim 1 wherein said solid state switching means includes a pair of "Nor" logic units, the first "Nor" logic unit being connected to the memory unit and to the second signal converter means and the second "Nor" logic unit being connected to the first "Nor" logic unit and the first signal converter means, said first signal converter means including separate signal converters for each of said normally closed contacts of the manually operated switches, a four input "Nor" logic unit having output means connected to the memory unit, a "not" logic unit connected between each of said separate signal converters and a corresponding input of the four input "Nor" logic units, a four input "or" logic unit, switch means connecting the "or" logic unit to said separate signal converters and two input "or" logic units connected to said first "or" logic unit and to the four input "Nor" logic units and to the second "Nor" logic unit of the solid state switching means.

24. The machine control circuit of claim 23 wherein the pair of power connection means are windings of a transformer and said windings are connected being the normally open contacts of two manually operated switches, and dummy plug indicating means are provided including separate means connected across the corresponding normally open contacts and the one winding.

25. The machine control circuit of claim 23 wherein said separate means includes a transformer and a lamp.

26. A cyclically operable machine control having a portion of each cycle controlled by a plurality of manually operable switches having normally open contacts and normally closed contacts, comprising

a transformer having a primary winding means and a pair of secondary windings,

an energizing circuit including a semiconductor switch means with one of said secondary windings and one of said normally open contacts of said switches connected in series to one side of the switch means and the second of said secondary windings and the second of said normally open contacts to the opposite side of said switch means, said energy circuit having an output means for controlling a machine, and

means connected in circuit with said normally closed contacts and said semiconductor switch means to require cyclical actuation of said manually operated switches to cyclically operate the machine.

27. A cyclically operable machine control having a portion of each cycle controlled by a plurality of manually operable switches having normally open contacts and normally closed contacts, comprising

an energizing circuit including a power source and the normally open contacts of said switches connected in series with a semiconductor static switch means, a first signal source connected in circuit with the normally closed contacts of said manually operated switches,

a second signal source connected in circuit with a machine actuated switch and said normally open contacts, and

an off-return memory unit having an output connected to control the semiconductor static switch means and having a pair of input means connected one each to said signal sources, said first signal source resetting the memory unit to establish a firing signal on said static switch for firing said semiconductor switch means upon closing of said normally open contacts and said second signal source setting the memory unit to remove said firing signal and turning off said semiconductor switch means.

28. The machine control of claim 27 having a fault sensing means connected in circuit to periodically sense the voltage on the static switch means to check the status of said switch means and insure turn-off of said switch means by said memory unit.

29. The machine control of claim 27 wherein the power

17

source is alternating current power and each of said signal sources is a transformer-rectifier assembly to provide an isolated direct current control signal to the memory unit and the static switch means for controlling the alternating current power in said energizing circuit.

30. The machine control of claim 27 wherein the power source is alternating current power and each of said signal converters includes a transformer-rectifier assembly establishing a direct current output having an appreciable ripple content, a transistor has output terminal means connected in series with the assembly of the second source to the memory unit and the switch means, said transistor having input terminal means connected in series with a Zener type diode to the assembly of the second source, and a voltage dividing network connected to the assembly of the second source and including a capacitive means connected across the input means and the diode to establish a delay in the transmission of the signal from the second signal source in response to closing of the corresponding machine actuated switch.

5

10

15

20

18

References Cited

UNITED STATES PATENTS

2,798,170	7/1957	Carlisle	307—112
2,859,355	11/1958	Heiberger	307—112 X
2,888,576	5/1959	Giboney et al.	307—112 X
2,905,838	9/1959	King et al.	307—112
2,966,979	1/1961	Zarling	192—131
3,103,270	9/1963	Tilbury	192—131
3,260,898	7/1966	Jones	317—135
3,311,794	3/1967	Holland et al.	307—113 X

ROBERT K. SCHAEFER, *Primary Examiner.*

T. B. JOIKE, *Assistant Examiner.*

U.S. Cl. X.R.

192—131; 317—135; 328—7

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,446,985

May 27, 1969

Benjamin H. Carlisle et al.

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

Column 6, line 33, "a" should read -- the --. Column 7, line 15, "this" should read -- thus --; line 41, "this" should read -- the --. Column 10, line 18, "circiut" should read -- circuit --; line 55, "approximately" should read -- appropriately --. Column 12, line 3, after "bridge" cancel "the". Column 14, line 5, "when" should read -- then --. Column 16, line 74, cancel "source is alternating current power and each of said signal".

Signed and sealed this 21st day of April 1970.

(SEAL)

Attest:

Edward M. Fletcher, Jr.

Attesting Officer

WILLIAM E. SCHUYLER, JR.

Commissioner of Patents