EMBEDDED WAVEGUIDE DETECTORS

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ABSTRACT
A method of fabricating a detector that involves: forming a trench in a substrate, the substrate having an upper surface; forming a first doped semiconductor layer on the substrate and in the trench; forming a second semiconductor layer on the first doped semiconductor layer and extending into the trench, the second semiconductor layer having a conductivity that is less than the conductivity of the first doped semiconductor layer; forming a third doped semiconductor layer on the second semiconductor layer and extending into the trench; removing portions of the first, second and third layers that are above a plane defined by the surface of the substrate to produce an upper, substantially planar surface and expose an upper end of the first doped semiconductor layer in the trench; forming a first electrical contact to the first semiconductor doped layer; and forming a second electrical contact to the third semiconductor doped layer.
EMBEDDED WAVEGUIDE DETECTORS


TECHNICAL FIELD

[0002] The invention generally relates to optical detectors and methods of fabricating such detectors.

BACKGROUND

[0003] To build an optical signal distribution network within a semiconductor substrate, one needs to make good optical waveguides to distribute the optical signals, and one needs to fabricate elements that convert the optical signals to electrical signals in order to interface with other circuitry. Extracting the optical signals can be accomplished in two ways. Either the optical signal itself is extracted out of the waveguide and delivered to other circuitry that can convert it to the required form. Or the optical signal is converted into electrical form in the waveguide and the electrical signal is delivered to the other circuitry. Extracting the optical signal as an optical signal involves the use of mirrors, gratings or couplers within the waveguides, or other elements that function like these devices. The scientific literature has an increasing number of examples of technologies that can be used to construct such devices. Extracting the optical signal as an electrical signal involves the use of detectors within the waveguide, i.e., circuit elements that convert the optical signal to an electrical form. The scientific literature also has an increasing number of examples of detector designs that can be used to accomplish this.

[0004] The challenge in finding the combination of elements that produces an acceptable optical distribution network becomes greater, however, when one limits the frame of reference to particular optical signal distribution network designs and takes into account the practical reality that any such designs should be relatively easy to fabricate and financially economical.

[0005] The combination of silicon and SiGe alloys (e.g., Si$_x$Ge$_{1-x}$) has attracted attention as useful combination of materials from which one might be able to easily and economically fabricate optical signal distribution networks. With SiGe alloys it is possible to fabricate waveguides in the silicon substrates. The index of refraction of a SiGe alloy is slightly higher than that of silicon. For example, a SiGe alloy with 5% Ge (i.e., Si$_{0.95}$Ge$_{0.05}$) has an index of refraction of about 3.52 while crystalline silicon has an index of refraction that is less than that, e.g., about 3.50. So, if a SiGe alloy core is formed in a silicon substrate, the difference in the indices of refraction is sufficient to enable the SiGe alloy core to contain an optical signal through internal reflections. Moreover, this particular combination of materials lends itself to the use of conventional silicon based semiconductor fabrication technologies to fabricate the optical circuitry.

[0006] Of course, for such a system to work as an optical signal distribution network, the optical signal must have a wavelength to which both the Si and the SiGe alloy are transparent. Since the bandgap energy of these materials is approximately 1.1 eV, they appear transparent to optical wavelengths having a wavelength greater than 1150 nm. A further reduction in bandgap energy caused by use of a SiGe alloy rather than pure Silicon, and higher temperature operation as high as 250°C may further require the wavelength be longer than 1200 nm or even 1250 nm for very low absorption loss (approximately 1 dB/cm or less). But, the transparency of these materials to optical signals having those wavelengths brings with it another problem. These materials are generally not suitable for building detectors that can convert the optical signals to electrical form. To be a good detector, the materials must be able to absorb the light in a manner so as to create useful charge that can be detected electrically. That is, the optical signal must be capable of generating electron transitions from the valence band to the conduction band within the detector to produce an electrical output signal. But the wavelengths greater than 1150 nm are too long to produce useful absorption by electron transitions in silicon, or in Si$_{0.95}$Ge$_{0.05}$ alloys at room temperature. At a wavelength of 1300 nm, the corresponding photon energy is about 0.95 eV, well below the room temperature bandgap of silicon and Si$_{0.95}$Ge$_{0.05}$ and consequently well below the amount necessary to cause transitions from the valence band into the conduction band.

SUMMARY

[0007] In general, in one aspect, the invention features a method of fabricating a detector. The method involves: forming a trench in a substrate having an upper surface; forming a first doped semiconductor layer on the substrate and in the trench; forming a second semiconductor layer on the first doped semiconductor layer and extending into the trench, the second semiconductor layer having a conductivity that is less than the conductivity of the first doped semiconductor layer; forming a third doped semiconductor layer on the second semiconductor layer extending into the trench; removing portions of the first, second and third layers that are above a plane defined by the surface of the substrate to produce an upper, substantially planar surface and expose an upper end of the first doped semiconductor layer in the trench; forming a first electrical contact to the first semiconductor doped layer, and forming a second electrical contact to the third semiconductor doped layer.

[0008] Other embodiments include one or more of the following features. Forming the first and second doped semiconductor layers on the substrate involves depositing silicon. Forming the second semiconductor layer on the first doped semiconductor layer involves depositing a SiGe alloy. Depositing the first, second, and third layers involves epitaxially depositing. Removing involves removing by chemical mechanical polishing.

[0009] In general, in another aspect, the invention features another method of fabricating a detector. The method involves: forming a trench in a substrate having an upper surface; forming a first semiconductor layer on the substrate and in the trench; forming a second semiconductor layer on the first doped semiconductor layer and extending into the trench; forming a third semiconductor layer on the second semiconductor layer and extending into the trench, wherein the second semiconductor layer absorbs light of wavelength $\lambda$, and the first and third semiconductor layers transmits light of wavelength $\lambda$; removing deposited materials that are above a plane defined by the surface of the substrate and thereby forming an upper, substantially planar surface and exposing an upper end of the first doped layer in the trench; forming a
first electrical contact to the first semiconductor doped layer; and forming a second electrical contact to the third semiconductor doped layer.

[0010] Other embodiments include one or more of the following features. Forming the second semiconductor layer involves selecting a semiconductor material for the second semiconductor layer for which second bandgap is smaller than the bandgaps of both the first and third semiconductor layers. Alternatively, forming the second semiconductor layer involves introducing a dopant that produces deep level energy states in the bandgap between the conduction and valence bands.

[0011] In general, in still another aspect, the invention features a detector including: a substrate having a top surface and a first trench formed therein; a first semiconductor layer conforming to an inside contour of the first trench and having an upper surface defining a second trench within the first trench, the first semiconductor layer having a first end that is substantially coplanar with the top surface of the substrate; a second semiconductor layer conforming to an inside contour of the second trench and having an upper surface defining a third trench within the second and first trenches; a third semiconductor layer filling the third trench and having a top side that is substantially coplanar with the top surface if the substrate; a first conductive material making an electrical contact to the first layer at the first end; and a second conductive material making electrical contact to the third layer on the top side of the third layer.

[0012] Other embodiments include one or more of the following features. The first and third semiconductor layers are made of a doped silicon. The second semiconductor layer is made of a SiGe alloy. The SiGe alloy is characterized by a conduction band located above and separated from a valence band by a bandgap, and the SiGe alloy contains an impurity that introduces deep level energy states in the bandgap between the conduction and valence bands. Alternatively, the second semiconductor layer absorbs light of wavelength \( \lambda \) and the first and third semiconductor layers transmit light of wavelength \( \lambda \). The second semiconductor layer has a bandgap that is less than the bandgap of both the first and third semiconductor layers.

[0013] Other features and advantages of the invention will be apparent from the following detailed description and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1A shows the band structure of silicon doped with deep level acceptors.

[0015] FIG. 1B shows the relative semiconductor energy bands of the transmission waveguide, the high absorption material, and the photon energy.


[0017] FIG. 3 depicts in schematic form an impurity-based SiGe alloy detector.


DETAILED DESCRIPTION

An Impurity-Based Detector

[0019] One embodiment of the invention is an impurity-based detector that is made of silicon and a SiGe alloy and that satisfactorily detects optical signals with wavelengths that are longer than the wavelength corresponding to the absorption edge of silicon or SiGe alloy including optical signals with a wavelength longer than 1150 nm. The detectors are made within a waveguide typically having a SiGe alloy of about 5% Ge forming the waveguide core by doping that core with a material that generates deep energy levels within the bandgap energy region of the SiGe alloy. That is, the dopant is characterized by producing energy states that are sufficiently far from either conduction or valence band so that an optical signal with a wavelength greater than 1150 nm will cause transitions of electrons between this dopant-induced state and one of the bands, creating free charge for an electrical current, thereby detecting the optical signal.

[0020] Within the periodic table there are a number of elements that produce deep energy levels in semiconductors. Two elements, in particular, share a number of characteristics that are important for constructing detectors that can be incorporated into conventional fabrication processes that one might typically find in the silicon semiconductor fabrication industry. They are thallium and indium. Referring to FIG. 1, they produce deep acceptor states 2, which means their energy states are closer to the valence band 4 than the conduction band 6, but far enough above the valence band to allow wavelengths longer than 1200 nm to be productively absorbed. Indium produces acceptor states at about 160 meV above the valence band and thallium produces acceptor states that are about 260 meV above the valence band. Both of these elements also have diffusion rates that are slow enough that they will stay substantially in place under normal fabrication and operational temperatures that the detectors might experience if used in an optical ready substrate in which other microelectronic devices are later fabricated. That is, they will not diffuse out of the detector during subsequent thermal cycles to which the wafer will be exposed.

[0021] It should also be noted that the impurity states could through a more complex interaction with the band edge produce a broad or smooth distribution of deep energy levels when incorporated into Si or a SiGe alloy. Thus a broad impurity absorption spectrum can occur near the band edge, appearing as an extension or tailing of the band absorption. This broad spectrum is generally useful in aiding the tolerance of the detector to known temperature shifts in the band gap that would otherwise move the absorption energy off resonance from the light quantum energy and negatively affect absorption with temperature changes.

[0022] The transition that is of interest in the described embodiment of the SiGe alloy impurity-based detector could be from valence band to conduction band via energy state bands that extend or tail into the energy gap because of the impurity effects, or from more band-isolated deep acceptor states to the conduction band. It is these transitions that will produce the electrical detection signal. When a SiGe alloy is doped with either indium or thallium, many of the valence states are ionized to produce the holes that characterize p-type semiconductor materials. To increase the population of electrons in the deep acceptor states, i.e., to fill the available acceptor sites, the SiGe alloy is also doped with a donor material, e.g., As or P. The electrons from the donor dopant fill the acceptor sites and thereby increase the number of acceptor sites that are available to support a transition of an electron up into the conduction band. This filling of the acceptor sites could also occur from transfer of electrons from donors in an adjacent N-type region within a PN diode structure to be discussed later.
The use of such co-dopants also yields another benefit in photoconductive detector mode to be discussed later. Filling up the holes generated by the deep level acceptor dopant, decreases the number of free electrons and/or holes that facilitate conduction through the material and thereby increase its resistance. In photoconductive detectors, the impurity-based SiGe alloy is used as the material for the intrinsic or low charge region between the two of same type (N or P) electrodes. The lower the resistance of this region, the higher the dark current that is produced by the device in the absence of an optical signal. It is desirable to keep the dark current as low as possible. Introducing an opposite type co-dopant along with the deep level state helps accomplish this objective. If the co-dopant is increased beyond that needed to make the material intrinsic, or charge balanced, then the material can have the charge of the opposite sign in the other band. This leads to a photo-transistor effect that can provide more gain at the expense of bandwidth or speed. This device will be discussed in more detail later.

The increase in the population of both holes and electrons by using co-dopants also yields yet another benefit. It helps reduce the recombination time of free charges, which is the time needed for a detector to recover after sensing an optical signal, especially in photoconductive type detectors. Stated differently, it increases the recombination rate of electrons and holes, thereby increasing the speed of the device due to there being more electrons and holes together.

Both indium and thallium are characterized by a low solid solubility in Si or SiGe alloys. That means there is an upper limit to how much each of these materials can be added to the silicon lattice before the lattice will no longer accept more of it. The optimum doping levels appear to be in the range of about $10^{15}$ cm$^{-3}$ to $10^{18}$ cm$^{-3}$. In the case of thallium the highest doping levels are typically around 2x$10^{17}$ cm$^{-3}$. To increase this effective density and thereby increase the efficiency of the detectors that are fabricated from these materials one can add a co-dopant that increases the solid solubility of the material in the silicon lattice. In essence, the co-dopant keeps the deep level dopant in the lattice sites and discourages it from coming out of the lattice. In the case of indium, an example of a co-dopant that accomplishes that function is carbon. Other co-dopants that may help activation of indium and thallium include arsenic, phosphorous and other N-type donors in higher concentrations than needed just to fill acceptor sites.

In other words, there are at least four reasons for using one or more appropriate co-dopants along with the thallium or indium. First, they can be used to charge the acceptor impurity to fill the empty holes thereby increasing the number of electrons available to absorb the optical signal (i.e., increasing the sensitivity of the detector). Second, they can be used to produce a higher dark resistance by reducing the number of free charges. Third, they can be used to help reduce the recombination time (i.e., increases the recombination rate) of free charges. And fourth, they can be used to help increase the probability that the deep level acceptor element will occupy a lattice site instead of an interstitial site so as to be optically active. That is, they can produce better activation on the silicon lattice.

In addition, co-dopants can also serve still other useful functions in this context. For example, they can be used to reduce the diffusion coefficient of another co-dopant or they can be used to enhance the thermal stability of the deep level acceptor dopant making it less likely that it will become deactivated in the host lattice by thermal cycling or high temperature operation.

There are a number of co-dopants that serve one or more of the functions just described. For example, in the case of indium, a Group IV element, works to increase the solid solubility of the indium in the silicon lattice. A number of Group V elements, including the widely used elements of arsenic and phosphorous, serve multiple functions. For example, arsenic is a dopant that produces energy states that are about 14 meV from the conduction band. When used with indium or thallium, it significantly enhances the performance of the indium or the thallium by filling the holes with electrons thereby increasing the population of electrons that can undergo a transition into the conduction band. The arsenic also appears to help by enabling more indium or thallium to go into the lattice. And, in the case of indium, it appears to form more complex microstructures with the indium that produces a broader spectrum response for the device.

It is also reported that the Group V element antimony (Sb) is an effective co-dopant for increasing the solid solubility of TI, and that the Group V element bismuth (Bi) is an effective co-dopant for increasing the solid solubility of In (see e.g. Ion Implantation in Semiconductors, Mayer, Eriksson, and Davies, 1970).

A Narrow Bandgap-Based Detector

Another embodiment of the detector is one that is based on semiconductor materials with a smaller band gap than the waveguide SiGe alloy. This narrow band gap material can include a SiGe alloy with much greater Ge concentration, or other semiconductors such as SiGeC or GeC. A criterion for a useful narrow band gap is that the material satisfactorily detects optical signals with wavelengths that are longer than the wavelength corresponding to the absorption edge of silicon or SiGe alloy used in the waveguide, including optical signals with a wavelength longer than 1150 nm (see FIG. 1B). The detectors are made within a waveguide typically having a SiGe alloy of about 5% Ge. The detector is formed by placement of a narrow band gap material in the waveguide core or in sufficiently close proximity to the waveguide to interact with the light traveling within the waveguide. The light will transfer electrons from the lower or valance energy band of this material to the upper or conduction energy band of this material. The excess charge created in each of these bands will create current through the electrodes cladding this detector material.

A fast detector with less than approximately 10 picosecond rise time will typically need to absorb the light and create charge in a region of approximately 100 to 300 nm thick in which the electric fields are high and travel distance of electrons is short. The electron is detected when it reaches a much higher doped top and bottom electrodes. Thus the doping for conducting the current can be done in the electrodes without need for doping the narrow bandgap material. This simplifies the type of narrow bandgap material properties needed. For instance, the narrow bandgap material may be allowed to melt at points in the process since it does not require a delicate doping structure.

There are several materials of particular interest in creation of a narrow band gap detector. A common material is a SiGe alloy. For Ge concentrations above 85%, the band gap of SiGe alloy rapidly gets smaller. Thus, the absorption of SiGe increases greatly for Ge concentrations above 85%. One
issue of increasing germanium concentration is the lower melting point of germanium versus silicon. Although silicon melts at 1415°C, germanium melts at 937°C. Many processes used in fabrication of transistors need temperatures as high as 1050 to 1100°C. As such, a pure Ge detector will melt if made before these processes are completed.

[0033] Another material that may be of interest is SiGeC. Although only small amounts of carbon can be incorporated into SiGe in equilibrium, this small amount of carbon can help to relieve stress mismatch with silicon. A small amount of carbon in SiGe could also help increase the melting point of the SiGe alloy to increase the fabrication temperature in which the detector would survive.

A Method of Fabricating the Detector

[0034] An illustrative method for fabricating an impurity-based detector is depicted in the flow sequence of illustrations of FIG. 2A. In this example, the detector is fabricated in a silicon substrate 300, though it could be fabricated in any appropriately selected substrate in which waveguides can be fabricated such as for example an SOI substrate, an insulating material, or a low index material, just to name a few. The process begins with forming, e.g., by etching, a trench 302 that will define the outer perimeter of the detector (FIG. 2A). The etching of trench 302 is done using any one of a number of etching technologies that are widely used in the semiconductor fabrication industry, e.g., a plasma etch.

[0035] After trench 302 is made, a lower electrode layer 304 is deposited over the surface of substrate 300 and into trench 302 (FIG. 2B). This lower electrode is to be highly conducting for low electrical resistance. Electrode layer 304 can be made conducting, for example, using electrons from highly doped n-type silicon in which the dopant is phosphorous, arsenic, antimony, or bismuth. Alternatively, the electrode could be made conducting using holes with highly doped p-type silicon in which the dopant is boron, aluminum, gallium or indium. The object of this deposition is to form a conducting electrode layer that conforms to the trench but does not fill up the trench. Rather, it leaves a smaller trench of sufficiently large size to allow the several additional layers described below to be deposited.

[0036] This layer should be doped at a sufficient level that the resistance of this electrode does not prevent current from the detector to efficiently flowing into the external sensing circuit. This means the series resistance of all the electrodes should be comparable or less than the resistance of the sensing circuit. On the other hand, too much doping can cause free electron scattering and absorption that reduces efficiency of the detector. Useful ranges of electrode doping are from $10^{14}$ to $10^{19}$ cm$^{-3}$, with the optimum depending on design requirements for loss and resistance. Furthermore, an improved design would use electrode doping that is non-uniform, with low doping in the area with high optical power, and high levels of electrode doping for low resistance in areas of that see low or no optical power. In contrast, the useful absorption caused by the impurity dopant is best placed in regions of high optical power. Increased thickness of the dopant increases absorption as long as it is illuminated by the light to be detected, but thicker regions of dopant could decrease the speed of the detector. For example, to construct a detector with response faster than 20 picoseconds, the dopant should be placed in a region approximately less than 300 nm thick.

[0037] After lower electrode layer 304 is deposited, a first intermediate layer 306 of SiGe alloy is deposited on top of it (FIG. 2C). First intermediate layer 306 is the host material that will receive one or more co-dopants in a subsequent step and it represents one half of the middle portion of the detector structure. The index of refraction of this material needs to be higher than that of the silicon electrode so that it functions as a waveguide structure that contains the light. Thus, the percentage of Ge needs to be appropriately chosen, e.g. at least as large as about 2%.

[0038] A deep level energy state inducing dopant 308, such as indium or thallium, is then implanted into first intermediate layer 306 to a sufficient depth that it will not evaporate out of the intermediate layer during subsequent processing (FIG. 2D). One or more co-dopants are also implanted into first intermediate layer 306. This can be done before, during, or after the implanting of the deep level acceptor dopant. If the co-dopant material serves multiple functions, then it may be acceptable to use only a single co-dopant. If the co-dopant material serves only one function (e.g. increasing the solubility of the deep level acceptor in the silicon lattice), then it will be appropriate to use multiple co-dopant materials. In other words, the types and number of co-dopants one selects during this phase depends on the results one wants to achieve.

[0039] After appropriate dopant materials 308 are co-implanted into first intermediate layer 306, a second intermediate layer 310 of silicon or SiGe alloys is deposited onto first intermediate layer 306 (FIG. 2E). Again the amount of deposition is selected to not fill the trench that remained after the last deposition. This is to leave room for the final deposition of the electrode.

[0040] Finally, an upper electrode layer 312 is deposited onto second intermediate layer 310. Like lower electrode 304, upper electrode 312 can be highly doped n-type silicon in which the dopant is phosphorous or arsenic, antimony, or bismuth. Alternatively, the electrode could be made conducting using holes with highly doped p-type silicon in which the dopant is boron, aluminum, gallium or indium.

[0041] After upper electrode 312 has been deposited, the structure is thermally treated (e.g. annealed) at a sufficiently high temperature and for a sufficiently long time to cause the co-implants to diffuse out into the first and second intermediate layers 306 and 310. A conventional anneal is typically performed at 1050°C. The anneal time and temperature required is determined by the diffusion coefficient of the dopant and the thickness of the first and second intermediate layers. This anneal can occur at any appropriate time after the upper electrode has been deposited, and it need not necessarily immediately follow the formation of the upper electrode.

[0042] If the impurity-based detector is part of a waveguide structure that is also fabricated into the silicon substrate and/ or it is to be part of an optical ready substrate to which connections are made from one side, then the structure is planarized (FIG. 2G). The planarizing process, which may be performed using chemical mechanical polishing (CMP), is meant to remove the deposited layers that are above the surface of silicon substrate 300. This will expose contact points 314 and 316 to lower and upper electrode layers 304 and 312, respectively.

[0043] In an alternate method where a narrow bandgap material is the absorber in the core region, processes in FIGS. 2D and 2E are replaced by an alternate process, as follows. If the narrow bandgap material can be grown with an acceptably low number of defects, then this material is grown in one
blanket layer replacing steps 2D and 2E. This is more likely with SiGe alloys in lower Ge concentrations, or SiGeC alloys with lattice structure and spacing near that of silicon.

Sometimes because of a difference in lattice constant of the narrow bandgap material relative to the silicon wafer and the low Ge concentration SiGe waveguide cladding, the narrow bandgap material cannot be grown well as a blanket growth with a lower number of defects. Additionally, for a lattice mismatch core material, the top electrode growth is also mismatched to the detector material and could also produce large numbers of defects or form polycrystals instead of one single SiGe alloy crystal. In those cases, alternative methods need to be used. One method to improve the quality of the core and top cladding semiconductor material is to form the embossed shallow bandgap material as small islands in the intermediate layer. After the lower electrode is formed, a silicon oxide or silicon nitride mask is formed. Holes are opened in this mask by lithographic patterning and etching of the mask. Then, the narrow bandgap core material can be grown with selective growth only in the openings as a possible option. For Ge and SiGe alloy growth, there are known selective processes that grow on other SiGe alloys and do not grow on silicon oxide or silicon nitride. The mask material can be removed selectively and leave islands of the narrow bandgap material on top of the lower electrode. In an alternative method, the narrow bandgap material can be grown everywhere in a blanket growth and then patterned and etched away to create the islands of absorption.

After the islands are formed, the top electrode can be grown around and laterally over the islands to form low defect material by starting the growth from the lower electrode. One method is to use selective growth of the top electrode on the lower electrode with epitaxial lateral overgrowth on top of the narrow bandgap material. An alternative method is to grow the top electrode on the narrow bandgap material and anneal out the defects in top electrode material. High temperature anneals are also useful for annealing defects out of the narrow bandgap material.

As noted previously, the impurity-based detector can be formed within and as part of the waveguide during the process of also fabricating the waveguide. For example, if a silicon substrate is used, the trench defines the location in which the waveguide is to be formed. The SiGe that is deposited into this trench functions primarily as a waveguide except in regions or locations along that trench at which the detectors are formed. In that case, the dopants introduced in layer 308 are selectively implanted only in regions in which a detector is desired by use of standard photolithographic patterning. This patterned selection of regions of a waveguide is especially useful in optical circuits in which most of the waveguide is used for transmission of light, and the selected regions of the waveguide are used for absorption of light by selectively implanting layer 308 into those regions. The electrode dopants can also be implanted only in the detector regions so as to reduce non-productive optical losses from free electron scattering and absorption in the transmission region of the waveguide.

Similarly, a narrow bandgap material can be patterned and selectively grown as discussed previously to be present at certain locations along the waveguide where absorption and detectors are desired. In an alternative to selective growth, the narrow bandgap material can also be grown everywhere in a blanket growth, and then patterned and removed etching it away where it not needed.

The introduction of the absorbing impurity or the conducting electrode dopants could be performed by implanting at high energy after layer growth as previously described, or alternatively by incorporation by use of additional gases or fluxes of these elements during the Si or SiGe alloy epitaxial layer growth. In the latter case, the selective pattern of the dopant could be performed by selective epitaxial growth. This requires patterning of a masking material such as silicon oxide or silicon nitride in areas where the silicon or doped silicon is not desired to grow. Then, the substrate temperature and growth rate is adjusted so that epitaxial growth only occurs on the exposed SiGe alloy surfaces and not on the masking material.

A narrow bandgap material can also be selectively grown by this same method.

An improved method which aids in lithographic patterning and CMP polishing is to form a masking layer of silicon nitride or silicon oxide before etching the trench in FIG. 2A. Then, in subsequent steps, this masking layer will be present only on the top surface but not on the surfaces within the trench. By growing the lower electrode and detector materials selectively on the trench material but not on the mask, the trench depth will be reduced for the patterning of the detector. A large trench depth can cause issues for photoresist side wall coverage and depth of focus on modern lithography machines. So, the shallower trench improves the ability of photolithography to selectively pattern the detectors at desired points along the waveguide. The use of selective growth in the trench also reduces the amount of material that must be removed by the chemical mechanical polishing (CMP). The masking layer also functions as an etch stop for the chemical mechanical polishing (CMP). As a result of providing this a highly selective etch stop, the wafer uniformity, flatness, and smoothness can be maintained and the original high quality low defect silicon surface can be brought to the surface in a reliable manner.

The above-described waveguide illustrates an example of using a trench to form the waveguide and the included impurity-based detectors. One could also use a ridge structure instead of a trench to fabricate the waveguide and the detectors. For example, an analogous functioning waveguide detector is realized by forming on the substrate a ridge of silicon that traces out the path of the optical waveguide. Then, the three layers, which in the impurity-based detector represent the two electrodes and the intermediate impurity-doped region, are deposited over the substrate so that they cover and conform to the ridge of silicon. After etching away the appropriate material, the three layers form the optical waveguide and, in areas in which the doping is modified appropriately as discussed above, they form the impurity-based detectors within the waveguide. In yet another physical embodiment, the layers can be grown on a planar surface and then the material on either side of a strip that is to be the waveguide is etched away. The material between the two strips that have been etched away represents the waveguide and wherever it is desired to have detectors located, the doping of the layers making up the waveguide can be modified accordingly during fabrication to produce impurity-based detectors at those locations. A fill material can also be deposited to fill up the portions that were etched away on either side of the waveguide to thereby define the side walls of the waveguide and the impurity-based detectors. The nature of the material that is used to fill those portions will depend on whether the material is designed to aid in confinement of the
optical signal or in electrically connecting to the detectors. For example, if it is meant to aid in confinement of the optical signal in the lateral direction, the fill material should have on average a lower refractive index than the material making up the detector and waveguide.

[0052] Of course, if the detector is to be used as a standalone device or in some other environment, it might not be necessary to planarize the structure to expose the contact point for the lower electrode, as described above. Rather, one could make one contact to the top electrode from above and the other to the lower electrode from below through the backside of the structure. Yet another alternative is to form an insulating contact hole from the top to contact the bottom electrode.

[0053] In any case, in one embodiment, the final steps involve depositing an insulating layer 318 over the structure, forming contact vias 320 and 322 through insulating layer 318 and to the contact points 314 and 316 on the lower and upper electrodes, respectively; depositing a metal, e.g., aluminum, within the vias to form ohmic contacts at the bottom of the vias; and then filling vias 320 and 322 with metal (e.g., tungsten plugs) that provides electrical connectivity to the ohmic contacts at the bottom of the vias. Of course, there are likely to be many other layers deposited on top of the structure depending on the circuit in which this device is embedded. So, the process of forming the contact vias might occur much later in a more involved fabrication process. In addition, if the device is part of an optical ready wafer, the eventual connection to the lower and upper electrodes might be performed by another entity, such as the company that fabricates the semiconductor microelectronic circuits above the optical layer.

[0054] Referring to FIG. 3, there are a number of considerations worth keeping in mind when fabricating the detectors just described. For one thing, if the detector is coupled to a waveguide, the optical energy from the waveguide will need to propagate into the detecting region 400. It is thus important to carefully match the mode of the waveguide to the mode of the detector so that this coupling of energy is optimized.

[0055] In the case of a SiGe alloy waveguide that is designed to carry 1300 nm optical signals, we have found that a core that is about 1 μm deep and 3 μm wide works well. For a waveguide of that design, a good geometry for the detector is as shown in FIG. 2 with the dimensions as follows: the width “a” of the upper electrode equals about 1.0 μm; the depth of the upper electrode equals about 0.25 μm, the width “b” of the detecting region equals about 0.75 μm; the depth “h” of the detecting region equals about 1.0 μm; and the width “w” of the lower electrode equals about 1.0 μm. For high-speed performance it is preferred to keep the series resistance of the detector as low as possible. For high speed operation with probing through a 50 Ohm transmission line, it is desirable to keep the resistance R of the upper extension of the lower electrode to the contact point on the surface to less than about 10kΩ. For high-speed operation with a high resistance local sensor such as a transistor, the useful resistance could be larger, as high as 1000 to 3000 ohm over length of detector in micrometers. The limit of the resistance is the product of the device capacitance, about 2 femto-Farads per micrometer for a PN diode in the geometry described above and the series resistance, giving an electrical charging time response of 2 to 6 picoseconds for the high resistance described above. A smaller series resistance is accomplished by making the width “w” larger and making the height “h” shorter. Also, additional higher doping outside the region seen by the light could lower the series resistance without increasing optical absorption from the free carriers.

[0056] Another consideration is to keep the light of the optical signal away from the electrons in the highly-doped electrode regions 304 and 312. This can be accomplished in both lower electrode 304 and upper electrode 312 by grading the doping away from the light of the mode propagating through the detector. One way to do this in lower electrode 304 is to change the doping of the layer as it is being deposited. For example, the first half of the deposition puts down a layer of doped silicon in which Np=10^18 cm^-3 and the second half of the deposition puts down a layer with Np=10^17 cm^-3. Thus, the region of electrode 304 that is closest to the light that is propagating through the center of the detector (i.e., absorbing region 400 in FIG. 2) has lower doping levels and is thus less likely to provide electrons that absorb light through scattering. A similar approach can be used to deposit upper electrode 312, putting the more highly doped part of upper electrode 312 near the surface where the contact will be formed.

[0057] The doping profiles can be made up by another entity, such as the company that fabricates the semiconductor microelectronic circuits above the optical layer.

[0058] In general, during this phase of the fabrication process for an impurity-based detector (i.e., forming the intermediate layer that is implanted with a deep level energy state), the goal is to choose the ion implanting energies, the doses, the times and the temperatures so that the detector region is heavily doped with deep level energy states, especially within the light/solid interaction region and preferably where the light intensity is strongest. A typical energy for implanting the thallium or the indium into the first intermediate layer is between 100 kV and 200 kV, which is the range of energies in which many commercially available implantation systems operate. In general, the ion energy needs to be sufficient to achieve an adequate projected range into the host SiGe alloy (e.g., at least about 0.1 μm) so the dopant remains in the host material during subsequent processing. Because economically useful implant energies may only allow shallow implants, smaller than the micrometer thickness of the SiGe alloy waveguide, it may be necessary to interrupt the growth of the waveguide so as to create the implant at a point where the light intensity is highest within the guide.

[0059] As an alternative to implanting, the impurity could be incorporated as part of the SiGe growth process by CVD or MBE, but only allowed to incorporate during the part of the growth where the impurity is desired to be placed. This in-situ impurity growth technique is well known for creating doping profiles of P and N regions in different layers using very similar species of boron, arsenic, and phosphorous.

[0060] In reality, the implant energies can be as low as a few hundred keV or as high as a few MeV. If low implant energies are used, then other known techniques will likely have to be employed to prevent that shallow implanted material from escaping during subsequent processing before it is able to diffuse into the host material. A commonly used well-known technique to address this problem is to use a capping layer
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(e.g. SiO₂, or Si₃N₄) to hold the implant in place until the diffusion into the host material has taken place.

[0061] The target doses for the indium or thallium during implantation are generally between about 10¹⁰-5×10¹⁳ cm⁻² and more particularly between about 10¹⁰-10¹⁴ cm⁻² to the depth of about 0.1 μm. When this implanted dopant is later diffused down into the two intermediate layers, that will produce a doping level in the range of 10¹⁴-10¹⁵ cm⁻³, depending of course on whether a co-dopant is also used to reach the higher concentration. As noted above, the diffusion increases absorption and thus the efficiency of the detector but it also increases the dark current in the photodiode circuit. So the optimum level will depend on the design goals for the system in which the detector will be implemented and will be a trade-off between these two considerations.

Fabricating an Electronic Circuitry on an Optical Ready Substrate

[0062] As noted above, the impurity-based detector can be formed in an optical ready-substrate onto which semiconductor electronic circuitry will later be fabricated. The sequence of process steps for fabricating the electronic circuitry above the optical-ready substrate is generally illustrated in FIGS. 4A-1.

[0063] After the structure shown in FIG. 1F is planarized using for example CMP, the resulting structure is as shown in FIG. 4A. It is assumed that the substrate also includes other optical components that are not shown, such as laser elements for generating the optical signals from electrical signals, optical waveguides for distributing the optical signals, and mirrors or other reflecting elements for directing optical signals up to circuitry that is fabricated above the waveguides or for receiving optical signals from above and directing those signals into the waveguides.

[0064] On top of the planarized surface that was formed above the optical circuitry, a layer of silicon 402 is deposited (see FIG. 4B). This may be accomplished in a number of alternative ways including for example, through a chemical vapor deposition process. The resulting layer provides a surface onto which a silicon wafer can then be bonded by using well-known processes to form an SOI (silicon-on-insulator) structure. The SOI structure includes an insulating layer 404 (e.g. SiO₂) and above that a silicon layer 406, which provides a substrate into which the electronic circuitry is to be fabricated (see FIG. 4C).

[0065] Next, a hard protective layer 408 (e.g. silicon nitride) is deposited over the surface and patterned to create isolation openings 410 that form electrically-isolated islands of silicon 412 (see FIG. 4D). After using an appropriate mask, deeper isolation openings 414 are then etched through both insulating layer 404 and silicon layer 402 to expose the underlying impurity-based detectors (see FIG. 4E).

[0066] To produce a smooth, flat surface for fabricating the electronic circuitry into the islands of silicon an oxide layere 416 (e.g. SiO₂) is deposited over the surface of the wafer. Then, CMP is used to planarize that deposited oxide layer and remove protective layer 408 in the process, thereby exposing the upper surfaces of the silicon islands 412 (see FIG. 4F).

[0067] The rest of the process generally involves standard semiconductor circuit fabrication steps except when it comes to electrically connecting with the underlying impurity-based detectors. In other words, transistors 418 and other electrical components (not shown) are then formed in the islands of silicon using known fabrication techniques, e.g. CMOS fabrication techniques (see FIG. 4G). After that, a thick oxide 420 is deposited over the entire wafer and planarized (see FIG. 4I). Following that, contact openings 422 are etched in the oxide down to the components. The etch that is done during this phase is modified in comparison to conventional etch schedules so that in selected areas the openings 424 reach deeper down to the detectors located at a level below the electrical components (see FIG. 4J). After the contact openings are formed, metal 426 is deposited and patterned to form the required interconnects (see FIG. 4J). Though the metallization is illustrated as all residing in a single layer, for the more complex circuits for which one would likely use the optical ready substrate, the metallizations occupy multiple layers each separated by insulating material, e.g. SiO₂..

[0068] Note that the above description of a process for fabricating the electronic circuitry above the optical ready substrate omitted many minor steps that are well known to persons of ordinary skill in the art. This discussion was meant to be merely a high level description of an example of a sequence of fabrication steps that would produce the desired structure. For a more detailed discussion of all of the process steps that are involved the reader is referred to other publicly available sources in the public literature.

Use of Absorption in a Detector Device

[0069] There are many ways to use absorption in a detector. Depending on the semiconductor doping in the cladding electrode layers surrounding the absorber region relative to the charge polarity of the absorber region, a detector device could be a photodiode detector, a PIN diode detector, or a phototransistor.

A Photodiode Detector

[0070] If the cladding electrode layers of the impurity region have the same majority carrier as the impurity region, then the detector is photoconductive. For example, if thallium or indium is used as an impurity, they tend to create a P-type semiconductor with excess holes. If both top and bottom cladding electrode layers are also doped with P-type acceptors such as boron that create holes, then the device is a photoconductor. A narrow bandgap material with p-type doping and P-type electrode doping would also be a photoconductor. A photoconductor has the property of changing electrical resistance when carriers are generated by light absorption. If more or less carriers are created by transitions to or from an impurity, then the resistance will change. For low dark current, the middle impurity region can be co-doped to reduce net free charge. For instance, the thallium or indium doping could be co-doped with arsenic that creates electrons. If the arsenic co-doping is properly balanced so an electron is made to fill each hole, but not too much to have extra electrons, then the impurity region could be made to have low excess charge from electrons or holes. This would then increase the resistance and lower the current through the unit, or dark, photoconductor.

A P-I-N Diode Detector

[0071] Fabricating a P-I-N diode detector can solve the problem of the relatively large dark currents that tend to characterize the photoconductive detectors. The P-I-N structure is basically the same as what was described above except that the one electrode is highly doped with a P-type acceptor such as boron and the other buffer electrode is doped with a
donor such as arsenic or phosphorous. When this detector is run in reverse electrical bias, low electrical current leaks through a good quality diode, yet efficient high speed detection of light can occur.

[0072] A Phototransistor Detector

[0073] Yet another type of detector is a phototransistor. If the cladding electrode layers of the absorber region have the opposite majority carrier as the absorber region doping, then the detector is a phototransistor. For example, if thallium or indium is used as an impurity, they tend to create a P-type semiconductor with excess holes. If both top and bottom cladding electrode layers are doped with the opposite N-type acceptors such as arsenic or phosphorous that create electrons, then the device is a phototransistor. A phototransistor has the property of amplifying the charge current generated by light absorption. The amplification is the well-known transistor effect from bipolar NPN transistors, but in this case the transistor's base current is provided by the optical absorption rather than a third connecting wire.

[0074] Though we have described photoconductor, photodiode, and phototransistor detectors, it should be understood that these are simply specific examples of what can be referred to more generally as photoconductive detectors and photodiode detectors, respectively. In other words, the electrodes are not restricted to being N-type or P-type, they could also be metal electrodes. In addition, the absorbing region (i.e., the l-region) may be an insulator, a weakly conductive region, or even a highly conductive region.

[0075] The embedded SiGe alloy-based detectors described above are considered to be particularly useful in the fabrication of the optical ready substrates such as are described in detail in U.S. patent application Ser. No. 10/280,505, filed Oct. 25, 2002, entitled “Optical Ready Substrates,” and U.S. patent application Ser. No. 10/280,492, filed Oct. 25, 2002, entitled “Optical Ready Wafers,” both of which are incorporated herein by reference. Some of the waveguides that are mentioned in connection with the optical ready substrates are SiGe alloy waveguides. Methods of making such waveguides are described in publicly available scientific literature including, for example, U.S. patent application Ser. No. 09/866,172, filed May 24, 2001, entitled “Method for Fabricating Waveguides,” and to U.S. patent application Ser. No. 10/014,466, filed Dec. 11, 2001, entitled “Waveguides Such As SiGeC alloy Waveguides and Method of Fabricating Same,” both of which are incorporated herein by reference.

[0076] The embedded detector can be fabricated either after the SiGe alloy waveguide has been fabricated or before. Also, it can be part of the optical waveguide or as a termination of an optical waveguide.

[0077] In addition, multiple different circuit components that employ optical conversion, e.g., diodes, free space detectors, modulators, transistors, and more complex circuit elements, can benefit from the principles described herein. That is, the invention is not limited to just optical detectors fabricated in or next to optical waveguides.

Other Embodiments

[0078] The embodiments described above use SiGe alloys as the semiconductor. Other alternative semiconductors can be used including, but not limited to, Si, Ge, and SiGeC Group IV alloys and Group III-V alloys such as GaAs, InP, and combinations thereof such as InGaAsP. The availability of the other materials extends the range of wavelengths for which this detector can be used from about 650 nm to at least about 1500 nm. More specifically, the above-described concepts can be used to fabricate detectors that work for wavelengths well beyond 1500 nm. For example, one could use such concepts to fabricate detectors that operate in the wavelength region of 10 µm and beyond, i.e., the far infra-red.

[0079] It should also be understood that methods other than the one described above could be used to fabricate the intermediate detector region. The above-described method involved growing half of the layer, implanting the deep level acceptor material, and then growing the other half of the layer. Alternatively, one could epitaxially grow the entire intermediate layer and then use a higher energy to implant the deep level material farther into that layer. Or, one could employ in-situ doping of the intermediate layers as it is being deposited by epitaxial methods or by physical vapor deposition (PVD) or by chemical vapor deposition (CVD) or by other known deposition methods.

[0080] The deep level implants are also not limited to indium and thallium as dopants. They include any material, e.g. element, isotope, molecule or chemical complex, which produces a deep level energy state. In general, deep level energy states are those energy states that are at least about 100 meV from the conduction or the valence band; whereas, shallow level dopants are those that produce energy states that might be less than about 20-40 meV from the band edge. Other elements or isotopes that produce such deep level acceptor states might include zinc, iron, tin, and sulphur, just to name a few. Of course, the range of choices that can be used to fabricate these devices might be severely limited by other requirements that are placed on the device. For example, if the device is expected to survive subsequent thermal cycling to high temperatures, e.g. 1000°C, then the choices are fewer because that will likely exclude materials having high diffusion rates and materials whose thermal stability is not sufficient.

[0081] Indeed, the deep level energy states could be produced in ways other than through introducing dopants into the material. For example, one could produce such states by creating crystallographic defects in the material, by creating a periodic multilayer structure, or by creating microstructures in the material. It should be understood that any mechanism that produces the deep level energy states in the energy band would be acceptable.

[0082] In addition, two or more co-implants or co-dopants can be used in the deep level dopant to accomplish one or more of the previously described beneficial objectives. For example, both carbon and arsenic can be used in connection with indium. Or arsenic and phosphorous can be used along with a deep level acceptor dopant. Or more than two codopants can be used depending on what the desired objectives are. Indeed, as experience in other devices shows, it is often advantageous to introduce multiple co-dopants to optimize performance.

[0083] In the described embodiment of the impurity-based detector, we focused on one particular transition, namely, the transition of an electron from the filled deep level acceptor state to the conduction band. There are, however, at least two other transitions that are of potential interest. The first one is a transition of an electron from deep in the valence band to the neutral acceptor. The second one is a transition of an electron from the valence band to an ionized donor site. Any of these transitions create excess carriers that will contribute to an electrical signal. It might be desirable to emphasize one or
another of these transitions by manipulating the ionization level of the deep acceptor states.

[0084] One way of manipulating this ionization level is with co-dopants, as described above. Without co-doping, roughly half of the indium acceptors will be neutral, and more than 90% of the thallium acceptors will be neutral. Another way of manipulating the ionization level of the acceptors would be using a P-N junction (in the photodiode detector). In this case, virtually all of the acceptors in the P-N junction depletion region would be ionized, facilitating the acceptor-conduction band transitions.

[0085] An improvement is to place the impurity-based detector in an optical resonator for the wavelength to be detected, which allows more absorption and photocurrent at a given or lower optical power. For example, a cavity can be created by using two mirrors spaced on opposite sides of the absorber with a separation that causes the light to resonate through constructive interference. These mirrors can be created by a thin metal, a dielectric stack, or a periodic pattern along the waveguide as in a Bragg grating. The Bragg grating has a special advantage in that it can be made very narrow band in wavelength, even narrower than the resonator bandwidth. So, if light is not amplified it will not be reflected either.

[0086] Other resonators for the detector can be made with waveguide rings in close coupling to the serial waveguide, which would also only detect light at the resonant wavelength and transmit light at other wavelengths. The limitation of a resonator is that it must be sufficiently stable over all temperatures and not reflect sufficient light back down the waveguide that could cause interference with the optical source. Both of the above-mentioned resonators could accomplish this task with good engineering.

[0087] Finally, we note that the structure shown in FIG. 3 is connected as a two-terminal detector. However, the ideas described herein can be embodied in devices with three or more terminals. For example, if used in a three terminal bipolar transistor, the impurity-doped region might be the base region of the device.

[0088] Still other embodiments are within the following claims.

What is claimed is:

1. A method of fabricating a detector, said method comprising:
   forming a first trench in an upper surface of a substrate;
   forming a first doped semiconductor layer on the substrate
   and in the first trench, said first doped semiconductor layer having an upper surface which defines a second trench that extends down into the first trench;
   forming a second semiconductor layer on the first doped semiconductor layer and extending into the second trench, said second semiconductor layer having an upper surface which defines a third trench that extends down into the first trench, said second semiconductor layer having a conductivity that is less than the conductivity of the first doped semiconductor layer;
   forming a third doped semiconductor layer on the second semiconductor layer that extends into and fills the third trench;
   removing portions of the first, second and third layers that are above a plane defined by the surface of the substrate to produce an upper, substantially planar surface and thereby expose above the first trench first and second upper ends of the first doped semiconductor layer and an upper area of the third doped semiconductor layer that lies between the first and second upper ends of the first doped semiconductor layer;
   forming a first electrical contact to the first upper end of the first doped semiconductor layer; and
   forming a second electrical contact to the exposed upper area of the third doped semiconductor layer.

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