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**Yang et al.**

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(54) **SEMICONDUCTOR DEVICE PACKAGE AND A METHOD OF MANUFACTURING THE SAME**

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(Continued)

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See application file for complete search history.

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*Primary Examiner* — Marcos D. Pizarro

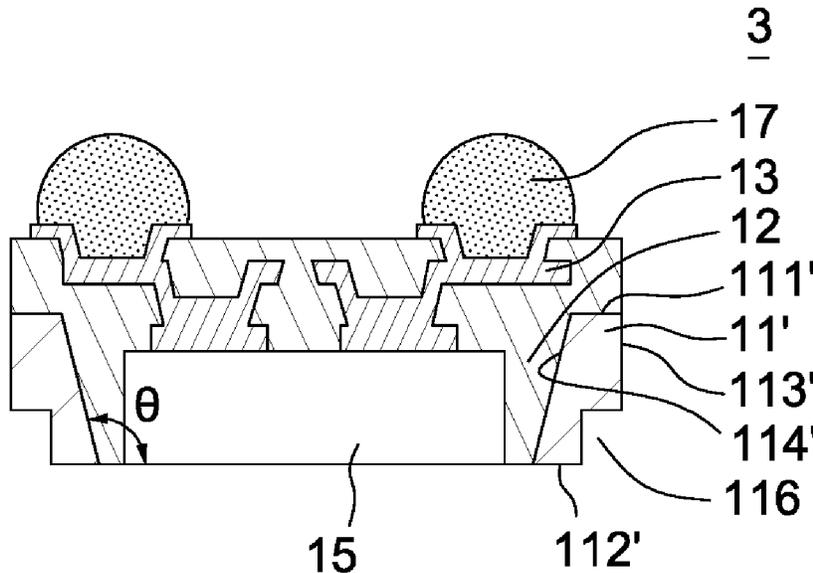
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(57) **ABSTRACT**

A semiconductor device package comprises a semiconductor device, a first encapsulant surrounding the semiconductor device, a second encapsulant covering the semiconductor

(Continued)



device and the first encapsulant, and a redistribution layer extending through the second encapsulant and electrically connected to the semiconductor device.

**17 Claims, 16 Drawing Sheets**

- (51) **Int. Cl.**  
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*H01L 23/538* (2006.01)  
*H01L 21/48* (2006.01)  
*H01L 21/56* (2006.01)
- (52) **U.S. Cl.**  
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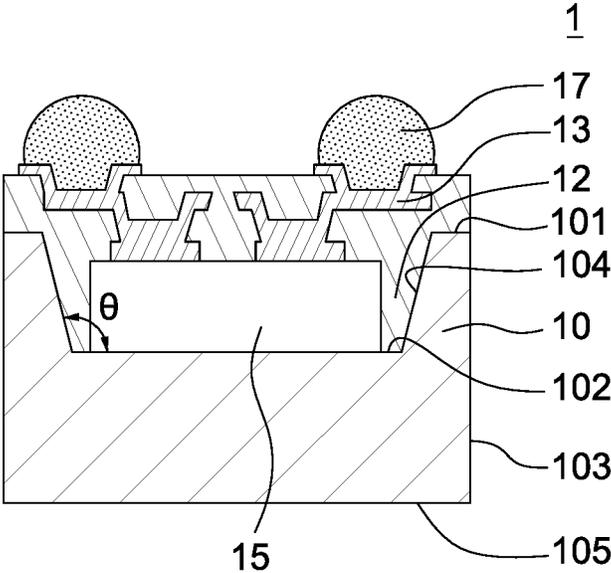


FIG. 1

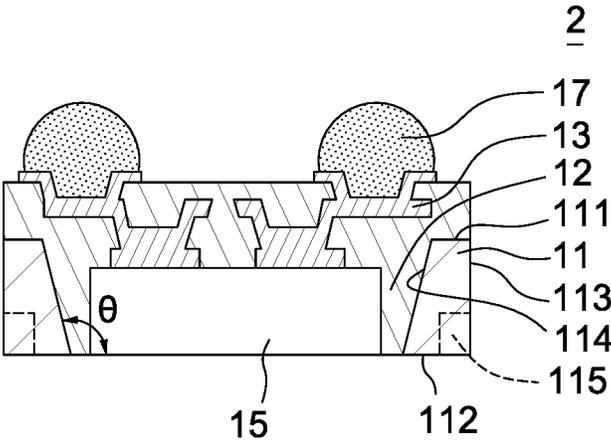


FIG. 2

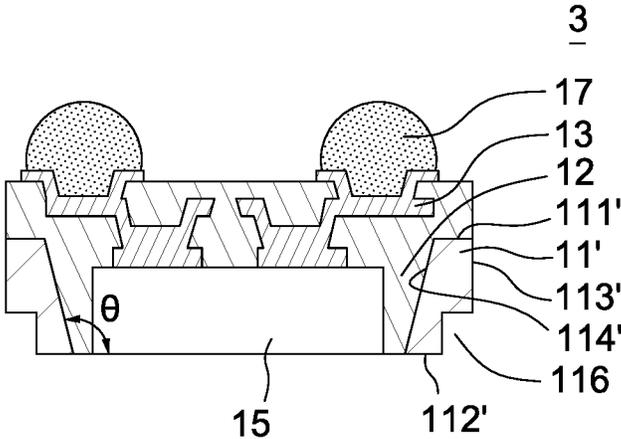


FIG. 3

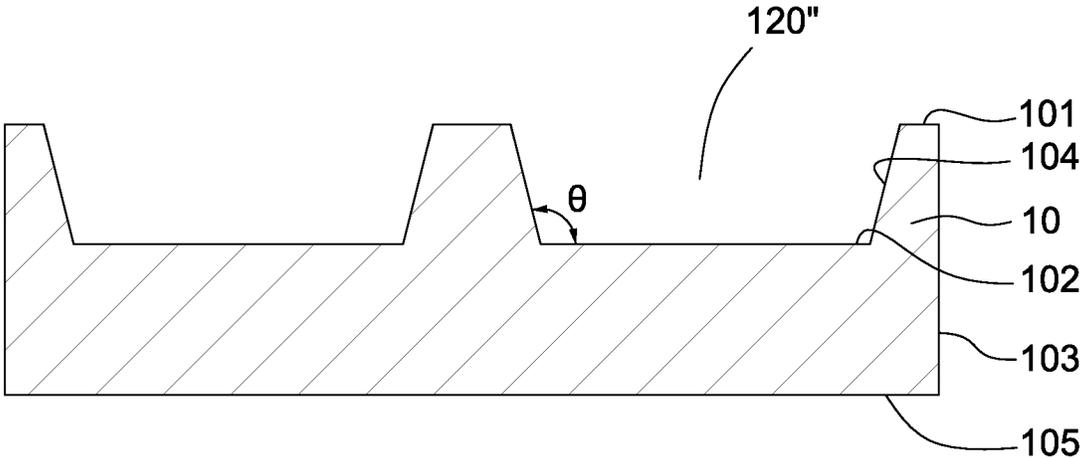


FIG. 4A

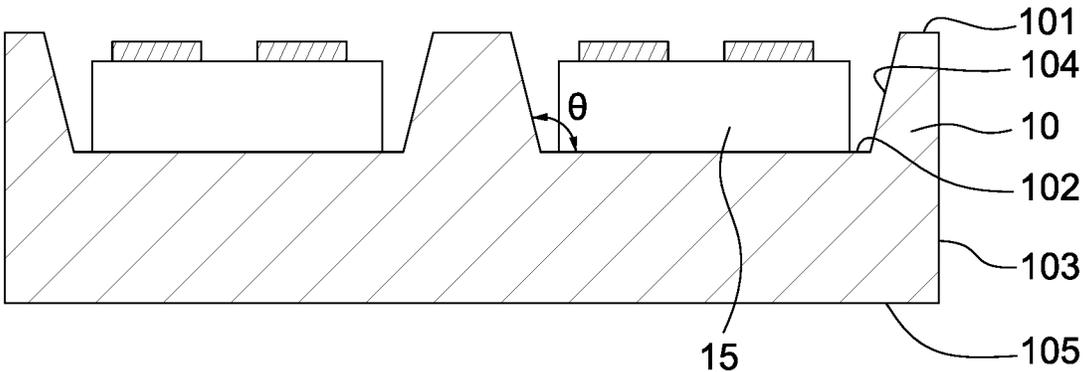


FIG. 4B

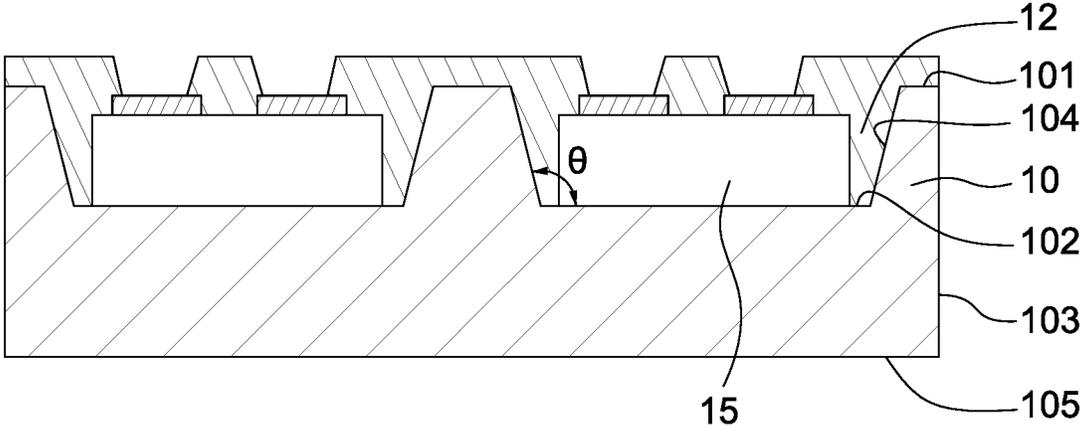


FIG. 4C

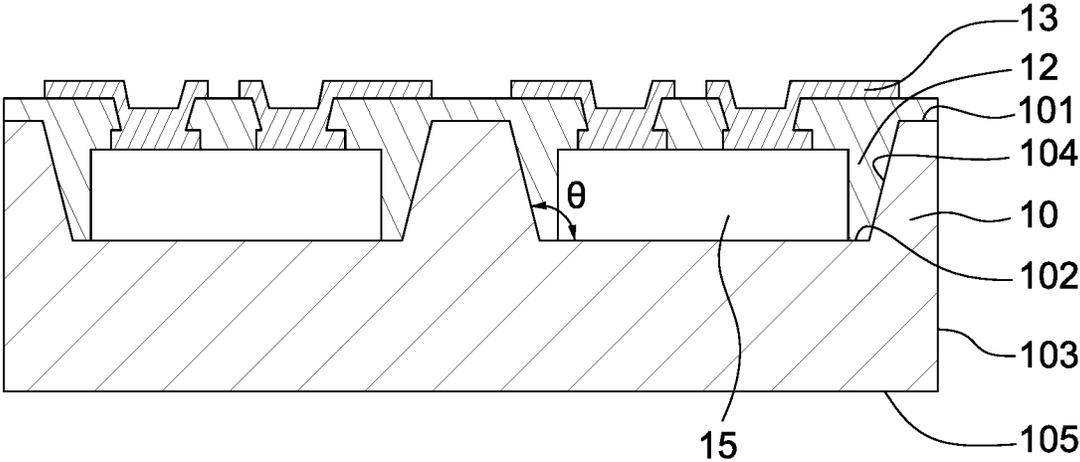


FIG. 4D

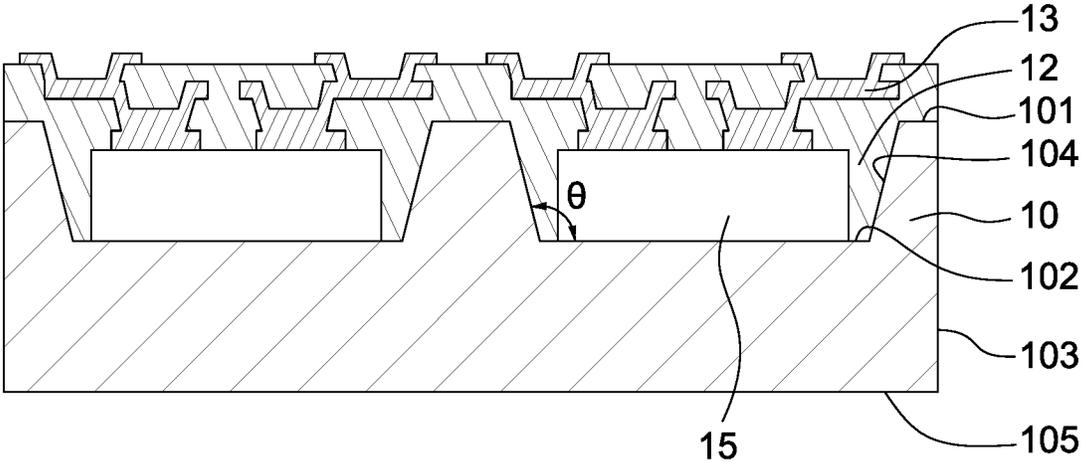


FIG. 4E

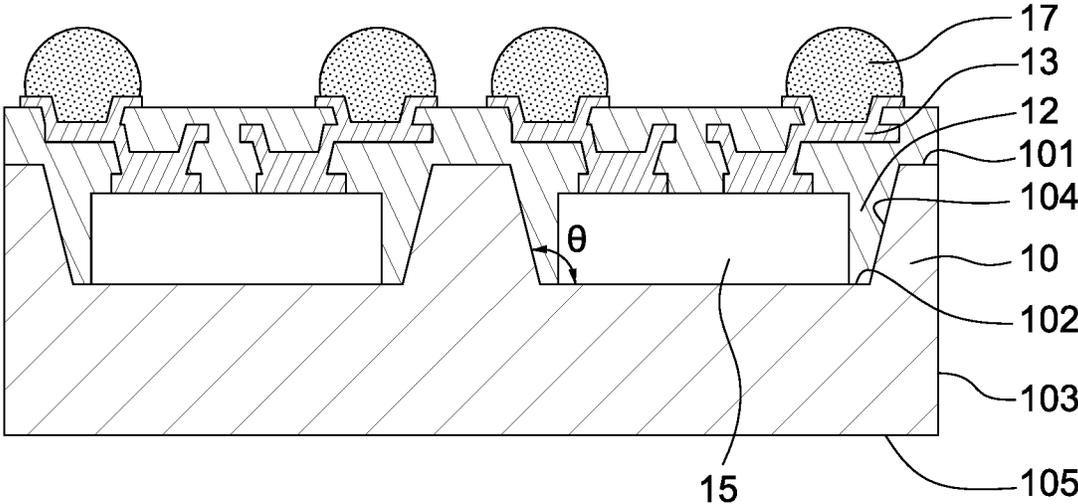


FIG. 4F

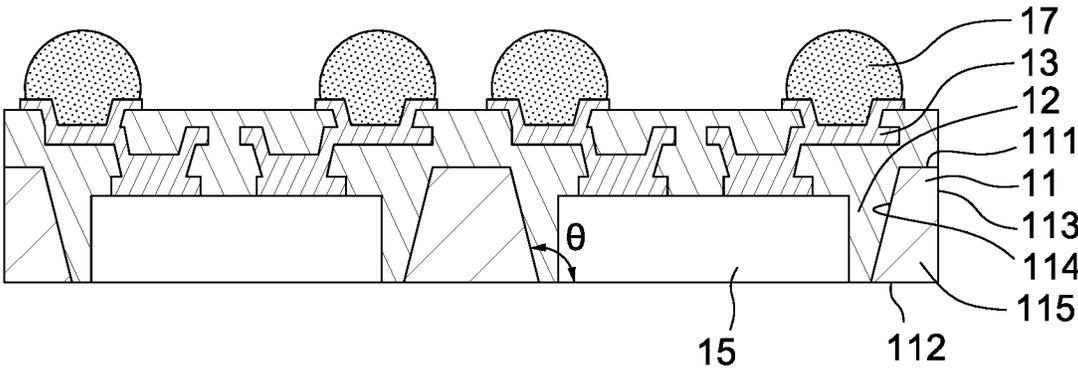


FIG. 4G

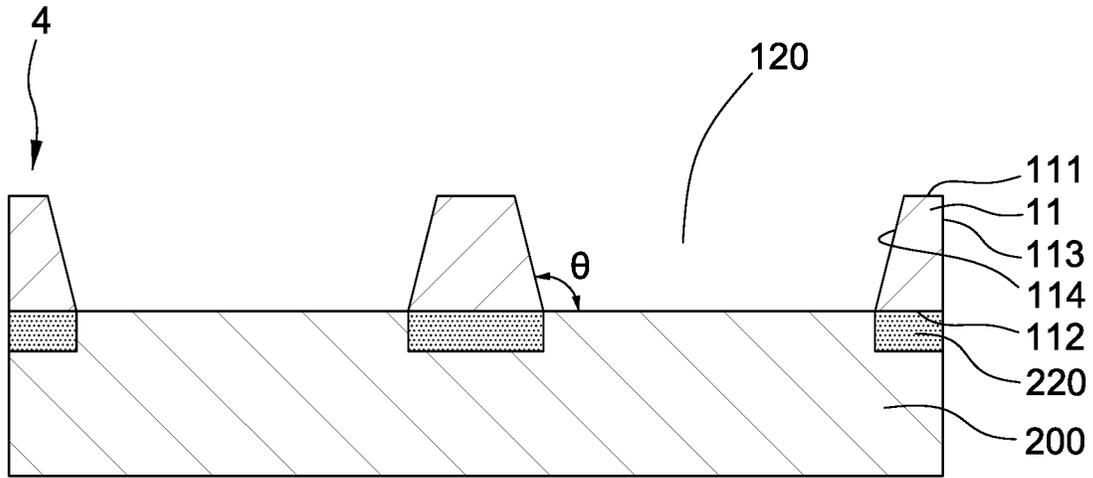


FIG. 5A

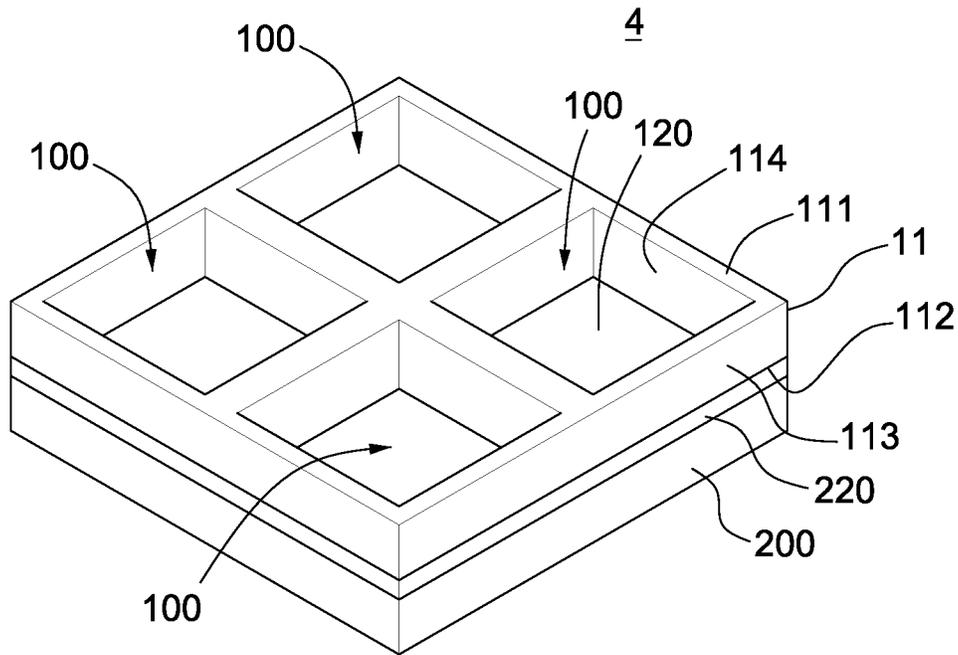


FIG. 5B

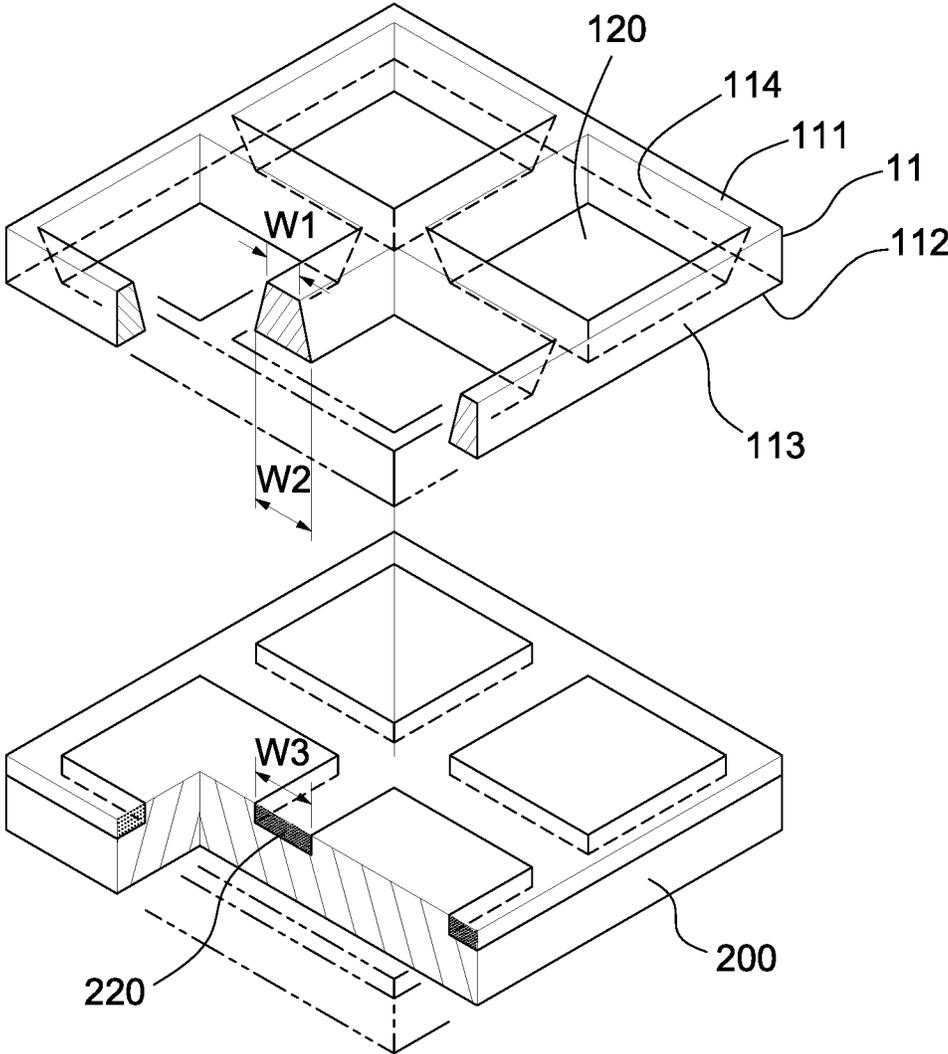


FIG. 5C

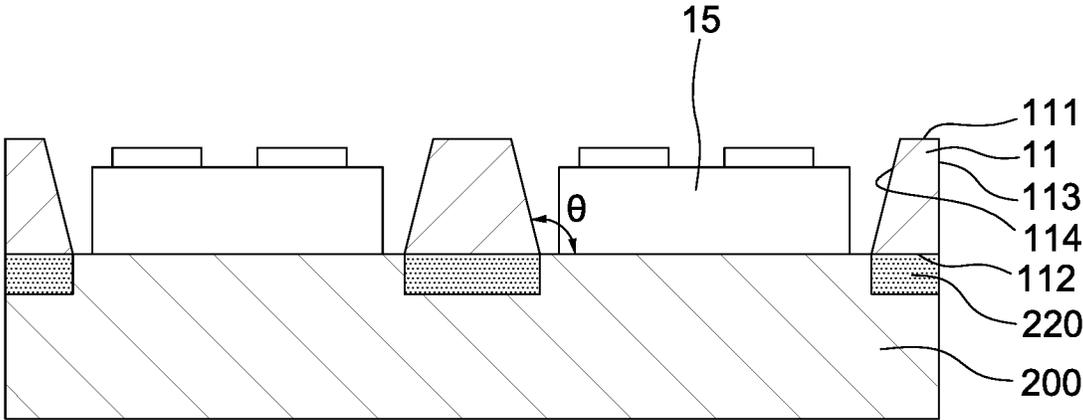


FIG. 5D

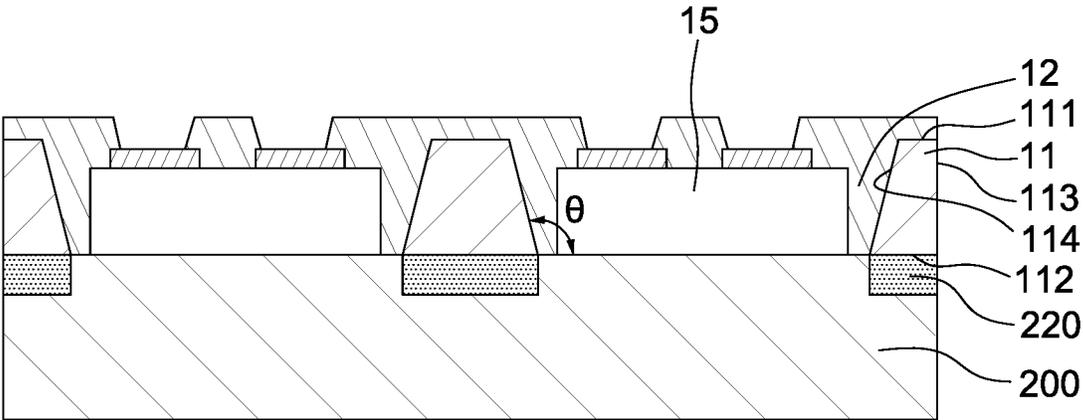


FIG. 5E

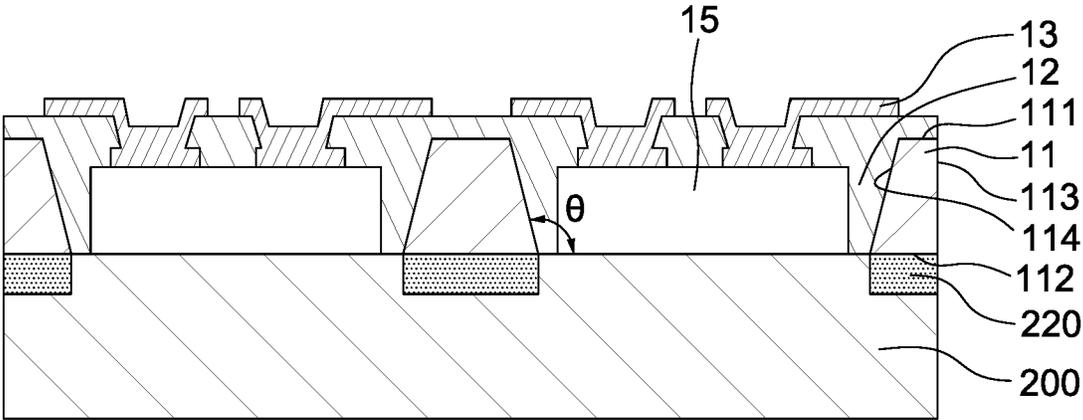


FIG. 5F

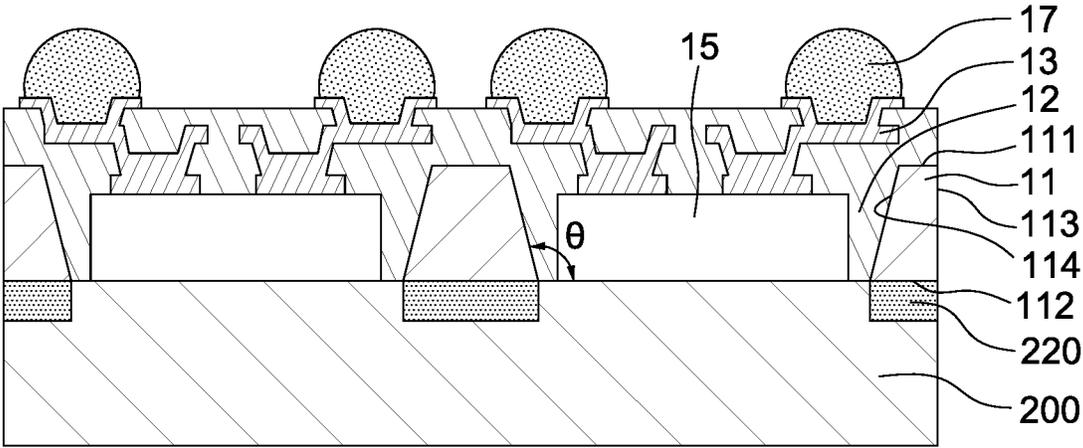


FIG. 5G

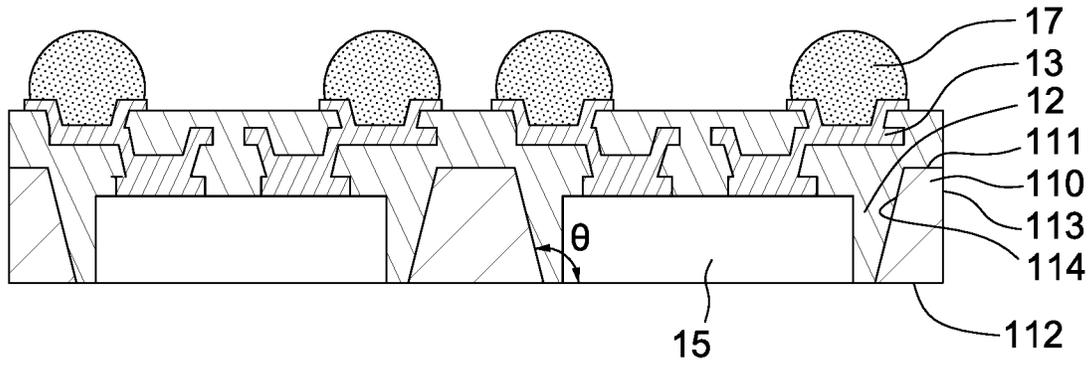


FIG. 5H

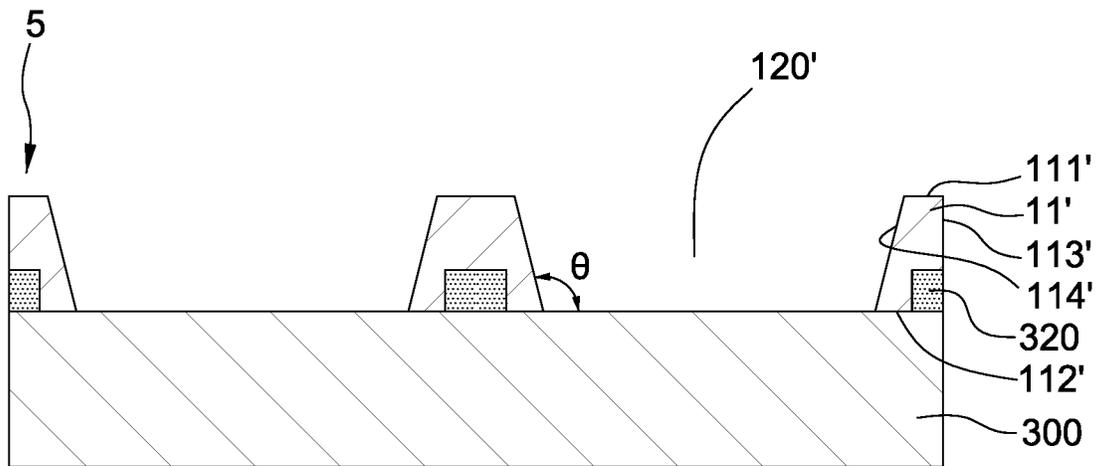


FIG. 6A

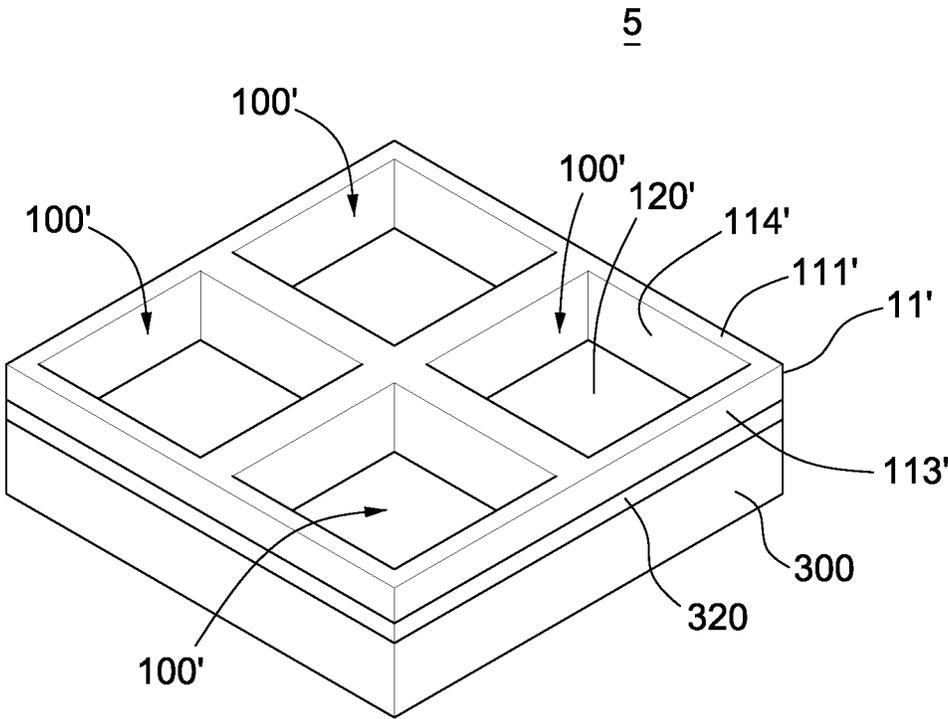


FIG. 6B

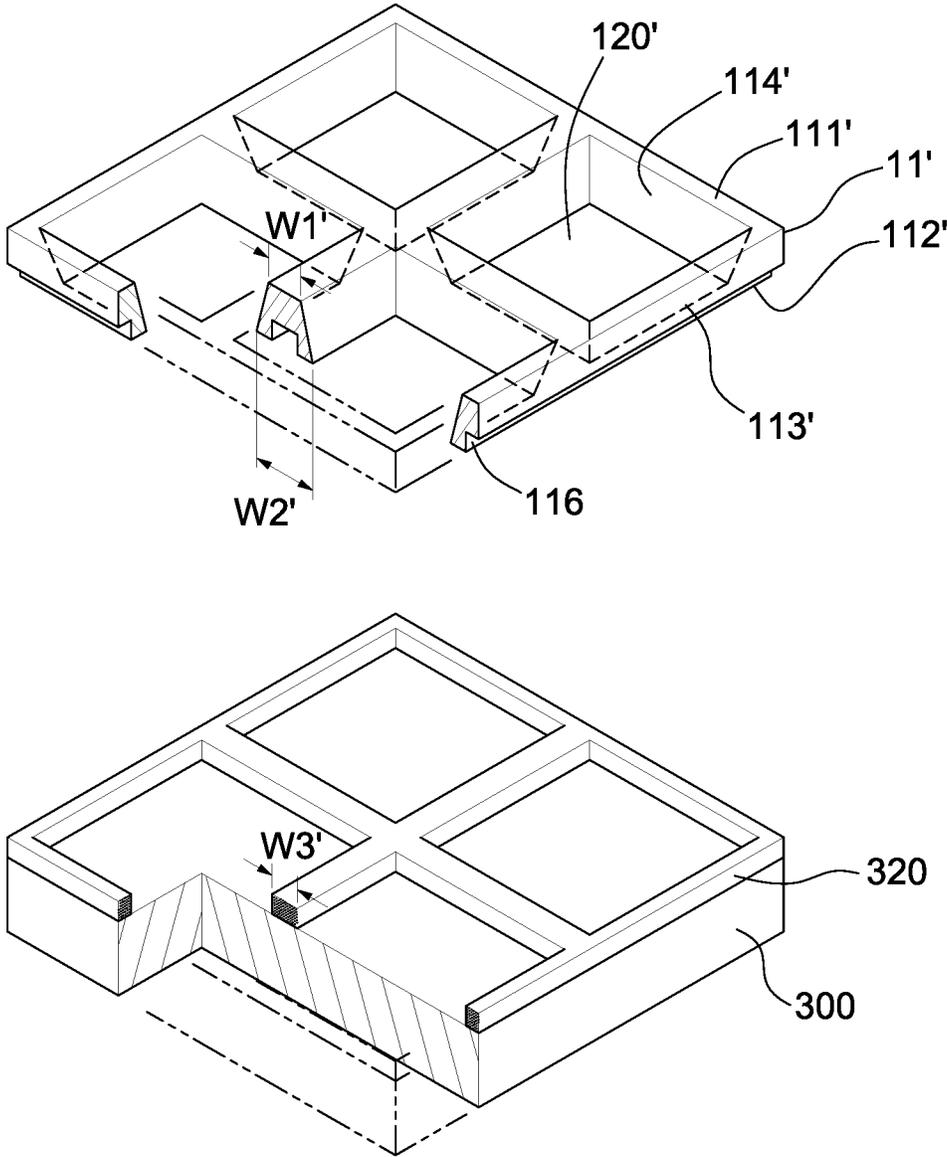


FIG. 6C

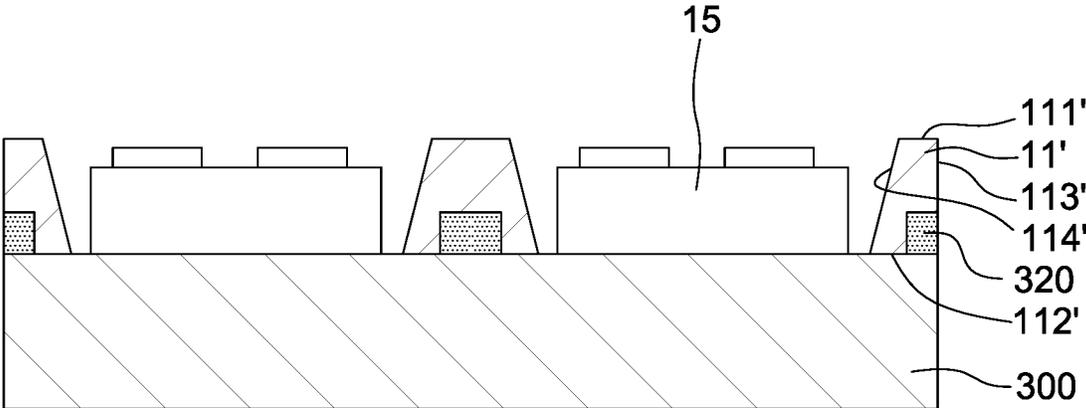


FIG. 6D

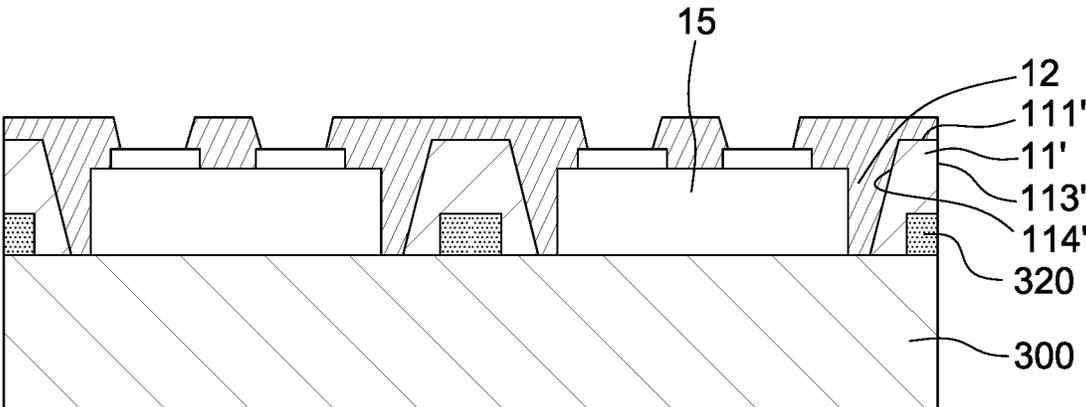


FIG. 6E

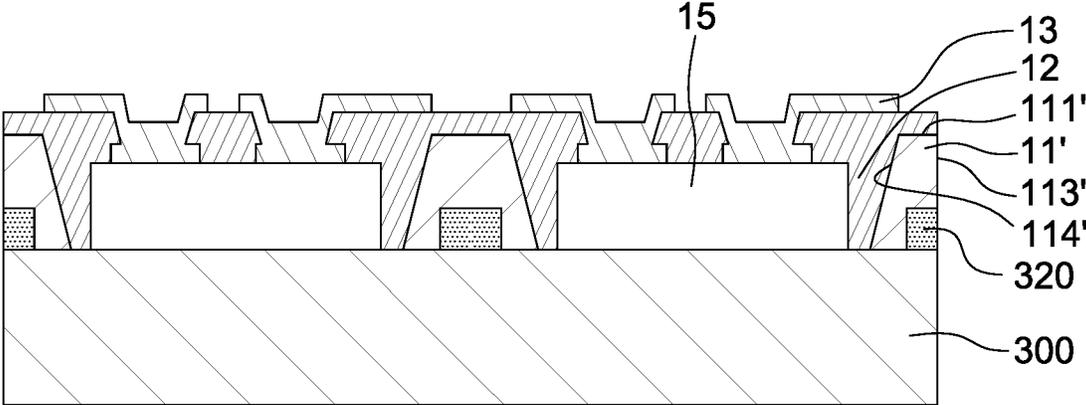


FIG. 6F

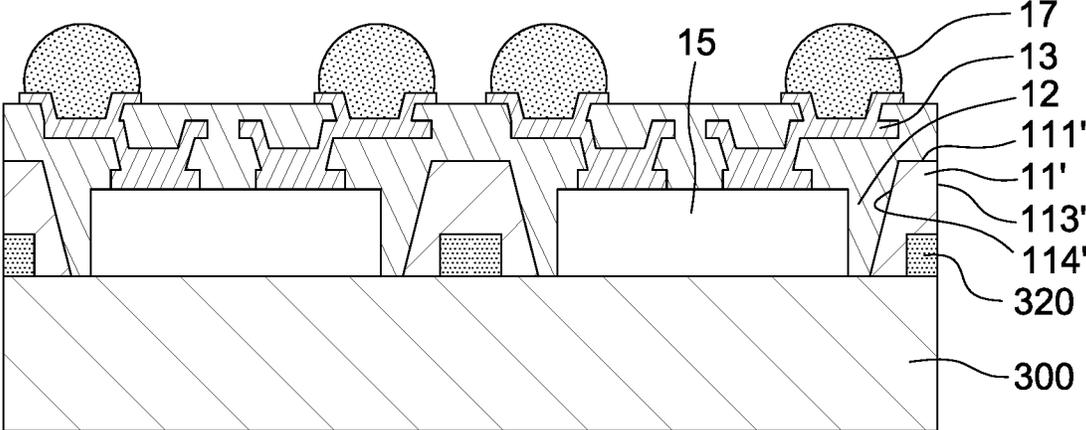


FIG. 6G

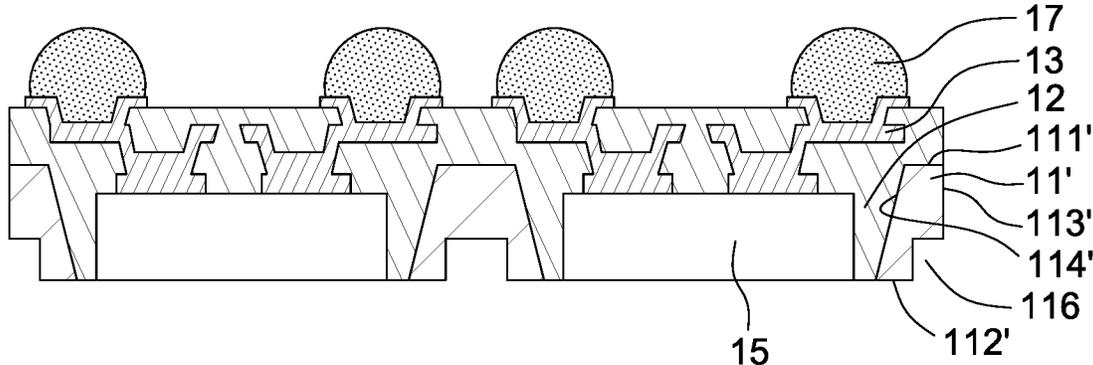


FIG. 6H

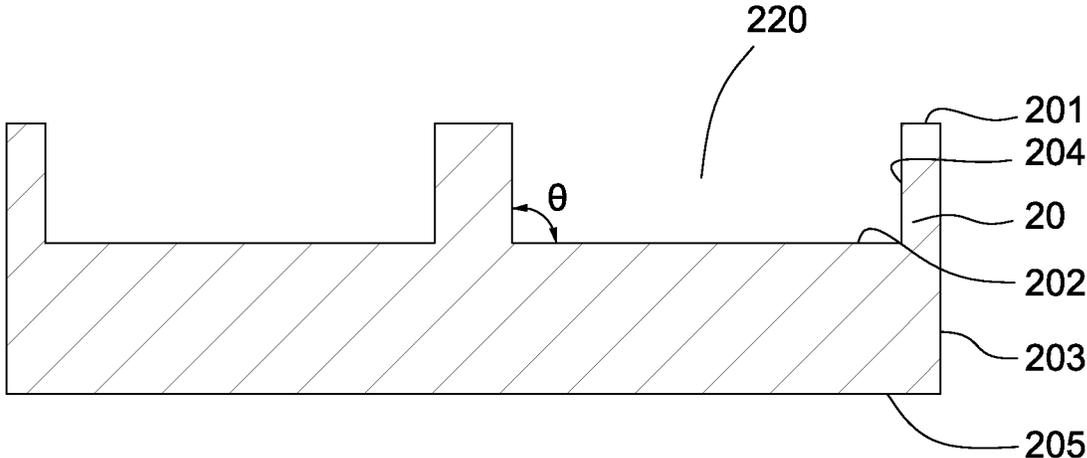


FIG. 7A

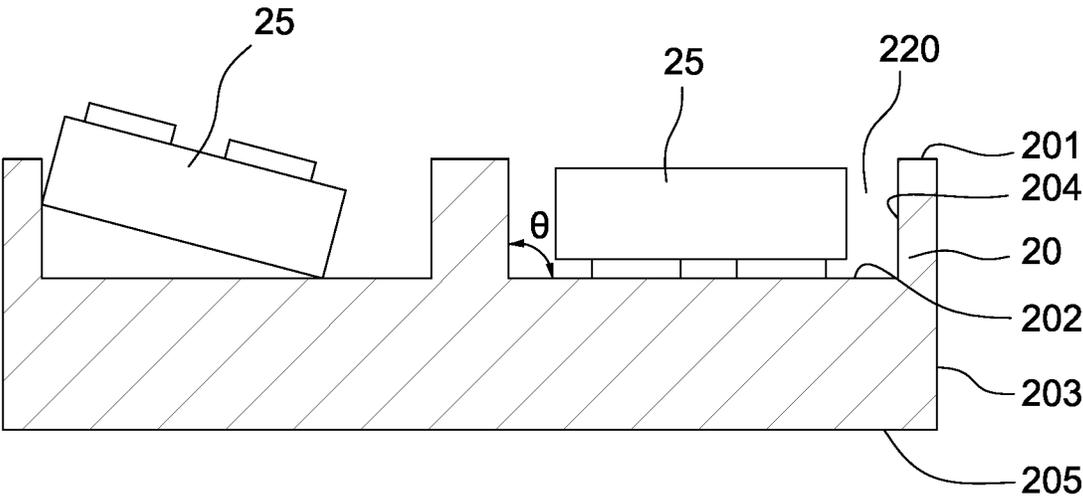


FIG. 7B

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# SEMICONDUCTOR DEVICE PACKAGE AND A METHOD OF MANUFACTURING THE SAME

## CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of and priority to U.S. Provisional Application No. 62/379,153, filed Aug. 24, 2016, the content of which is incorporated herein by reference in its entirety.

## BACKGROUND

### 1. Technical Field

The present disclosure relates to a semiconductor device package. More particularly, the present disclosure relates to a semiconductor device package including an encapsulant surrounding a semiconductor device and another encapsulant covering the semiconductor device and the former encapsulant.

### 2. Description of the Related Art

A semiconductor device is typically attached to a carrier (e.g., a substrate, a lead frame, and so forth) and molded by an encapsulant to form a semiconductor device package. However, warpage phenomenon, die-shifting phenomenon or other problems may cause reliability issues.

## SUMMARY

In some embodiments, according to one aspect, a semiconductor device package comprises a semiconductor device, a first encapsulant surrounding the semiconductor device, a second encapsulant covering the semiconductor device and the first encapsulant, and a redistribution layer extending through the second encapsulant and electrically connected to the semiconductor device.

In some embodiments, according to another aspect, a method is disclosed for manufacturing a semiconductor device package. The method comprises: providing a first encapsulant defining a cavity; disposing a semiconductor device in the cavity; forming a second encapsulant in and over the cavity to cover the semiconductor device and the first encapsulant; and forming a redistribution layer electrically connected to the semiconductor device.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional view of a semiconductor device package according to some embodiments of the present disclosure.

FIG. 2 illustrates a cross-sectional view of a semiconductor device package according to some embodiments of the present disclosure.

FIG. 3 illustrates a cross-sectional view of a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4A illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4B illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

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FIG. 4C illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4D illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4E illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4F illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 4G illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5A illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5B illustrates a perspective view of a substrate array according to some embodiments of the present disclosure.

FIG. 5C illustrates an exploded perspective view of a substrate array according to some embodiments of the present disclosure.

FIG. 5D illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5E illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5F illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5G illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 5H illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6A illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6B illustrates a perspective view of a substrate array according to some embodiments of the present disclosure.

FIG. 6C illustrates an exploded perspective view of a substrate array according to some embodiments of the present disclosure.

FIG. 6D illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6E illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6F illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6G illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 6H illustrates a method of manufacturing a semiconductor device package according to some embodiments of the present disclosure.

FIG. 7A illustrates a cross-sectional view of a comparative encapsulant according to some embodiments of the present disclosure.

FIG. 7B illustrates a cross-sectional view of a comparative encapsulant with a semiconductor device thereon according to some embodiments of the present disclosure.

Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar components. Embodiments of the present disclosure will be readily understood from the following detailed description taken in conjunction with the accompanying drawings.

Spatial descriptions, such as “above,” “below,” “up,” “left,” “right,” “down,” “top,” “bottom,” “vertical,” “horizontal,” “side,” “higher,” “lower,” “upper,” “over,” “under,” and so forth, are specified with respect to a certain component or group of components, or a certain plane of a component or group of components, for the orientation of the component(s) as shown in the associated figure. It should be understood that the spatial descriptions used herein are for purposes of illustration only, and that practical implementations of the structures described herein can be spatially arranged in any orientation or manner, provided that the merits of embodiments of this disclosure are not deviated from by such arrangement.

FIG. 1 is a cross-sectional view of a semiconductor device package 1 in accordance with some embodiments of the present disclosure. The semiconductor device package 1 includes an encapsulant 10, a semiconductor device 15, another encapsulant 12, a redistribution layer 13, and a connection element 17.

The encapsulant 10 includes a surface (or top surface) 101, a surface (or cavity bottom surface) 102, a surface (or bottom surface) 105, a lateral surface 103, and a sidewall (or cavity sidewall) 104.

The surface 101 is opposite to the surface 105. The surface 101 is opposite to the surface 102. The lateral surface 103 extends between the surface 101 and the surface 105. The sidewall 104 extends between the surface 101 and the surface 102. In some embodiments, a roughness of the lateral surface 113 is greater than a roughness of the bottom surface 112.

The sidewall 104 and the surface 102 define a space or cavity to accommodate or receive the semiconductor device 15 and the encapsulant 12. The sidewall 104 may be tapered from the surface 101 to the surface 102. The sidewall 104 and the surface 102 form an angle ( $\theta$ ) which is an obtuse angle in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ . The sidewall 104 and a bottom surface (or backside) of the semiconductor device 15 also form the angle ( $\theta$ ) which is an obtuse angle in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ . In some embodiments, the encapsulant 10 may include a polyimide, a molding compound, a ceramic material, a conductive material, a metallic alloy, or other suitable materials.

The encapsulant 12 fills the cavity. The encapsulant 12 covers the cavity. The encapsulant 12 encapsulates or covers the semiconductor device 15. The encapsulant 12 also covers the encapsulant 10. In some embodiments, the encapsulant 12 may function as a planarization layer. The encapsulant 12 may include a polyimide, a dielectric material or other suitable materials. The sidewall 104 of the encapsulant 10 surrounds a portion of the encapsulant 12 disposed in the cavity. In some embodiments, a material of the encapsulant 10 may be the same as a material of the encapsulant 12. The material of the encapsulant 10 may be different from the material of the encapsulant 12.

The sidewall 104 of the encapsulant 10 surrounds the semiconductor device 15. The surface 101 is higher than a

top surface (or active side) of the semiconductor device 15. In some embodiments, the semiconductor device 15 may include an application-specific integrated circuit (ASIC), a controller, a processor or other electronic component or semiconductor device.

The redistribution layer 13 is disposed at least partially within the encapsulant 12. The redistribution layer 13 is disposed on a portion of the encapsulant 12. The redistribution layer 13 is surrounded by the encapsulant 12. The redistribution layer 13 is electrically connected to the semiconductor device 15. In some embodiments, the redistribution layer 13 includes a patterned conductive layer. The redistribution layer 13 includes conductive traces, pads and vias.

The connection element 17 is disposed on the redistribution layer 13. The connection element 17 is electrically connected to the semiconductor device 15. In some embodiments, the connection element 17 may be a solder ball, a solder paste, a joint material, or other suitable materials.

FIG. 2 is a cross-sectional view of a semiconductor device package 2 in accordance with some embodiments of the present disclosure. The semiconductor device package 2 includes an encapsulant 11, a semiconductor device 15, another encapsulant 12, a redistribution layer 13, and a connection element 17. The depicted structure of FIG. 2 is similar to the structure depicted in FIG. 1, except that the encapsulant 10 depicted in FIG. 1 is replaced with the encapsulant 11.

The encapsulant 11 includes a surface (or top surface) 111, a surface (or bottom surface) 112, a lateral surface 113, and a sidewall (or cavity sidewall) 114. The encapsulant 11 includes corner portions 115. The surface 111 is opposite to the surface 112. The surface 112 is substantially perpendicular to the lateral surface 113. In some embodiments, the bottom surface 112 of the encapsulant 11 is grinded. In some embodiments, a roughness of the bottom surface 112 may be greater than a roughness of the lateral surface 113. The roughness of the lateral surface 113 also may be greater than the roughness of the bottom surface 112. The encapsulant 11 defines a cavity. In some embodiments, the encapsulant 11 may comprise a polyimide, a molding compound, a ceramic material, a conductive material, a metallic alloy, or other suitable materials.

The encapsulant 12 includes a bottom surface. The sidewall 114 of the encapsulant 11 and the bottom surface of the encapsulant 12 define a space or cavity to accommodate or receive the semiconductor device 15. The sidewall 114 may be tapered from the surface 111 to the surface 112. The sidewall 114 and the bottom surface of the encapsulant 12 form an angle ( $\theta$ ) which is an obtuse angle in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ . The encapsulant 12 fills the cavity. The encapsulant 12 covers the cavity. The encapsulant 12 encapsulates the semiconductor device 15 and the encapsulant 11. In some embodiments, the encapsulant 12 may function as a planarization layer. The encapsulant 12 may include a polyimide, a dielectric material or other suitable materials. The sidewall 114 of the encapsulant 11 surrounds a portion of the encapsulant 12 disposed in the cavity. In some embodiments, a material of the encapsulant 11 may be the same as a material of the encapsulant 12. The material of the encapsulant 11 may be different from the material of the encapsulant 12.

A bottom surface (or backside) of the semiconductor device 15 is exposed by the encapsulant 12. A height of the encapsulant 11 is higher than a height of the semiconductor device 15. The tapered sidewall 114 of the encapsulant 11

surrounds the semiconductor device **15**. In some embodiments, the semiconductor device **15** may include an ASIC, a controller, a processor or other electronic component or semiconductor device.

The redistribution layer **13** is disposed at least partially within the encapsulant **12**. The redistribution layer **13** is disposed on a portion of the encapsulant **12**. The redistribution layer **13** is surrounded by the encapsulant **12**. The redistribution layer **13** is electrically connected to the semiconductor device **15**. In some embodiments, the redistribution layer **13** includes a patterned conductive layer. The redistribution layer **13** includes conductive traces, pads and vias.

The connection element **17** is disposed on the redistribution layer **13**. The connection element **17** is electrically connected to the semiconductor device **15**. In some embodiments, the connection element **17** may be a solder ball, a solder paste, a joint material, or other suitable materials.

FIG. 3 is a cross-sectional view of a semiconductor device package **3** in accordance with some embodiments of the present disclosure. The semiconductor device package **3** includes an encapsulant **11'**, a semiconductor device **15**, another encapsulant **12**, a redistribution layer **13**, and a connection element **17**. The depicted structure of FIG. 3 is similar to the structure depicted in FIG. 2, except that the corner portions **115** of the encapsulant **11** depicted in FIG. 2 are removed from the structure depicted in FIG. 3 so as to form recesses **116**. The third encapsulant **11'** comprises a step structure.

During a singulation operation, the encapsulant **11'** is cut with a saw. The structure of the encapsulant **11'** may reduce the consumption or degradation of the saw during the singulation operation because the singulated portion is reduced in the structure of the encapsulant **11'**.

FIG. 4A through FIG. 4G illustrate some embodiments of a method of manufacturing the semiconductor device package **1** or the semiconductor device package **2** according to some embodiments of the present disclosure.

Referring to FIG. 4A, the method includes providing the encapsulant **10**. In some embodiments, the encapsulant **10** is pre-designed with a particular specification.

The encapsulant **10** includes the surface **101**, the surface **102**, the surface **105**, the lateral surface **103**, and the sidewall **104**. The sidewall **104** extends from the surface **101** to the surface **102**. The sidewall **104** and the surface **102** form an angle ( $\theta$ ) which is in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ . The sidewall **104** and the surface **102** define a cavity **120''**.

Referring to FIG. 4B, the semiconductor device **15** is disposed in the cavity **120''** of the encapsulant **10**. The semiconductor device **15** is disposed on the surface **102** of the encapsulant **10**. While disposing the semiconductor device **15** on the surface **102** of the encapsulant **10**, the tapered sidewall **104** may help to guide the semiconductor device **15** to the surface **102** to avoid a misalignment or die-shift issue. The semiconductor device **15** may be directly disposed on the surface **102**.

Referring to FIG. 4C, the encapsulant **12** is disposed or formed in and over the cavity **120''** to cover the encapsulant **10** and the semiconductor device **15**. The encapsulant **12** may function as a planarization layer. The quantity of the encapsulant **12** is relatively less and a warpage issue here is mitigated. Conductive pads of the semiconductor device **15** are exposed by the encapsulant **12**. The conductive pads of the semiconductor device **15** are exposed by the encapsulant **12** via, for example but not limited to, a photolithography

technique. The conductive pads of the semiconductor device **15** are exposed by the encapsulant **12** via, for example but not limited to, a grinding technique.

Referring to FIG. 4D, the redistribution layer **13** is formed on the encapsulant **12**.

Referring to FIG. 4E, an additional portion of the encapsulant **12** is further disposed or formed on the redistribution layer **13** and covers the redistribution layer **13**. The additional portion of the encapsulant **12** is patterned to expose the redistribution layer **13**. An additional redistribution layer **13** is further formed on the additional portion of the encapsulant **12**. The redistribution layer **13** is surrounded by the encapsulant **12**. The redistribution layer **13** is electrically connected to the semiconductor device **15**.

Referring to FIG. 4F, the connection element **17** is disposed on the redistribution layer **13**. The connection element **17** is electrically connected to the semiconductor device **15**.

The semiconductor device package **1** depicted in FIG. 1 is then formed if the structure depicted in FIG. 4F is singulated by a singulation operation.

Referring to FIG. 4G, the encapsulant **10** is grinded by a grinding operation to form the encapsulant **11**. A roughness of the bottom surface **112** of the encapsulant **11** may be greater than a roughness of the lateral surface **113** of the encapsulant **11**. The semiconductor device **15** is exposed by the encapsulant **11**.

The semiconductor device package **2** depicted in FIG. 2 is then formed if the structure depicted in FIG. 4G is singulated by a singulation operation.

FIG. 5A and FIG. 5D through FIG. 5H illustrate some embodiments of a method of manufacturing the semiconductor device package **2** according to some embodiments of the present disclosure.

Referring to FIG. 5A, the method includes providing a substrate array **4**. The substrate array **4** includes a portion including an encapsulant and a portion including a release layer with a carrier. The substrate array **4** includes a plurality of substrates **100** (as shown in FIG. 5B). Each substrate **100** includes an encapsulant **11**, a release layer **220**, and a carrier **200**. The encapsulant **11** is attached to the carrier **200** via the release layer **220**. The release layer **220** is covered by the encapsulant **11**. The carrier **200** serves to support the encapsulant **11**. In some embodiments, a plurality of the encapsulants **11** of the substrates **100** can be pre-designed or pre-molded. The carrier **200** may be recyclable. The volume of the encapsulant **11** can be designed as a minimum or reduced volume to reduce manufacturing cost.

The encapsulant **11** includes the surface **111**, the surface **112**, the lateral surface **113**, and the sidewall **114**. In some embodiments, the bottom surface **112** of the encapsulant **11** may be grinded. The bottom surface **112** of the encapsulant **11** may not be grinded. The encapsulant **11** defines a cavity **120**. The sidewall **114** of the encapsulant **11** and a top surface of the carrier **200** define the cavity or space **120**. The sidewall **114** may be tapered from the surface **111** to the surface **112**. The tapered sidewall **114** of the encapsulant **11** and the top surface of the carrier **200** form an angle ( $\theta$ ) which is in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ .

FIG. 5B illustrates a perspective view of the substrate array **4** according to some embodiments of the present disclosure. The substrate array **4** includes the plurality of substrates **100**. The encapsulant portion of the substrate array **4** has a grid pattern. The release layer portion of the substrate array **4** has a grid pattern. Each substrate **100** includes the encapsulant **11**, the release layer **220**, and the

carrier **200**. The encapsulant **11** is attached to the carrier **200** via the release layer **220**. In some embodiments, the encapsulant **11** may include a polyimide, a molding compound, a ceramic material, a conductive material, a metallic alloy, or other suitable materials. In some embodiments, the release layer **220** may be a thermal release film or an ultraviolet (UV) light release film. The release layer **220** may be a tape, a glue, or an adhesive.

FIG. 5C illustrates an exploded perspective view of the substrate array **4** according to some embodiments of the present disclosure. The substrate array **4** is divided into the encapsulant portion and the release layer portion with the carrier **200**. The release layer **220** is embedded in the carrier **200**.

For the encapsulant **11** of the substrate **100**, the surface **111** of the encapsulant **11** has a width **W1** (corresponding to a top line width of the grid pattern of the encapsulant portion). The surface **112** of the encapsulant **11** has a width **W2** (corresponding to a bottom line width of the grid pattern of the encapsulant portion). The width **W2** is larger than the width **W1**. The release layer **220** is embedded in the carrier **200**. The release layer **220** has a width **W3** (corresponding to a line width of the grid pattern of the release layer portion). In some embodiments, the width **W3** may be less than the width **W2**. The width **W3** may be substantially equal to the width **W2**.

Referring to FIG. 5D, the semiconductor device **15** is disposed in the cavity **120** of the encapsulant **11**. While disposing the semiconductor device **15** on the top surface of the carrier **200**, the tapered sidewall **114** may help to guide the semiconductor device **15** to the top surface of the carrier **200** to avoid a misalignment or die-shift issue. The semiconductor device **15** can be directly disposed on the top surface of the carrier **200**.

Referring to FIG. 5E through FIG. 5G, the depicted operations are similar to the operations of FIG. 4C through FIG. 4F. Referring to FIG. 5E, the encapsulant **12** is disposed or formed in and over the cavity **120** to cover the encapsulant **11** and the semiconductor device **15**. The encapsulant **12** may function as a planarization layer. The quantity of the encapsulant **12** can be controlled as a relatively lesser quantity. In some embodiments, material characteristics of the encapsulant **11** can be relatively hard, as compared to, for example, the encapsulant **12**. The encapsulant **11** may comprise a molding compound with a relatively higher amount of fillers. The encapsulant **11** may comprise a polyimide. The warpage issue can be mitigated because the encapsulant **11** can be relatively hard and the quantity of the encapsulant **12** formed in the cavity **120** is relatively less. In some embodiments, the encapsulant **12** may comprise a polyimide. The substrate **100** can act as a mold chase. Accordingly, another mold chase may be omitted. Since the encapsulant **11** may comprise a molding compound with a relatively high amount of fillers and the encapsulant **11** can be relatively hard, a rigidity of the encapsulant **11** is sufficient high to support the encapsulant **12** so as to enhance the rigidity of the whole package.

Referring to FIG. 5F, the redistribution layer **13** is formed on the encapsulant **12**.

Referring to FIG. 5G, an additional portion of the encapsulant **12** is further formed on the redistribution layer **13** and covers the redistribution layer **13**. Then, the additional portion of the encapsulant **12** is patterned to expose the redistribution layer **13**. An additional redistribution layer **13** is further formed on the encapsulant **12**. The redistribution layer **13** is surrounded by the encapsulant **12**. The connection element **17** is disposed on the redistribution layer **13**.

The redistribution layer **13** is electrically connected to the semiconductor device **15**. The connection element **17** is electrically connected to the semiconductor device **15**.

Referring to FIG. 5H, the release layer **220** and the carrier **200** are removed.

The semiconductor device package **2** depicted in FIG. 2 is then formed if the structure depicted in FIG. 5H is singulated by a singulation operation.

FIG. 6A and FIG. 6D through FIG. 6H illustrate some embodiments of a method of manufacturing the semiconductor device package **3** according to some embodiments of the present disclosure.

Referring to FIG. 6A, the method includes providing a substrate array **5**. The substrate array **5** includes a portion including an encapsulant and a portion including a release layer with a carrier. The substrate array **5** includes a plurality of substrate **100'** (as shown in FIG. 6B). Each substrate **100'** includes an encapsulant **11'**, a release layer **320**, and a carrier **300**. The encapsulant **11'** is attached to the carrier **300** via the release layer **320**. The release layer **320** is covered by the encapsulant **11'**. The release layer **320** is embedded in the encapsulant **11'**. The carrier **300** serves to support the encapsulant **11'**. In some embodiments, a plurality of the encapsulants **11'** of the substrates **100'** can be pre-designed or pre-molded. The carrier **300** may be recyclable. The volume of the encapsulant **11'** can be designed as a minimum or reduced volume to reduce manufacturing cost.

The encapsulant **11'** includes the surface **111'**, the surface **112'**, the lateral surface **113'**, and the sidewall **114'**. The sidewall **114'** may be tapered from the surface **111'** to the surface **112'**. In some embodiments, the surface **112'** of the encapsulant **11'** may be grinded. The surface **112'** of the encapsulant **11'** may not be grinded. The encapsulant **11'** defines a cavity **120'**. The sidewall **114'** of the encapsulant **11'** and a top surface of the carrier **300** define the cavity or space **120'**. The sidewall **114'** of the encapsulant **11'** and the top surface of the carrier **300** form an angle ( $\theta$ ) which is in a range from approximately  $91^\circ$  to approximately  $125^\circ$  or from approximately  $91^\circ$  to approximately  $115^\circ$ .

FIG. 6B illustrates a perspective view of the substrate array **5** according to some embodiments of the present disclosure. The substrate array **5** includes the plurality of substrates **100'**. Each substrate **100'** includes the encapsulant **11'**, the release layer **320**, and the carrier **300**. The encapsulant **11'** is attached to the carrier **300** via the release layer **320**. In some embodiments, the encapsulant **11'** may include a polyimide, a molding compound, a ceramic material, a conductive material, a metallic alloy, or other suitable materials. In some embodiments, the release layer **320** may be a thermal release film or an UV light release film. The release layer **320** may be a tape, a glue, or an adhesive.

FIG. 6C illustrates an exploded perspective view of the substrate array **5** according to some embodiments of the present disclosure. The substrate array **5** is divided into the encapsulant portion and the release layer portion with the carrier **300**. The release layer **320** is disposed on the carrier **300**.

For the encapsulant **11'** of the substrate **100'**, the surface **111'** of the encapsulant **11'** has a width **W1'**. The surface **112'** of the encapsulant **11'** has a width **W2'**. The width **W2'** is larger than the width **W1'**. The release layer **320** is disposed on the carrier **300**. The release layer **320** has a width **W3'**. In some embodiments, the width **W3'** is less than the width **W2'**.

Referring to FIG. 6D, the semiconductor device **15** is disposed into the cavity **120'** of the encapsulant **11'**. While disposing the semiconductor device **15** on the top surface of

the carrier **300**, the tapered sidewall **114'** may help to guide the semiconductor device **15** to the top surface of the carrier **300** to avoid a misalignment or die-shift issue. The semiconductor device **15** can be directly disposed on the top surface of the carrier **300**.

Referring to FIG. 6E through FIG. 6G, the depicted operations are similar to the operations of FIG. 4C through FIG. 4F. Referring to FIG. 6E, the encapsulant **12** is formed to cover the encapsulant **11'** and the semiconductor device **15**. The encapsulant **12** is formed as a planarization layer. The quantity of the encapsulant **12** can be controlled as a relatively lesser quantity. In some embodiments, material characteristics of the encapsulant **11'** can be relatively hard, as compared to, for example, the encapsulant **12**. The encapsulant **11'** may comprise a molding compound with a relatively higher amount of fillers. The encapsulant **11'** may comprise a polyimide. The warpage issue can be mitigated because the encapsulant **11'** can be relatively hard and the quantity of the encapsulant **12** formed in the cavity **120'** is relatively less. In some embodiments, the encapsulant **12** may comprise a polyimide. The substrate **100'** can act as a mold chase. Accordingly, another mold chase may be omitted. Since the encapsulant **11'** may comprise a molding compound with a relatively high amount of fillers and the encapsulant **11'** can be relatively hard, a rigidity of the encapsulant **11'** is sufficient high to support the encapsulant **12** so as to enhance the rigidity of the whole package.

Referring to FIG. 6F, the redistribution layer **13** is formed on the encapsulant **12**.

Referring to FIG. 6G, an additional portion of the encapsulant **12** is further formed on the redistribution layer **13** and covers the redistribution layer **13**. Then, the additional portion of the encapsulant **12** is patterned to expose the redistribution layer **13**. An additional redistribution layer **13** is further formed on the encapsulant **12**. The redistribution layer **13** is surrounded by the encapsulant **12**. The connection element **17** is disposed on the redistribution layer **13**. The redistribution layer **13** is electrically connected to the semiconductor device **15**. The connection element **17** is electrically connected to the semiconductor device **15**.

Referring to FIG. 6H, the release layer **320** and the carrier **300** are removed to form the recesses **116** of the encapsulant **11'**. The encapsulant **11'** defines the recesses **116**.

The semiconductor device package **3** depicted in FIG. 3 is then formed if the structure depicted in FIG. 6H is singulated by a singulation operation.

FIG. 7A illustrates a cross-sectional view of a comparative encapsulant **20** according to some embodiments of the present disclosure.

The encapsulant **20** includes a surface **201**, a surface **202**, a surface **205**, a lateral surface **203**, and a sidewall **204**. The surface **201** is opposite to the surface **205**. The surface **201** is opposite to the surface **202**. The lateral surface **203** extends between the surface **201** and the surface **205**. The sidewall **204** extends between the surface **201** and the surface **202**.

The sidewall **204** and the surface **202** define a space or a cavity **220** to accommodate or receive a semiconductor device **25** (as shown in FIG. 7B). The sidewall **204** is substantially perpendicular to the surface **202**.

FIG. 7B illustrates a cross-sectional view of the comparative encapsulant **20** with a semiconductor device **25** thereon according to some embodiments of the present disclosure.

While disposing the semiconductor device **25** on the surface **202** of the encapsulant **20**, since the sidewall **204** is substantially perpendicular to the surface **202** and is not conducive towards helping to guide the semiconductor

device **25** to the surface **202**, the semiconductor device **25** may be in a tilted position with one edge resting on the surface **202** and one edge against the sidewall **204** due to a misalignment or die-shift issue. In a worst case, the semiconductor device **25** may flip on the surface **202** of the encapsulant **20**. Accordingly, the misalignment or die-shift issue may result in a failure for packaging the semiconductor device **25**.

As used herein and not otherwise defined, the terms “substantially,” “substantial,” “approximately” and “about” are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can encompass instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can encompass a range of variation of less than or equal to  $\pm 10\%$  of that numerical value, such as less than or equal to  $\pm 5\%$ , less than or equal to  $\pm 4\%$ , less than or equal to  $\pm 3\%$ , less than or equal to  $\pm 2\%$ , less than or equal to  $\pm 1\%$ , less than or equal to  $\pm 0.5\%$ , less than or equal to  $\pm 0.1\%$ , or less than or equal to  $\pm 0.05\%$ . For example, “substantially” parallel can refer to a range of angular variation relative to  $0^\circ$  that is less than or equal to  $\pm 10^\circ$ , such as less than or equal to  $\pm 5^\circ$ , less than or equal to  $\pm 4^\circ$ , less than or equal to  $\pm 3^\circ$ , less than or equal to  $\pm 2^\circ$ , less than or equal to  $\pm 1^\circ$ , less than or equal to  $\pm 0.5^\circ$ , less than or equal to  $\pm 0.1^\circ$ , or less than or equal to  $\pm 0.05^\circ$ . For example, “substantially” perpendicular can refer to a range of angular variation relative to  $90^\circ$  that is less than or equal to  $\pm 10^\circ$ , such as less than or equal to  $\pm 5^\circ$ , less than or equal to  $\pm 4^\circ$ , less than or equal to  $\pm 3^\circ$ , less than or equal to  $\pm 2^\circ$ , less than or equal to  $\pm 1^\circ$ , less than or equal to  $\pm 0.5^\circ$ , less than or equal to  $\pm 0.1^\circ$ , or less than or equal to  $\pm 0.05^\circ$ . The term “substantially coplanar” can refer to two surfaces within micrometers of lying along a same plane, such as within  $40\ \mu\text{m}$ , within  $30\ \mu\text{m}$ , within  $20\ \mu\text{m}$ , within  $10\ \mu\text{m}$ , or within  $1\ \mu\text{m}$  of lying along the same plane.

As used herein, the singular terms “a,” “an,” and “the” may include plural referents unless the context clearly dictates otherwise. In the description of some embodiments, a component provided “on” or “over” another component can encompass cases where the former component is directly on (e.g., in physical contact with) the latter component, as well as cases where one or more intervening components are located between the former component and the latter component.

While the present disclosure has been described and illustrated with reference to specific embodiments thereof, these descriptions and illustrations are not limiting. It should be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the true spirit and scope of the present disclosure as defined by the appended claims. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the present disclosure and the actual apparatus due to manufacturing processes and tolerances. There may be other embodiments of the present disclosure which are not specifically illustrated. The specification and the drawings are to be regarded as illustrative rather than restrictive. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective, spirit and scope of the present disclosure. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it will be understood that these opera-

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tions may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the present disclosure. Accordingly, unless specifically indicated herein, the order and grouping of the operations are not limitations.

What is claimed is:

1. A semiconductor device package, comprising:  
 a semiconductor device including a top surface and a lateral surface;  
 a first encapsulant layer comprising a top surface and a tapered sidewall and surrounding the semiconductor device;  
 a second encapsulant layer in contact with the top surface and the lateral surface of the semiconductor device and the top surface and the tapered sidewall of the first encapsulant layer;  
 a redistribution layer extending through the second encapsulant layer and electrically connected to the semiconductor device, the redistribution layer including a patterned conductive layer adjacent to a top surface of the second encapsulant layer, and  
 a connection element disposed on the patterned conductive layer,  
 wherein the tapered sidewall of the first encapsulant layer surrounds the semiconductor device and forms an obtuse angle with a bottom surface of the semiconductor device,  
 wherein the patterned conductive layer of the redistribution layer has a recess with a first surface and a second surface lower than the first surface, and the second surface of the recess is lower than the top surface of the second encapsulant layer, and  
 wherein the connection element is a solder ball, and a portion of the connection element is lower than the top surface of the second encapsulant layer.
2. The semiconductor device package of claim 1, wherein the first encapsulant layer surrounds the second encapsulant layer.
3. The semiconductor device package of claim 1, wherein the redistribution layer is surrounded by the second encapsulant layer.
4. The semiconductor device package of claim 1, wherein the first encapsulant layer comprises a first surface and a second surface substantially perpendicular to the first surface, and wherein a roughness of the first surface is greater than a roughness of the second surface.
5. The semiconductor device package of claim 1, wherein the semiconductor device is exposed by the second encapsulant layer.
6. The semiconductor device package of claim 1, wherein the second encapsulant layer includes a bottom surface, and wherein the tapered sidewall of the first encapsulant layer and the bottom surface of the second encapsulant layer form an angle in a range from approximately 91° to approximately 115°.
7. The semiconductor device package of claim 1, wherein the semiconductor device has a bottom surface, and the bottom surface of the semiconductor device is exposed by the second encapsulant layer.
8. The semiconductor device package of claim 1, wherein the first encapsulant layer comprises a step structure.

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9. The semiconductor device package of claim 1, wherein the second encapsulant layer is a planarization layer.
10. The semiconductor device package of claim 9, wherein the planarization layer comprises polyimide.
11. The semiconductor device package of claim 1, wherein the patterned conductive layer is disposed on a projection area of the tapered sidewall of the first encapsulant layer.
12. The semiconductor device package of claim 11, wherein the patterned conductive layer laterally extends over the projection area of the tapered sidewall of the first encapsulant layer.
13. The semiconductor device package of claim 11, wherein the connection element is vertically aligned with the projection area of the tapered sidewall of the first encapsulant layer.
14. The semiconductor device package of claim 1, wherein the redistribution layer is disposed in the second encapsulant layer.
15. The semiconductor device package of claim 14, wherein a portion of the redistribution layer is exposed from the second encapsulant layer.
16. The semiconductor device package of claim 15, wherein the redistribution layer comprises conductive traces, pads and vias.
17. A semiconductor device package, comprising:  
 a semiconductor device including a top surface and a lateral surface;  
 a first encapsulant layer comprising a top surface and a tapered sidewall and surrounding the semiconductor device;  
 a second encapsulant layer in contact with the top surface and the lateral surface of the semiconductor device and the top surface and the tapered sidewall of the first encapsulant layer; and  
 a redistribution layer extending through the second encapsulant layer and electrically connected to the semiconductor device, the redistribution layer including a patterned conductive layer adjacent to a top surface of the second encapsulant layer,  
 wherein the tapered sidewall of the first encapsulant layer surrounds the semiconductor device and forms an obtuse angle with a bottom surface of the semiconductor device,  
 wherein the patterned conductive layer of the redistribution layer has a recess with a first surface and a second surface lower than the first surface, and the second surface of the recess is lower than the top surface of the second encapsulant layer,  
 wherein the semiconductor device includes a conductive pad protruding from the top surface of the semiconductor device, and the conductive pad of the semiconductor device is lower than the top surface of the first encapsulant layer.

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