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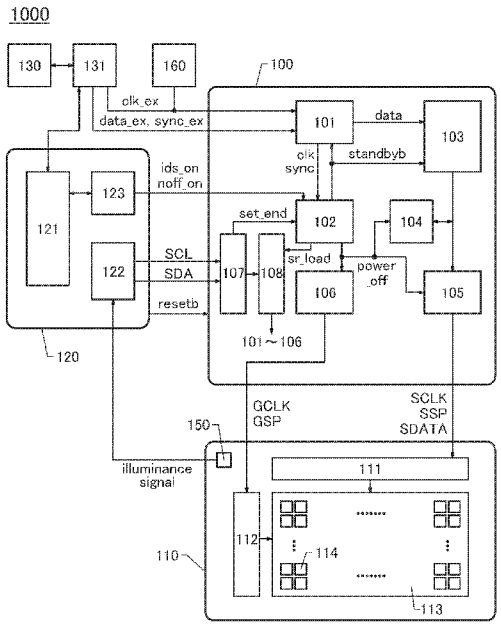
FIG. 1



(57) Abstract: A display system that occupies a small area is provided. The display system includes a display device and a display controller. The display device includes a plurality of pixels arranged in a matrix. The display controller has a function of processing image data based on setting parameters and supplying the processed image data to the display device. The setting parameters used for processing image data are determined in accordance with the row number.

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DESCRIPTION

DISPLAY SYSTEM

TECHNICAL FIELD

[0001]

One embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. One embodiment of the invention disclosed in this specification and the like also relates to a process, a machine, manufacture, or a composition of matter. In particular, one embodiment of the invention disclosed in this specification and the like relates to a semiconductor device, a display device, a display system, and the like.

[0002]

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A display device (e.g., a liquid crystal display device and a light-emitting display device), a projection device, a lighting device, an electro-optical device, a power storage device, a memory device, a semiconductor circuit, an imaging device, an electronic device, and the like may be referred to as a semiconductor device. Alternatively, they may include a semiconductor device.

BACKGROUND ART

[0003]

An active-matrix display device where a transistor for driving a display element is provided in each pixel is known. For example, an active-matrix liquid crystal display device that includes a liquid crystal element as a display element, an active-matrix light-emitting display device that includes a light-emitting element, such as an organic electroluminescent (EL) element, as a display element, and the like are known. These active-matrix display devices are easier to increase in display size or definition than simple-matrix display devices, and have an advantage in reduced power consumption and the like.

[0004]

Patent Document 1 discloses a light-emitting display device including an organic EL element as a display element.

[0005]

Moreover, there is a trend in an active matrix display device towards a larger screen, e.g., a screen diagonal of 30 inches or more, and further, the development of an active matrix display device is aimed at a screen diagonal of 60 inches or more, even at a screen diagonal of 120

inches or more. In addition, there is a trend in resolution of a screen toward higher definition, e.g., full high definition (number of pixels: 1920 × 1080; also referred to as "2K resolution", "2K1K", "2K", and the like), ultra high definition (number of pixels: 3840 × 2160; also referred to as"4K resolution", "4K2K", "4K", and the like), and super high definition (number of pixels: 7680 × 4320; also referred to as "8K resolution", "8K4K", "8K", and the like).

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2014-197522

DISCLOSURE OF INVENTION

[0007]

In order to match input color data with color development characteristics of a display device, signal correction processing is performed for each color by using a gamma value, a value shown in a look up table (LUT), or the like as a correction value. However, when a circuit for performing signal correction processing is provided for each color, the area occupied by the processing circuit increases.

[0008]

In addition, as a display device has a larger size and a higher definition, high-speed processing of signal correction is required. In particular, in a display device having a resolution of 8K or more, further improvement in the speed of the signal correction processing is required. In particular, when a display device has a structure in which a plurality of pixels controlling different colors are connected to one video signal line, setting parameters for the signal correction processing need to be switched for each row (for each scan line); thus, further improvement in the speed of the signal correction processing is required.

[0009]

An object of one embodiment of the present invention is to provide a display system having high display quality. Another object is to provide a display system with low power consumption. Another object is to provide a display system with high productivity. Another object is to provide a display system having high reliability. Another object is to provide a display system that occupies a small area. Another object is to provide a novel display system.

[0010]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other

objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0011]

One embodiment of the present invention is a display system including a display device and a display controller. The display device includes a plurality of pixels arranged in *m* rows and *n* columns (*m* and *n* are each an integer of 2 or more). The display controller has a function of processing image data based on a setting parameter and supplying the processed image data to the display device. The setting parameter used for processing image data is determined in accordance with the row number.

[0012]

Another embodiment of the present invention is a display system including the display device and the display controller. The display device includes a display portion. The display portion includes a plurality of pixels arranged in *m* rows and *n* columns, scan lines in *m* rows, and video signal lines in *n* columns. The display controller includes a setup register, a master controller, and a data processing circuit. The setup register has a function of retaining a plurality of setting parameters. The master controller has a function of controlling the setup register so that one of the plurality of setting parameters is input to the data processing circuit in accordance with the row number of the scan line. The data processing circuit has a function of processing the first image data to the second image data based on the input setting parameter. The display controller has a function of supplying the second image data to the display device.

[0013]

Another embodiment of the present invention is the display system in which the video signal line in the *j*-th column (*j* is an integer of 1 or more) is electrically connected to a pixel that controls the first color and a pixel that controls the second color included in the plurality of pixels.

[0014]

According to one embodiment of the present invention, a display system having high display quality can be provided. A display system with low power consumption can be provided. A display system with high productivity can be provided. A display system having high reliability can be provided. A display system that occupies a small area can be provided. A novel display system can be provided.

[0015]

Note that the description of these effects does not preclude the existence of other effects. One embodiment of the present invention does not have to have all the effects listed above.

Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0016]

FIG. 1 is a block diagram illustrating one embodiment of the present invention;

FIGS. 2A to 2G are block diagrams illustrating one embodiment of the present invention;

FIG. 3 is a block diagram illustrating one embodiment of the present invention;

FIG. 4 is a timing chart showing one embodiment of the present invention;

FIG. 5 is a flow chart describing one embodiment of the present invention;

FIG. 6 is a block diagram illustrating one embodiment of the present invention;

FIGS. 7A to 7D illustrate pixel configuration examples;

FIGS. 8A1 to 8C2 illustrate structure examples of a transistor;

FIGS. 9A1 to 9B2 illustrate structure examples of a transistor;

FIGS. 10A1 to 10C2 illustrate structure examples of a transistor;

FIGS. 11A to 11C illustrate a structure example of a transistor;

FIGS. 12A to 12C illustrate a structure example of a transistor;

FIGS. 13A to 13C illustrate a structure example of a transistor;

FIGS. 14A to 14D illustrate structure examples of a transistor;

FIGS. 15A to 15C illustrate a structure example of a transistor;

FIGS. 16A and 16B illustrate structure examples of a display device;

FIGS. 17A and 17B illustrate structure examples of a display device;

FIGS. 18A to 18F illustrate electronic devices; and

FIGS. 19A to 19F illustrate electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

[0017]

Embodiments will be described in detail with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Thus, the present invention should not be construed as being limited to the description in the following embodiments and example. Note that in the structures of the present invention described below, the same portions or portions

having similar functions are denoted by the same reference numerals in different drawings, and the description thereof is not repeated in some cases.

[0018]

The position, size, range, and the like of each component illustrated in the drawings and the like are not accurately represented in some cases for easy understanding of the invention. Therefore, the present invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like. For example, in the actual manufacturing process, a layer, a resist mask, or the like might be unintentionally reduced in size by treatment such as etching, which is not illustrated in some cases for easy understanding of the invention.

[0019]

Especially in a top view (also referred to as a "plan view"), a perspective view, or the like, some components might not be illustrated for easy understanding of the invention. In addition, some hidden lines and the like might not be shown.

[0020]

Ordinal numbers such as "first" and "second" in this specification and the like are used in order to avoid confusion among components and do not denote the priority or the order such as the order of steps or the stacking order. A term without an ordinal number in this specification and the like might be provided with an ordinal number in a claim in order to avoid confusion among components. A different ordinal number from an ordinal number used to denote a component in this specification and the like might be used to denote the component in a claim. Moreover, a term with an ordinal number in this specification and the like might not be provided with any ordinal number in a claim.

[0021]

In addition, in this specification and the like, the term such as an "electrode" or a "wiring" does not limit a function of the component. For example, an "electrode" is used as part of a "wiring" in some cases, and vice versa. Further, the term "electrode" or "wiring" can also mean a combination of a plurality of "electrodes" and "wirings" provided in an integrated manner.

[0022]

In this specification and the like, a transistor is an element having at least three terminals of a gate, a drain, and a source. The transistor includes a channel formation region between the drain (a drain terminal, a drain region, or a drain electrode) and the source (a source terminal, a source region, or a source electrode), and current can flow between the source and the drain through the channel formation region. Note that in this specification and the like, a channel formation region refers to a region through which current mainly flows.

[0023]

A transistor described in this specification and the like refers to an enhancement-mode (normally-off) field-effect transistor, unless otherwise specified. A transistor described in this specification and the like also refers to an n-channel transistor, unless otherwise specified. Therefore, the threshold voltage (also referred to as "V_{th}") thereof is higher than 0 V, unless otherwise specified.

[0024]

Note that the V_{th} of a transistor including a back gate in this specification and the like refers to a V_{th} obtained when the potential of the back gate is set equal to that of a source or a gate, unless otherwise specified.

[0025]

Unless otherwise specified, off-state current in this specification and the like refers to drain current of a transistor in an off state (also referred to as a non-conducting state and a cutoff state). Unless otherwise specified, the off state of an n-channel transistor means that a potential difference (hereinafter also referred to as V_g) between its gate and source when the potential of the source is regarded as a reference potential is lower than the threshold voltage V_{th}, and the off state of a p-channel transistor means that the voltage V_g between its gate and source is higher than the threshold voltage V_{th}. For example, the off-state current of an n-channel transistor sometimes refers to drain current that flows when V_g is lower than the threshold voltage (hereinafter also referred to as V_{th}).

[0026]

In the above description of off-state current, a drain may be replaced with a source. That is, the off-state current sometimes refers to a current that flows through a source of a transistor in the off state.

[0027]

In this specification and the like, the term "leakage current" sometimes expresses the same meaning as "off-state current". In this specification and the like, the off-state current sometimes refers to current that flows between a source and a drain of a transistor in the off state, for example.

[0028]

Furthermore, in this specification and the like, an explicit description "X and Y are connected" means that X and Y are electrically connected, X and Y are functionally connected, and X and Y are directly connected. Accordingly, without being limited to a predetermined connection relationship, for example, a connection relationship shown in drawings or texts, another connection relationship is included in the drawings or the texts.

[0029]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on the "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Accordingly, even when the expression "electrically connected" is used in this specification, there is a case in which no physical connection is made and a wiring is just extended in an actual circuit.

[0030]

Note that the term "over" or "under" in this specification and the like does not necessarily mean that a component is placed "directly on" or "directly below" and "directly in contact with" another component. For example, the expression "electrode B over insulating layer A" does not necessarily mean that the electrode B is on and in direct contact with the insulating layer A and can mean the case where another component is provided between the insulating layer A and the electrode B.

[0031]

In this specification, unless otherwise specified, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. In addition, unless otherwise specified, the term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to −30° and less than or equal to 30°. The term "perpendicular" or "orthogonal" indicates, unless otherwise specified, that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly also includes the case where the angle is greater than or equal to 85° and less than or equal to 95°. In addition, unless otherwise specified, the term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120°.

[0032]

In the specification and the like, the terms "identical", "the same", "equal", "uniform", and the like (including synonyms thereof) used in describing calculation values and actual measurement values allow for a margin of error of ±20 % unless otherwise specified.

[0033]

(Embodiment 1)

A structure example of a display system 1000 of one embodiment of the present invention will be described with reference to drawings.

[0034]

<Structure Example>

FIG. 1 is a block diagram illustrating the structure example of the display system 1000. The display system 1000 includes a display controller 100, a display device 110, a processor 120, a DRAM 130, a DRAM controller 131, and a clock generation circuit 160.

[0035]

The DRAM 130 has a function of retaining image data. For example, the DRAM 130 retains image data as a frame memory. In addition, the DRAM 130 retains a plurality of frames to enable processing such as image data comparison between frames and data reception/transmission between the processor 120 and the display controller 100.

[0036]

The DRAM controller 131 has a function of controlling writing and reading of the DRAM 130 and generating a control signal for the DRAM 130. The DRAM controller 131 is electrically connected to a data processing circuit 121. The clock generation circuit 160 has a function of generating a clock signal and supplying the clock signal to the display controller 100.

[0037]

[Display controller 100]

The display controller 100 includes an input I/F 101, a master controller 102, a data processing circuit 103, a frame memory 104, an output I/F 105, a timing controller 106, a register chain 107, and a setup register 108. The display controller 100 is electrically connected to the processor 120.

[0038]

The input I/F 101 has a function of receiving image data to be displayed on a display. When the image data is received using a data transmission signal (e.g., LVDS), the input I/F 101 may have a function of converting the signal standard into a signal standard which can be internally processed. In addition, the input I/F 101 has a function of receiving a clock signal. Whether the receiving operation in the input I/F 101 can be performed or not is controlled by a clock standby signal and a data standby signal from the master controller 102. Note that only DC leakage occurs when a clock receiving circuit and a data receiving circuit are in a standby state, so that power consumption during that period can be lower than that of normal operation.

[0039]

The master controller 102 has a function of controlling the operation of the display controller 100. In other words, the master controller 102 controls the operations of the input I/F

101, the data processing circuit 103, the frame memory 104, the output I/F 105, the timing controller 106, the register chain 107, and the setup register 108. The master controller 102 controls the operations of each circuit using a standby inverted signal *stanbyb* and a power supply stop signal *power-off*. In addition, the master controller 102 determines whether data setting in the register chain 107 is completed or not based on a setting completion signal *set_end* received from the register chain 107. After the data setting in the register chain 107 is completed, the master controller 102 activates a signal *sr_load* and transmits it to the setup register 108. In this manner, the data is transmitted from the register chain 107 to the setup register 108.

[0040]

The data processing circuit 103 has a function of performing image processing (correction processing) on image data. When the image data transmitted from the input I/F 101 is compressed data, decompression processing can be performed by adding a decoding function to the data processing circuit 103, for example.

[0041]

The frame memory 104 has a function of retaining image data to be transmitted to the display device 110. With this function, unnecessary data processing in the display controller 100 can be significantly reduced, and thus, power consumption can be reduced.

[0042]

The output I/F 105 has a function of transmitting image data SDATA, a synchronization clock signal SCLK, and a start pulse SSP to the display device 110. The output I/F 105 may have a circuit for converting the signal standard to be transmitted to the display device 110.

[0043]

The timing controller 106 has a function of generating control signals (a synchronization clock signal GCLK and a start pulse GSP) for a gate driver 112 included in the display device 110.

[0044]

The register chain 107 has a function of transmitting a setting parameter given by a user to the setup register 108. In addition, by providing a nonvolatile backup circuit in the register chain 107, even when power supply is stopped for a certain period and restarted, the circuit state can be immediately restored to the state before the power supply is stopped. Thus, driving with low power consumption can be achieved by stopping the power supply with high frequency (also referred to as "normally-off operation"). Although data is transmitted to the register chain 107 using an I^2C (an I^2C clock signal SCL and an I^2C data signal SDA) in the present invention, other transmission methods may be employed.

[0045]

The setup register 108 includes setting parameters for each circuit in the display controller 100. The setup register 108 has a function of transmitting the setting parameters to each circuit in the display controller 100. The parameters retained in the setup register 108 are transmitted to each circuit in the display controller 100, whereby the circuit function of the display controller 100 is determined.

[0046]

[Display device 110]

The display device 110 includes a data driver 111, a gate driver 112, and a display portion 113. The display portion 113 includes a plurality of pixels 114.

[0047]

The data driver 111 has a function of generating image information (also referred to as "image potential", "image signal", or "video signal") based on the image data SDATA, the synchronization clock signal SCLK, and the start pulse SSP supplied from the display controller 100. The data driver 111 has a function of supplying the image information to the display portion 113.

[0048]

The gate driver 112 has a function of sequentially selecting pixels 114 included in the display portion 113 based on the synchronization clock signal GCLK and the start pulse GSP supplied from the timing controller 106.

[0049]

The display device 110 may have a function of idling stop (IDS) driving. The idling stop (IDS) driving mode refers to a method in which after image data is written, rewriting of image data is stopped. This increases the interval between writing of image data and subsequent writing of image data, thereby reducing the power that would be consumed by writing of image data in that interval can be reduced.

[0050]

In the IDS driving, the frame frequency can be about 1/100 to 1/10 of the normal driving mode. For example, a still image is displayed by the same video signals in consecutive frames. Thus, the IDS driving is particularly effective for displaying a still image. In particular, a reflective liquid crystal display device does not need electric power for light emission, and accordingly the power consumption of the display device is equivalent to that in circuit operation. Thus, the power consumption of the display device can be reduced in proportion to a reduction in rewriting frequency. In addition, when an image is displayed using

IDS driving, power consumption is reduced, image flickering (flicker) is suppressed, and eyestrain can be reduced.

[0051]

In the IDS driving, it is preferable that a potential hold portion of a pixel circuit in the pixel 114 includes a transistor using an oxide semiconductor, which is one type of a metal oxide, in a semiconductor layer where a channel is formed (also referred to as OS transistor). Because the off-state current of an OS transistor is extremely low, the image potential can be easily retained for a long time.

[0052]

An optical sensor 150 has a function of measuring the illuminance of environment where the display device 110 is used. By measuring the illuminance, image display suitable for the use environment can be achieved. For example, the data processing circuit 103 and the data processing circuit 121 can perform processing such as changing the illuminance of the display and adjusting color of an image. Although the optical sensor 150 is incorporated in the display device 110 in this embodiment, the optical sensor 150 may be externally provided.

[0053]

Here, a structure example of the display device 110 will be described in detail. FIG. 2A is a block diagram illustrating the structure example of the display device 110.

[0054]

The display device 110 illustrated in FIG. 2A includes the data driver 111, the gate driver 112, and the display portion 113. Note that the data driver 111 and the gate driver 112 are collectively referred to as "driver circuit" or "peripheral driver circuit" in some cases. A variety of circuits such as a shift register, a level shifter, an inverter, a latch, a demultiplexer, an analog switch, and a logic circuit can be used as the peripheral driver circuit.

[0055]

The gate driver 112 can function as, for example, a scan line driver circuit. The data driver 111 can function as, for example, a signal line driver circuit. Some sort of circuit may be provided to face the data driver 111 with the display portion 113 positioned therebetween. Alternatively, some sort of circuit may be provided to face the gate driver 112 with the display portion 113 positioned therebeween.

[0056]

The display device 110 illustrated in FIG. 2A includes *m* wirings 116 (also referred to as "scan lines" or "gate lines") that are arranged substantially parallel to each other and whose potentials are controlled by the gate driver 112, and *n* wirings 117 (also referred to as "video signal lines", "signal lines", or "source lines") that are arranged substantially parallel to each

other and whose potentials are controlled by the data driver 111. In addition, the display portion 113 includes a plurality of pixels 114 arranged in a matrix of *m* rows and *n* columns (*m* and *n* are each an integer of 2 or more).

[0057]

In FIG. 2A, the wiring 116 in the first row, the wiring 116 in the *m*-th row, and the wiring 116 in the *i*-th row (*i* is an integer greater than or equal to 1 and less than or equal to *m*) are denoted as "wiring 116[1]", "wiring 116[*m*]", and "wiring 116[*i*]", respectively. Similarly, the wiring 117 in the first column, the wiring 117 in the *n*-th column, and the wiring 117 in the *j*-th column (*j* is an integer greater than or equal to 1 and less than or equal to *n*) are denoted as "wiring 117[1]", "wiring 117[*n*]", and "wiring 117[*j*]", respectively. The pixel 114 in the *i*-th row and the *j*-th column is denoted as "pixel 114[*i*,*j*]".

[0058]

A plurality of pixels 114 arranged in the *i*-th row are electrically connected to the wiring 116[*i*]. A plurality of pixels 114 arranged in the *j*-th column are electrically connected to the wiring 117[*j*].

[0059]

The pixel 114 can function as a sub pixel. Full-color display can be achieved when at least three pixels 114 collectively function as one pixel 115, as illustrated in FIG. 2G. The three pixels 114 each control the transmittance, reflectance, and amount of emitted light, or the like of red light (R), green light (G), or blue light (B). The light colors controlled by the three pixels 114 are not limited to the combination of red, green, and blue, and may be yellow (Y), cyan (C), and magenta (M).

[0060]

A pixel 114 that controls white light (W) may be added to the pixels controlling red light, green light, and blue light so that the four pixels 114 will collectively function as one pixel 115. The addition of the pixel 114 that controls white light can heighten the luminance of the display image. FIG. 2B illustrates an example where four pixels 114, the pixels 114[*i*,*j*], 114[*i*+1,*j*], 114[*i*,*j*+1], and 114[*i*+1,*j*+1], are collectively function as one pixel 115. FIG. 2E illustrates an example where four pixels 114, the pixels 114[*i*,*j*], 114[*i*+1,*j*], 114[*i*+2,*j*], and 114[i+3,*j*], are collectively function as one pixel 115.

[0061]

As illustrated in FIGS. 2C and 2F, the pixel 114 that controls yellow light may be provided instead of the pixel 114 that controls white light. Alternatively, as illustrated in FIG. 2D, the pixels 114 that control the light of yellow, cyan, magenta, and white may be combined.

[0062]

When the number of the pixels 114 functioning as one pixel 115 is increased to use red, green, blue, yellow, cyan, and magenta in appropriate combination, more variety of halftones can be expressed.

[0063]

When the pixels 114 that control different colors are used in appropriate combination, the color gamut of various standards can be reproduced. For example, the display device of one embodiment of the present invention can reproduce the color gamut of the following standards: the Phase Alternating Line (PAL) or National Television System Committee (NTSC) standard used for TV broadcasting; the standard RGB (sRGB) or Adobe RGB standard used widely for display devices in electronic devices such as personal computers, digital cameras, and printers; the International Telecommunication Union Radiocommunication Sector Broadcasting Service (Television) 709 (ITU-R BT.709) standard used for high-definition televisions (HDTV, also referred to Hi-Vision); the Digital Cinema Initiatives P3 (DCI-P3) standard used for digital cinema projection; and the ITU-R BT.2020 (Recommendation 2020 (REC.2020)) standard used for ultra-high-definition televisions (UHDTV, also referred to as Super Hi-Vision); and the like.

[0064]

Using the pixels 115 arranged in a 1920 × 1080 matrix, the display device 110 can display an image with "full high definition" (also referred to as "2K resolution", "2K1K", "2K", and the like). Using the pixels 115 arranged in a 3840 × 2160 matrix, the display device 110 can display an image with "ultra high definition" (also referred to as "4K resolution", "4K2K", "4K", and the like). Using the pixels 115 arranged in a matrix of 7680 × 4320, the display device 110 can display an image with "super high definition" (also referred to as "8K resolution", "8K4K", "8K", and the like). Using a larger number of pixels 115, the display device 110 can display an image with 16K or 32K resolution.

[0065]

[Processor 120]

The processor 120 includes the data processing circuit 121, a register value generation circuit 122, and a processor controller 123.

[0066]

The processor 120 has a function of controlling the DRAM controller 131 to transmit necessary image data from the DRAM 130 to the display controller 100. In addition, the processor 120 has a function of generating a control signal for the display controller 100.

[0067]

The data processing circuit 121 has a function of performing processing on image data and on signals related to system control. The data processing circuit 121 can add a display effect to image data.

[0068]

The register value generation circuit 122 has a function of generating setting parameters for the setup register 108 in the display controller 100. For example, the register value generation circuit 122 regenerates parameters for the setup register 108 based on the illuminance of ambient light detected by the optical sensor 150 in the display device 110, and feeds the parameters back to the display controller 100. In this manner, setting parameters suitable for use environment can be generated in real time.

[0069]

When an application that displays still image is started or when there is no change in an image between different frames in a moving image, the processor controller 123 can activate *ids_on* to perform idling stop driving, which enables display with low power consumption. In addition, when the display system is in a sleep mode or a mode displaying no image, the processor controller 123 can activate *noff_on* to perform the normally-off operation, which enables system operation with lower power consumption than in the IDS mode.

[0070]

<Operation Example>

Next, an operation example of the display system 1000 will be described below. In this embodiment, an operation example where one pixel 115 includes four pixels 114 is described. Specifically, the operation of changing the setting parameters for the data processing circuit 103 for each row of the display portion 113 with 8K resolution, in the case where the pixel 115 has the structure of FIG. 2E, will be described.

[0071]

FIG. 3 is a block diagram illustrating the connection relation among a context generation circuit 240 (part of the master controller 102), the setup register 108, the data processing circuit 103, the output I/F 105, and the data driver 111 included in the display device 110. FIG. 4 is a timing chart showing the operation of the block diagram in FIG. 3. FIG. 5 is a flow chart describing an operation example of the display system 1000.

[0072]

The setup register 108 includes a setup register 229, a latch group 221, a latch group 222, a latch group 223, and a latch group 224. The latch groups 221 to 224 each include one or more latches 220.

[0073]

The latch 220 has a function of retaining input information. A backup circuit including nonvolatile memory for the latch 220 may be provided in or separated from the latch 220. The information retained in the latch 220 is stored in the nonvolatile memory before the power supply is stopped so that the information is written from the nonvolatile memory to the latch 220 at the time of restarting the power supply. In this manner, the display system 1000 can be quickly restored to the state before the power supply is stopped at the time of restarting the power supply.

[0074]

The latch group 221 retains p setting parameters Q0 (Q0[0] to Q0[p−1]) (p is an integer of 1 or more) for performing correction processing in the data processing circuit 103, for example, on red image data.

[0075]

The latch group 222 retains p setting parameters Q1 (Q1[0] to Q1[p−1]) (p is an integer of 1 or more) for performing correction processing in the data processing circuit 103, for example, on green image data.

[0076]

The latch group 223 retains p setting parameters Q2 (Q2[0] to Q2[p−1]) (p is an integer of 1 or more) for performing correction processing in the data processing circuit 103, for example, on blue image data.

[0077]

The latch group 224 stores p setting parameter Q3 (Q3[0] to Q3[p−1]) (p is an integer of 1 or more) for applying correction processing in the data processing circuit 103, for example, on white data.

[0078]

A selector 230 has a function of outputting one setting parameter selected from the four setting parameters (Q0, Q1, Q2, and Q3) as a setting parameter Q (Q[0] to Q[p−1]) in accordance with a context signal *context*[1:0] output from the context generation circuit 240.

[0079]

The context generation circuit 240 has a function of selecting one of an externally-generated context signal *ex_context*[1:0] input from the outside of the display controller 100 and a context signal generated in an internal context generation circuit 241, and outputting the signal as the context signal *context*[1:0].

[0080]

In addition, the context generation circuit 240 has a function of counting the row number after a signal *sync* that indicates the start of frame processing becomes active (e.g., H potential). The context generation circuit 240 has a function of generating an internally generated context signal based on the row number when one or both of an input data enable signal *In_en* and an output data enable signal *Out_en* is/are active (e.g., H potential).

[0081]

The master controller 102 has a function of detecting the row number *i* of the wiring 116 (the wiring 116 in the *i*-th row) selected in conjunction with the timing controller 106.

[0082]

As an input data *In*, the master controller 102 controls the setup register 108 so that red image data R is input to the data processing circuit 103 when the row number *i* corresponds to $4x+1$ (*x* is an integer of 0 or more). The master controller 102 controls the setup register 108 so that green image data G is input to the data processing circuit 103 when the row number *i* corresponds to $4x+2$. The master controller 102 controls the setup register 108 so that blue image data B is input to the data processing circuit 103 when the row number *i* corresponds to $4x+3$. The master controller 102 controls the setup register 108 so that white image data W is input to the data processing circuit 103 when the row number *i* corresponds to $4x+4$.

[0083]

As a setting parameter Q, the master controller 102 controls the setup register 108 so that the setting parameter Q0 retained in the setup register 108 is input to the data processing circuit 103, when the row number *i* corresponds to $4x+1$. The master controller 102 controls the setup register 108 so that the setting parameter Q1 retained in the setup register 108 is input to the data processing circuit 103, when the row number *i* corresponds to $4x+2$. The master controller 102 controls the setup register 108 so that the setting parameter Q2 retained in the setup register 108 is input to the data processing circuit 103, when the row number *i* corresponds to $4x+3$. The master controller 102 controls the setup register 108 so that the setting parameter Q3 retained in the setup register 108 is input to the data processing circuit 103, when the row number *i* corresponds to $4x+4$.

[0084]

Thus, the master controller 102 has a function of supplying a signal (a context signal) for determining the setting parameter Q in accordance with the row number to the setup register 108, and the setup register 108 has a function of inputting the determined setting parameter Q to the data processing circuit 103 in accordance with the signal.

[0085]

The data processing circuit 103 has a function of performing correction processing (processing) determined by the setting parameter Q[0] to Q[n–1] on the input data *In* (image data), and outputting the data as an output data *Out* (corrected image data). In FIG. 4, image data R, G, B, and W corrected (processed) by the data processing circuit 103 are denoted as image data R', G', B', and W'. In FIG. 4, the numbers following each of the image data R, G, B, and W indicate the column numbers.

[0086]

The input data enable signal *In_en* becomes active (e.g., H potential) during a data period in which the input data *In* is valid. The output data enable signal *Out_en* becomes active (e.g., H potential) during a data period in which the output data *Out* is valid. Note that the signals are not limited to the signals *In_en* and *Out_en*, and other signals can be substituted as long as the start time and the end time of data processing can be determined.

[0087]

[Step 1]

Whether the signal *sync* is active or not is determined (See Step S601 in FIG. 5).

[0088]

[Step 2]

When the signal *sync* is active, a 2 bit counter signal *In_en_cnt*[1:0] that counts the row number is reset (Step S602).

[0089]

The signal *In_en_cnt*[1:0] determines the current row number *i* in the first to fourth rows, for every four rows. The row number is determined as the first row ((4*x*+1)-th row) when the signals *In_en_cnt*[0] and *In_en_cnt*[1] are both L potential. The row number is determined as the second row ((4*x*+2)-th row) when the signal *In_en_cnt*[0] is H potential and the signal *In_en_cnt*[1] is L potential. The row number is determined as the third row ((4*x*+3)-th row) when the signal *In_en_cnt*[0] is L potential and the signal *In_en_cnt*[1] is H potential. The row number is determined as the fourth row ((4*x*+4)-th row) when the signals *In_en_cnt*[0] and *In_en_cnt*[1] are both H potential.

[0090]

[Step 3]

The value of the signal *context*[1:0] is determined in accordance with the signal *In_en_cnt*[1:0] (Step S603). In this embodiment, the signal *context*[1:0] has the same value as the signal *In_en_cnt*[1:0].

[0091]

[Step 4]

The setting parameter Q (any one of Q0 to Q3) is determined in accordance with the value of the signal *context*[1:0] (Step S604). When the signal *context*[1:0] is 0, the setting parameter Q0 retained in the latch group 221 is used as the setting parameter Q. When the signal *context*[1:0] is 1, the setting parameter Q1 retained in the latch group 222 is used as the setting parameter Q. When the signal *context*[1:0] is 2, the setting parameter Q2 retained in the latch group 223 is used as the setting parameter Q. When the signal *context*[1:0] is 3, the setting parameter Q3 retained in the latch group 224 is used as the setting parameter Q.

[0092]

[Step 5]

The setting parameter Q is set to the data processing circuit 103 (Step S605).

[0093]

[Step 6]

The input data *In* is corrected by the data processing circuit 103 in accordance with the setting parameter Q and the output data *Out* is generated (Step S606).

[0094]

[Step 7]

The output data *Out* is transmitted to the data driver 111 in the display device 110 through the output I/F 105 (Step S607).

[0095]

[Step 8]

Next, 1 is added to the signal *In_en_cnt*[1:0] (Step S608). If the signal *In_en_cnt*[1:0] before adding 1 is 3, the signal *In_en_cnt*[1:0] is set to 0.

[0096]

By repeating the Steps S601 to S608, image data appropriately corrected for each color can be provided to the display device 110. According to one embodiment of the present invention, a display device having a high display quality can be achieved. According to one embodiment of the present invention, a display system that occupies a small area can be achieved.

[0097]

In this embodiment, the operation example where one pixel 115 includes four pixels 114 is described. However, one embodiment of the present invention is not limited thereto, and in the case where one pixel 115 includes k pixels 114 (k is an integer of 2 or more), the above structure example and the operation example can be modified as appropriate.

[0098]

<Modification Example>

FIG. 6 is a block diagram illustrating a display system 1000A which is a modification example of the display system 1000. The display system 1000A includes a touch sensor 140 and a touch sensor controller 109 in addition to the structure of the display system 1000.

[0099]

The touch sensor 140 is provided to overlap with the display portion 113. The touch sensor 140 has a function of converting an input operation by a user into an electrical signal and outputting the electric signal to the data processing circuit 121 included in the processor 120. The touch sensor controller 109 is provided in the display controller 100, and has a function of supplying a signal for controlling the touch sensor 140.

[0100]

The data processing circuit 121 adds display effect to image data, and performs user interface processing such as application operation, based on the input information from the touch sensor 140.

[0101]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and the like.

[0102]

(Embodiment 2)

In this embodiment, structure examples of the pixel 114 are described with reference to the drawings.

[0103]

FIGS. 7A to 7D illustrate circuit configuration examples that can be used for the pixel 114. The pixel 114 includes a pixel circuit 534 and a display element 462.

[0104]

[Display element]

Various display elements can be used as the display element 462. Examples of display elements include display elements containing a display medium whose contrast, luminance, reflectance, transmittance, or the like is changed by electrical or magnetic effect, such as an electroluminescent (EL) element (e.g., an organic EL element, an inorganic EL element, or an EL element including both organic and inorganic materials), an LED (e.g., a white LED, a red LED, a green LED, and a blue LED), a transistor (a transistor that emits light depending on current), an electron emitter, a liquid crystal element, electronic ink, an electrophoretic element, a grating light valve (GLV), a display element using microelectromechanical systems (MEMS), a digital micromirror device (DMD), a digital micro shutter (DMS), MIRASOL (registered trademark), an

interferometric modulation (IMOD) element, a MEMS shutter display element, an optical-interference-type MEMS display element, an electrowetting element, a piezoelectric ceramic display, and a display element using a carbon nanotube. Moreover, quantum dots may be used for the display element.

[0105]

Examples of display devices using EL elements as the display element 462 include an EL display. Examples of display devices including electron emitters include a field emission display (FED) and an SED-type flat panel display (SED: surface-conduction electron-emitter display). Examples of display devices including quantum dots include a quantum dot display. Examples of display devices including liquid crystal elements include a liquid crystal display (e.g., a transmissive liquid crystal display, a transflective liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, and a projection liquid crystal display). Examples of display devices including electronic ink, electronic liquid powder (registered trademark), or electrophoretic elements include electronic paper. Other examples of display devices are a plasma display panel (PDP), a retina scanning type projector, and a display device including a micro LED.

[0106]

In a transflective liquid crystal display and a reflective liquid crystal display, some or all of pixel electrodes function as reflective electrodes. For example, some or all of pixel electrodes are formed to contain aluminum, silver, or the like. In such a case, a memory circuit such as SRAM can be provided under the reflective electrodes. Thus, power consumption can be further reduced.

[0107]

In the case of using an LED, graphene or graphite may be provided under an electrode or a nitride semiconductor of the LED. Graphene or graphite may be a multilayer film in which a plurality of layers are stacked. Providing graphene or graphite in the above manner facilitates formation of a nitride semiconductor thereover, such as an n-type GaN semiconductor layer including crystals. Furthermore, a p-type GaN semiconductor layer including crystals or the like can be provided thereover, and thus the LED can be formed. Note that an AlN layer may be provided between the n-type GaN semiconductor layer including crystals and graphene or graphite. The GaN semiconductor layers included in the LED may be formed by MOCVD. Note that when graphene is provided, the GaN semiconductor layers included in the LED can also be formed by a sputtering method.

[0108]

[Pixel Circuit]

[Example of pixel circuit for light-emitting display device]

The pixel circuit 534 illustrated in FIG. 7A includes a transistor 461, a capacitor 463, a transistor 468, and a transistor 464. The pixel circuit 534 in FIG. 7B is electrically connected to a light-emitting element that can function as the display element 462.

[0109]

There is no particular limitation on the transistor used as the transistors 461, 468, and 464. For example, a transistor using amorphous silicon for a semiconductor layer where a channel is formed, or an OS transistor may be used.

[0110]

One of a source and a drain of the transistor 461 is electrically connected to the wiring 117. A gate of the transistor 461 is electrically connected to the wiring 116. The wiring 117 supplies a video signal.

[0111]

The transistor 461 has a function of controlling writing of a video signal to a node 465.

[0112]

One of a pair of electrodes of the capacitor 463 is electrically connected to the node 465, and the other is electrically connected to a node 467. The other of the source and the drain of the transistor 461 is electrically connected to the node 465.

[0113]

The capacitor 463 functions as a storage capacitor for storing data written to the node 465.

[0114]

One of a source and a drain of the transistor 468 is electrically connected to a potential supply line VL_a, and the other is electrically connected to the node 467. A gate of the transistor 468 is electrically connected to the node 465.

[0115]

One of a source and a drain of the transistor 464 is electrically connected to a potential supply line V0, and the other is electrically connected to the node 467. A gate of the transistor 464 is electrically connected to the wiring 116.

[0116]

As the display element 462, an organic electroluminescent element (organic EL element) can be used, for example. Note that the display element 462 is not limited thereto and may be an inorganic EL element containing an inorganic material, for example.

[0117]

When a light-emitting element such as an organic EL or an inorganic EL is used as the display element 462, one of an anode or a cathode of the display element 462 is electrically connected to a potential supply line VL_b, and the other is electrically connected to the node 467.

[0118]

A high power supply potential VDD is supplied to one of the potential supply line VL_a and the potential supply line VL_b, and a low power supply potential VSS is supplied to the other, for example.

[0119]

In the display device including the pixel 114 in FIG. 7A, the pixels 114 are sequentially selected row by row by the gate driver 112, so that the transistors 461 and 464 are turned on and a video signal is written to the node 465.

[0120]

The pixel 114 in which the data has been written to the node 465 is brought into a holding state when the transistors 461 and 464 are turned off. The amount of current flowing between the source electrode and the drain electrode of the transistor 468 is controlled in accordance with the potential of the data written to the node 465. The display element 462 (light-emitting element) emits light with a luminance corresponding to the amount of flowing current. This operation is sequentially performed row by row; thus, an image can be displayed.

[0121]

As illustrated in FIG. 7C, each of the transistors 461, 464, and 468 may be a transistor with a back gate. In each of the transistors 461 and 464 in FIG. 7C, the gate is electrically connected to the back gate; thus, the gate and the back gate always have the same potential. The back gate of the transistor 468 is electrically connected to the node 467; thus, the back gate always has the same potential as the node 467.

[0122]

[Example of pixel circuit for liquid crystal display device]

The pixel circuit 534 illustrated in FIG. 7B includes the transistor 461 and the capacitor 463. The pixel circuit 534 illustrated in FIG. 7B is electrically connected to a liquid crystal element that can function as the display element 462.

[0123]

The potential of one of a pair of electrodes of the display element 462 is set as appropriate according to the specifications of the pixel circuit 534. For example, one of the pair of electrodes of the display element 462 may be supplied with a common potential, or may have the same potential as a capacitor line CL which is described later. Alternatively, a potential

supplied to one of the pair of electrodes of the display element 462 may be different among the pixels 532. The other of the pair of electrodes of the display element 462 is electrically connected to a node 466. The alignment state of the display element 462 depends on data written to the node 466.

[0124]

Examples of a method for driving the display device including the display element 462 include a twisted nematic (TN) mode, a super-twisted nematic (STN) mode, a vertical alignment (VA) mode, an axially symmetric aligned micro-cell (ASM) mode, an optically compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, an MVA mode, a patterned vertical alignment (PVA) mode, an in-plane switching (IPS) mode, an FFS mode, a VA-IPS mode, and a transverse bend alignment (TBA) mode. Other examples of the method for driving the display device include an electrically controlled birefringence (ECB) mode, a polymer-dispersed liquid crystal (PDLC) mode, a polymer network liquid crystal (PNLC) mode, and a guest-host mode. Note that one embodiment of the present invention is not limited thereto, and various liquid crystal elements and driving methods can be employed.

[0125]

The liquid crystal element controls transmission or non-transmission of light utilizing an optical modulation action of liquid crystal. The optical modulation action of a liquid crystal is controlled by an electric field applied to the liquid crystal (including a horizontal electric field, a vertical electric field, and an oblique electric field). When a liquid crystal element is used as the display element 462, thermotropic liquid crystal, low-molecular liquid crystal, high-molecular liquid crystal, polymer dispersed liquid crystal, ferroelectric liquid crystal, antiferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

[0126]

As the liquid crystal material, either of a positive liquid crystal and a negative liquid crystal may be used, and an appropriate liquid crystal material can be used depending on the mode or design to be used.

[0127]

An alignment film can be provided to adjust the alignment of a liquid crystal. In the case where a horizontal electric field mode is employed, a liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is a liquid crystal phase that is generated just before a cholesteric phase changes into an isotropic phase while

temperature of cholesteric liquid crystal is increased. Since the blue phase is only generated within a narrow range of temperatures, a liquid crystal composition in which a chiral material is mixed to account for several weight percent or more is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition that includes the liquid crystal exhibiting a blue phase and a chiral material has a short response time and optical isotropy, which makes the alignment process unnecessary and the viewing angle dependence small. In addition, an alignment film does not need to be provided and rubbing treatment is thus not necessary; accordingly, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device in the manufacturing process can be reduced. Thus, productivity of the liquid crystal display device can be increased.

[0128]

Note that when a guest-host mode liquid crystal material is used for the liquid crystal element, a functional member such as a light diffusion layer or a polarizing plate is not necessarily provided. Accordingly, the productivity of the display device can be increased. In addition, since a functional member such as a polarizing plate is unnecessary, the luminance of reflected light, the amount of transmitted light, and the like of the display portion 113 can be increased. Accordingly, the visibility of the display device can be increased.

[0129]

The on and off states (bright and dark states) of a reflective liquid crystal display device including a circularly polarizing plate are switched depending on the alignment direction of the major axes of liquid crystal molecules: a direction substantially perpendicular to a substrate or a direction substantially parallel to the substrate. In general, it is difficult to use a liquid crystal element that operates in a horizontal electric field mode such as an IPS mode in a reflective liquid crystal display device because the major axes of liquid crystal molecules in the liquid crystal element are aligned in a direction substantially parallel to a substrate in both of the on and off states.

[0130]

The on and off states of a liquid crystal element that operates in a horizontal electric field mode such as a VA-IPS mode are switched depending on the alignment direction of the major axes of liquid crystal molecules: a direction substantially perpendicular to a substrate or a direction substantially parallel to the substrate. Thus, when a liquid crystal element that operates in a horizontal electric field mode is used in a reflective liquid crystal display device, the liquid crystal element preferably operates in a VA-IPS mode.

[0131]

It is also possible to use a method called domain multiplication or multi-domain design, in which the pixel 114 is divided into several regions and molecules are aligned in different directions in their respective regions.

[0132]

The specific resistance of the liquid crystal material is higher than or equal to 1×10^9 Ω·cm, preferably higher than or equal to 1×10^{11} Ω·cm, further preferably higher than or equal to 1×10^{12} Ω·cm. Note that the specific resistance in this specification is measured at 20 °C.

[0133]

In the pixel circuit 534 in the *i*-th row and the *j*-th column, one of the source and the drain of the transistor 461 is electrically connected to the wiring 117, and the other is electrically connected to the node 466. The gate of the transistor 461 is electrically connected to the wiring 116. The wiring 117 supplies a video signal. The transistor 461 has a function of controlling writing of a video signal to the node 466.

[0134]

One of a pair of electrodes of the capacitor 463 is electrically connected to a wiring to which a specific potential is supplied (hereinafter referred to as capacitor line CL), and the other is electrically connected to the node 466. The potential of the capacitor line CL is set as appropriate in accordance with the specifications of the pixel circuit 534. The capacitor 463 has a function as a storage capacitor for storing data written to the node 466.

[0135]

For example, in the display device 110 including the pixel circuits 534 in FIG. 7B, the pixel circuits 534 are sequentially selected row by row by the gate driver 112, so that the transistor 461 is turned on and a video signal is written to the node 466.

[0136]

The pixel circuit 534 in which the video signal has been written to the node 466 is brought into a holding state when the transistor 461 is turned off. This operation is sequentially performed row by row; thus, an image can be displayed on the display portion 113.

[0137]

As illustrated in FIG. 7D, the transistor 461 may be a transistor with a back gate. In the transistor 461 in FIG. 7D, the gate is electrically connected to the back gate; thus, the gate and the back gate always have the same potential.

[0138]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and the like.

[0139]

(Embodiment 3)

In this embodiment, examples of a transistor that can be used for the display device 110 and the like described in the above embodiments will be described with reference to drawings.

[0140]

The display device 110 and the like of one embodiment of the present invention can be fabricated by using a transistor with any of various structures, such as a bottom-gate transistor, a top-gate transistor, or the like. For example, a planar transistor or a staggered transistor may be used. Therefore, a material for a semiconductor layer or the structure of a transistor can be easily changed depending on the existing production line.

[0141]

[Bottom-gate transistor]

FIG. 8A1 is a cross-sectional view of a transistor 310 that is a channel-protective transistor, which is a type of bottom-gate transistor. In FIG. 8A1, the transistor 310 is formed over a substrate 371. The transistor 310 includes an electrode 322 over the substrate 371 with an insulating layer 372 provided therebetween. The transistor 310 includes a semiconductor layer 324 over the electrode 322 with an insulating layer 326 provided therebetween. The electrode 322 can function as a gate electrode. The insulating layer 326 can function as a gate insulating layer.

[0142]

The transistor 310 includes an insulating layer 327 over a channel formation region in the semiconductor layer 324. The transistor 310 includes an electrode 344a and an electrode 344b which are partly in contact with the semiconductor layer 324 and over the insulating layer 326. The electrode 344a can function as one of a source electrode and a drain electrode. The electrode 344b can function as the other of the source electrode and the drain electrode. Part of the electrode 344a and part of the electrode 344b are formed over the insulating layer 327.

[0143]

The insulating layer 327 can function as a channel protective layer. With the insulating layer 327 provided over the channel formation region, the semiconductor layer 324 can be prevented from being exposed at the time of forming the electrodes 344a and 344b. Thus, the channel formation region in the semiconductor layer 324 can be prevented from being etched at the time of forming the electrodes 344a and 344b. In accordance with one embodiment of the present invention, a transistor with favorable electrical characteristics can be provided.

[0144]

The transistor 310 includes an insulating layer 328 over the electrode 344a, the electrode 344b, and the insulating layer 327 and further includes an insulating layer 329 over the insulating layer 328.

[0145]

In the case where a semiconductor such as silicon is used for the semiconductor layer 324, a layer that functions as an n-type semiconductor or a p-type semiconductor is preferably provided between the semiconductor layer 324 and the electrode 344a and between the semiconductor layer 324 and the electrode 344b. The layer that functions as an n-type semiconductor or a p-type semiconductor can function as the source region or the drain region in the transistor.

[0146]

The insulating layer 329 is preferably formed using a material that can prevent or reduce diffusion of impurities into the transistor from the outside. The formation of the insulating layer 329 may also be omitted.

[0147]

A transistor 311 illustrated in FIG. 8A2 is different from the transistor 310 in that an electrode 323 that can function as a back gate electrode is provided over the insulating layer 329. The electrode 323 can be formed using a material and a method similar to those of the electrode 322.

[0148]

In general, a back gate electrode is formed using a conductive layer and positioned so that a channel formation region of a semiconductor layer is positioned between a gate electrode and the back gate electrode. Thus, the back gate electrode can function in a manner similar to that of the gate electrode. The potential of the back gate electrode may be the same as that of the gate electrode or may be a ground (GND) potential or a predetermined potential. By changing the potential of the back gate electrode independently of the potential of the gate electrode, the threshold voltage of the transistor can be changed.

[0149]

The electrode 322 and the electrode 323 can each function as a gate electrode. Thus, the insulating layers 326, 328, and 329 can each function as a gate insulating layer. The electrode 323 may also be provided between the insulating layers 328 and 329.

[0150]

In the case where one of the electrode 322 and the electrode 323 is simply referred to as a "gate electrode", the other can be referred to as a "back gate electrode". For example, in the transistor 311, in the case where the electrode 323 is referred to as a "gate electrode", the

electrode 322 is referred to as a "back gate electrode". In the case where the electrode 323 is used as a "gate electrode", the transistor 311 is a kind of top-gate transistor. Alternatively, one of the electrode 322 and the electrode 323 may be referred to as a "first gate electrode", and the other may be referred to as a "second gate electrode".

[0151]

By providing the electrode 322 and the electrode 323 with the semiconductor layer 324 provided therebetween and setting the potentials of the electrode 322 and the electrode 323 to be the same, a region of the semiconductor layer 324 through which carriers flow is enlarged in the film thickness direction; thus, the number of transferred carriers is increased. As a result, the on-state current and field-effect mobility of the transistor 311 are increased.

[0152]

Therefore, the transistor 311 has a comparatively high on-state current for its area. That is, the area of the transistor 311 can be small for a required on-state current. According to one embodiment of the present invention, the area of a transistor can be reduced. Therefore, according to one embodiment of the present invention, a semiconductor device having a high degree of integration can be provided.

[0153]

The gate electrode and the back gate electrode are formed using conductive layers and thus each have a function of preventing an electric field generated outside the transistor from influencing the semiconductor layer in which the channel is formed (in particular, an electric field blocking function against static electricity and the like). When the back gate electrode is formed larger than the semiconductor layer such that the semiconductor layer is covered with the back gate electrode, the electric field blocking function can be enhanced.

[0154]

Since the gate electrode and the back gate electrode each have a function of blocking an electric field from the outside, charges of charged particles and the like generated above and below the transistor do not influence the channel formation region of the semiconductor layer. Thus, degradation induced by a stress test (e.g., a negative gate bias temperature (NGBT) stress test where negative voltage is applied to a gate (this stress test is also referred to as "NBT" or "NBTS")) is reduced. In addition, the gate electrode and the back gate electrode can block an electric field generated from the drain electrode so as not to affect the semiconductor layer. Thus, changes in the rising voltage of on-state current due to changes in drain voltage can be suppressed. Note that this effect is significant when a potential is applied to the gate electrode and the back gate electrode.

[0155]

Before and after a positive gate bias temperature (PGBT) stress test where positive voltage is applied to a gate (this stress test is also referred to as "PBT" or "PBTS"), a transistor including a back gate electrode has a smaller change in threshold voltage than a transistor including no back gate.

[0156]

The BT stress test such as NGBT or PGBT is a kind of accelerated test and can evaluate, in a short time, a change by long-term use (i.e., a change over time) in characteristics of transistors. In particular, the amount of change in threshold voltage of the transistor between before and after the BT stress test is an important indicator when examining the reliability of the transistor. If the amount of change in the threshold voltage between before and after the BT stress test is small, the transistor has higher reliability.

[0157]

By providing the gate electrode and the back gate electrode and setting the potentials of the gate electrode and the back gate electrode to be the same, the change in threshold voltage is reduced. Accordingly, variation in electrical characteristics among a plurality of transistors is also reduced.

[0158]

In the case where light is incident on the back gate electrode side, when the back gate electrode is formed using a light-blocking conductive film, light can be prevented from entering the semiconductor layer from the back gate electrode side. Therefore, photodegradation of the semiconductor layer can be prevented and deterioration in electrical characteristics of the transistor, such as a shift of the threshold voltage, can be prevented.

[0159]

According to one embodiment of the present invention, a transistor with favorable reliability can be provided. Moreover, a semiconductor device with favorable reliability can be provided.

[0160]

FIG. 8B1 is a cross-sectional view of a channel-protective transistor 320 that is a type of bottom-gate transistor. The transistor 320 has substantially the same structure as the transistor 310 but is different from the transistor 310 in that the insulating layer 327 covers the semiconductor layer 324. The semiconductor layer 324 is electrically connected to the electrode 344a through an opening formed by selectively removing part of the insulating layer 327 which overlaps with the semiconductor layer 324. The semiconductor layer 324 is electrically connected to the electrode 344b through another opening formed by selectively removing part of the insulating layer 327 which overlaps with the semiconductor layer 324. A

region of the insulating layer 327 which overlaps with the channel formation region can function as a channel protective layer.

[0161]

A transistor 321 illustrated in FIG. 8B2 is different from the transistor 320 in that the electrode 323 that can function as a back gate electrode is provided over the insulating layer 329.

[0162]

With the insulating layer 327, the semiconductor layer 324 can be prevented from being exposed at the time of forming the electrodes 344a and 344b. Thus, the semiconductor layer 324 can be prevented from being etched at the time of forming the electrodes 344a and 344b.

[0163]

The length between the electrode 344a and the electrode 322 and the length between the electrode 344b and the electrode 322 in the transistors 320 and 321 are larger than those in the transistors 310 and 311. Thus, the parasitic capacitance generated between the electrode 344a and the electrode 322 can be reduced. Moreover, the parasitic capacitance generated between the electrode 344b and the electrode 322 can be reduced. According to one embodiment of the present invention, a transistor with favorable electrical characteristics can be provided.

[0164]

A transistor 325 illustrated in FIG. 8C1 is a channel-etched transistor that is a type of bottom-gate transistor. In the transistor 325, the electrodes 344a and 344b are formed without providing the insulating layer 327. Thus, part of the semiconductor layer 324 that is exposed at the time forming the electrodes 344a and 344b is etched in some cases. However, since the insulating layer 327 is not provided, the productivity of the transistor can be increased.

[0165]

A transistor 332 illustrated in FIG. 8C2 is different from the transistor 325 in that the electrode 323 which can function as a back gate electrode is provided over the insulating layer 329.

[0166]

[Top-gate transistor]

FIG. 9A1 is a cross-sectional view of a transistor 330 that is a type of top-gate transistor. The transistor 330 includes the semiconductor layer 324 over the insulating layer 372, the electrodes 344a and 344b over the semiconductor layer 324 and the insulating layer 372 and in contact with part of the semiconductor layer 324, the insulating layer 326 over the semiconductor layer 324 and the electrodes 344a and 344b, and the electrode 322 over the insulating layer 326.

[0167]

Since the electrode 322 overlaps with neither the electrode 344a nor the electrode 344b in the transistor 330, the parasitic capacitance generated between the electrodes 322 and 344a and the parasitic capacitance generated between the electrodes 322 and 344b can be reduced. After the formation of the electrode 322, an impurity 255 is introduced into the semiconductor layer 324 using the electrode 322 as a mask, so that an impurity region can be formed in the semiconductor layer 324 in a self-aligned manner (see FIG. 9A3). According to one embodiment of the present invention, a transistor with favorable electrical characteristics can be provided.

[0168]

The introduction of the impurity 255 can be performed with an ion implantation apparatus, an ion doping apparatus, or a plasma treatment apparatus.

[0169]

As the impurity 255, for example, at least one kind of element of Group 13 elements and Group 15 elements can be used. In the case where an oxide semiconductor is used for the semiconductor layer 324, it is possible to use at least one kind of element of a rare gas, hydrogen, and nitrogen as the impurity 255.

[0170]

A transistor 331 illustrated in FIG. 9A2 is different from the transistor 330 in that the electrode 323 and the insulating layer 227 are included. The transistor 331 includes the electrode 323 formed over the insulating layer 372 and the insulating layer 227 formed over the electrode 323. The electrode 323 can function as a back gate electrode. Thus, the insulating layer 227 can function as a gate insulating layer. The insulating layer 227 can be formed using a material and a method similar to those of the insulating layer 326.

[0171]

Like the transistor 311, the transistor 331 has a high on-state current for its area. That is, the area of the transistor 331 can be small for a required on-state current. According to one embodiment of the present invention, the area of a transistor can be reduced. Therefore, according to one embodiment of the present invention, a semiconductor device having a high degree of integration can be provided.

[0172]

A transistor 340 illustrated in FIG. 9B1 is a type of top-gate transistor. The transistor 340 is different from the transistor 330 in that the semiconductor layer 324 is formed after the formation of the electrodes 344a and 344b. A transistor 341 illustrated in FIG. 9B2 is different from the transistor 340 in that the electrode 323 and the insulating layer 227 are included. In

the transistors 340 and 341, part of the semiconductor layer 324 is formed over the electrode 344a and another part of the semiconductor layer 324 is formed over the electrode 344b.

[0173]

Like the transistor 311, the transistor 341 has a high on-state current for its area. That is, the area of the transistor 341 can be small for a required on-state current. According to one embodiment of the present invention, the area of a transistor can be reduced. Therefore, according to one embodiment of the present invention, a semiconductor device having a high degree of integration can be provided.

[0174]

A transistor 342 illustrated in FIG. 10A1 is a type of top-gate transistor. The transistor 342 is different from the transistor 330 or 340 in that the electrodes 344a and 344b are formed after the formation of the insulating layer 329. The electrodes 344a and 344b are electrically connected to the semiconductor layer 324 through openings formed in the insulating layers 328 and 329.

[0175]

Part of the insulating layer 326 that does not overlap with the electrode 322 is removed, and the impurity 255 is introduced into the semiconductor layer 324 using the electrode 322 and the insulating layer 326 that is left as a mask, so that an impurity region can be formed in the semiconductor layer 324 in a self-aligned manner (see FIG. 10A3). The transistor 342 includes a region where the insulating layer 326 extends beyond an end portion of the electrode 322. The semiconductor layer 324 in a region into which the impurity 255 is introduced through the insulating layer 326 has a lower impurity concentration than the semiconductor layer 324 in a region into which the impurity 255 is introduced without through the insulating layer 326. Thus, a lightly doped drain (LDD) region is formed in a region of the semiconductor layer 324 that does not overlap with the electrode 322.

[0176]

A transistor 343 illustrated in FIG. 10A2 is different from the transistor 342 in that the electrode 323 is included. The transistor 343 includes the electrode 323 that is formed over the substrate 371 and overlaps with the semiconductor layer 324 with the insulating layer 372 provided therebetween. The electrode 323 can function as a back gate electrode.

[0177]

As in a transistor 344 illustrated in FIG. 10B1 and a transistor 345 illustrated in FIG. 10B2, the insulating layer 326 in a region that does not overlap with the electrode 322 may be completely removed. Alternatively, as in a transistor 346 illustrated in FIG. 10C1 and a transistor 347 illustrated in FIG. 10C2, the insulating layer 326 may be left.

[0178]

In the transistors 342 to 347, after the formation of the electrode 322, the impurity 255 is introduced into the semiconductor layer 324 using the electrode 322 as a mask, so that an impurity region can be formed in the semiconductor layer 324 in a self-aligned manner. According to one embodiment of the present invention, a transistor with favorable electrical characteristics can be provided. Furthermore, according to one embodiment of the present invention, a semiconductor device having a high degree of integration can be provided.

[0179]

[Substrate]

There is no great limitation on a material used for the substrate. The material is determined according to the purpose in consideration of whether it has a light-transmitting property, heat resistance high enough to withstand heat treatment, or the like. For example, a glass substrate of barium borosilicate glass, aluminosilicate glass, or the like, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used. Alternatively, a semiconductor substrate, a flexible substrate, an attachment film, a base film, or the like may be used.

[0180]

As the semiconductor substrate, a semiconductor substrate of silicon, germanium, or the like or a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, or gallium oxide, or the like is used, for example. As the semiconductor substrate, a single-crystal semiconductor or a polycrystalline semiconductor may be used.

[0181]

As the substrate, a large-sized glass substrate having any of the following sizes can be used: the 6th generation (1500 mm × 1850 mm), the 7th generation (1870 mm × 2200 mm), the 8th generation (2200 mm × 2400 mm), the 9th generation (2400 mm × 2800 mm), and the 10th generation (2950 mm × 3400 mm). Thus, a large-sized display device can be manufactured. With the increase in area of glass substrates, a larger number of display devices can be produced from one glass substrate, which can reduce production cost.

[0182]

To increase the flexibility of the display device 110, a flexible substrate, an attachment film, a base film, or the like may be used as the substrate.

[0183]

Examples of materials that can be used for the flexible substrate, the attachment film, the base film, and the like include polyester resins such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), a polyacrylonitrile resin, an acrylic resin, a polyimide resin, a

polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, polyamide resins (e.g., nylon and aramid), a polysiloxane resin, a cycloolefin resin, a polystyrene resin, a polyamide-imide resin, a polyurethane resin, a polyvinyl chloride resin, a polyvinylidene chloride resin, a polypropylene resin, a polytetrafluoroethylene (PTFE) resin, an ABS resin, and cellulose nanofiber.

[0184]

When any of the above-described materials is used for the substrate, a lightweight display device can be provided. Furthermore, when any of the above-described materials is used for the substrate, a shock-resistant display device can be provided. Moreover, when any of the above-described materials is used for the substrate, a display device that is less likely to be broken can be provided.

[0185]

The flexible substrate used as the substrate preferably has a lower coefficient of linear expansion because deformation due to an environment is suppressed. The flexible substrate used as the substrate is formed using, for example, a material whose coefficient of linear expansion is lower than or equal to 1×10^{-3}/K, lower than or equal to 5×10^{-5}/K, or lower than or equal to 1×10^{-5}/K. In particular, aramid is preferably used for the flexible substrate because of its low coefficient of linear expansion.

[0186]

[Conductive layer]

As conductive materials for the gate, the source, and the drain of the transistor, and the conductive layer such as a wiring or an electrode included in the display device, a metal element selected from aluminum (Al), chromium (Cr), copper (Cu), silver (Ag), gold (Au), platinum (Pt), tantalum (Ta), nickel (Ni), titanium (Ti), molybdenum (Mo), tungsten (W), hafnium (Hf), vanadium (V), niobium (Nb), manganese (Mn), magnesium (Mg), zirconium (Zr), beryllium (Be), and the like; an alloy containing any of the above metal elements as a component; an alloy containing a combination of the above metal elements; or the like can be used. Alternatively, a semiconductor typified by polycrystalline silicon including an impurity element such as phosphorus, or silicide such as nickel silicide may be used. There is no particular limitation on the formation method of the conductive material, and a variety of formation methods such as an evaporation method, a CVD method, a sputtering method, and a spin coating method can be employed.

[0187]

A Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) may be used as the conductive material. A layer made of a Cu-*X* alloy can be processed with a wet etching process,

resulting in lower manufacturing cost. Alternatively, an aluminum alloy containing one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used as the conductive material.

[0188]

The conductive layer can be formed using a conductive material containing oxygen, such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. Moreover, a conductive material containing nitrogen, such as titanium nitride, tantalum nitride, or tungsten nitride, can be used. In addition, a stacked-layer structure formed using a conductive material containing oxygen, a conductive material containing nitrogen, and a material containing any of the above metal elements can be used for the conductive layer.

[0189]

For example, the conductive layer may have a single layer structure of an aluminum layer containing silicon, a two-layer structure in which a titanium layer is stacked over an aluminum layer, a two-layer structure in which a titanium layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a tantalum nitride layer, or a three-layer structure in which a titanium layer, an aluminum layer, and a titanium layer are stacked in this order.

[0190]

A stack of a plurality of conductive layers formed with the above conductive materials may be used. For example, a stacked-layer structure formed using a material containing the above metal element and a conductive material containing oxygen may be used for the conductive layer. Alternatively, a stacked-layer structure formed using a material containing the above metal element and a conductive material containing nitrogen may be used. Further alternatively, a stacked-layer structure formed using a material containing the above metal element, a conductive material containing oxygen, and a conductive material containing nitrogen may be used.

[0191]

For example, a three-layer structure of a conductive layer including oxygen and at least one of indium and zinc, a conductive layer including copper, and a conductive layer including oxygen and at least one of indium and zinc, can be used for the conductive layer. In that case, the side surface of the conductive layer including copper is preferably covered with the conductive layer including oxygen and at least one of indium and zinc. Alternatively, a stack of

a plurality of conductive layers including oxygen and at least one of indium and zinc may be used.

[0192]

[Insulating layer]

The insulating layers can be formed with a single layer or a stack of layers of one or more materials selected from aluminum nitride, aluminum oxide, aluminum nitride oxide, aluminum oxynitride, magnesium oxide, silicon nitride, silicon oxide, silicon nitride oxide, silicon oxynitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, aluminum silicate, and the like. Alternatively, a material in which two or more materials selected from an oxide material, a nitride material, an oxynitride material, and a nitride oxide material are mixed may be used.

[0193]

Note that in this specification, a nitride oxide refers to a compound that includes more nitrogen than oxygen. An oxynitride refers to a compound that includes more oxygen than nitrogen. The content of each element can be measured by Rutherford backscattering spectrometry (RBS), for example.

[0194]

It is particularly preferable that the insulating layers 372 and 329 be formed using an insulating material that is relatively impermeable to impurities. For example, a single layer or a stack of layers of an insulating material containing boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum is used. Examples of an insulating material that is relatively impermeable to impurities include aluminum oxide, aluminum nitride, aluminum oxynitride, aluminum nitride oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, and silicon nitride.

[0195]

When the insulating material that is relatively impermeable to impurities is used for the insulating layer 372, impurity diffusion from the substrate 371 side can be suppressed, and the reliability of the transistor can be improved. When the insulating material that is relatively impermeable to impurities is used for the insulating layer 329, impurity diffusion from layers above the insulating layer 329 can be suppressed, and the reliability of the transistor can be improved.

[0196]

As the insulating layer, an insulating layer that can function as a planarization layer may be used. The insulating layer that can function as a planarization layer can be formed using an organic material having heat resistance, such as a polyimide, an acrylic resin, a benzocyclobutene resin, a polyamide, or an epoxy resin. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that a plurality of insulating layers formed of these materials may be stacked.

[0197]

Note that the siloxane resin corresponds to a resin including a Si-O-Si bond formed using a siloxane-containing material as a starting material. The siloxane resin may include as a substituent an organic group (e.g., an alkyl group or an aryl group) or a fluoro group. In addition, the organic group may include a fluoro group.

[0198]

A surface of the insulating layer or the like may be subjected to CMP treatment. By the CMP treatment, unevenness of the surface can be reduced, and coverage with an insulating layer or a conductive layer formed later can be increased.

[0199]

[Semiconductor layer]

As a semiconductor material used for the semiconductor layer of the transistor, an amorphous semiconductor or a semiconductor having crystallinity (a microcrystalline semiconductor, a polycrystalline semiconductor, a single crystal semiconductor, or a semiconductor partly including crystal regions) may be used.

[0200]

For example, silicon or germanium can be used as a semiconductor material used for the semiconductor layer of the transistor. Furthermore, a compound semiconductor such as a silicon carbide, a gallium arsenide, a metal oxide, or a nitride semiconductor, an organic semiconductor, or the like can be used.

[0201]

For example, amorphous silicon can be used as a semiconductor material used for the transistor. In particular, amorphous silicon is easily mass-produced and provided over a large-sized substrate. Note that in general, amorphous silicon used for a transistor contains a large amount of hydrogen; hence, amorphous silicon containing a large amount of hydrogen is referred to as hydrogenated amorphous silicon or a-Si:H in some cases. Moreover, amorphous silicon can be formed at temperatures lower than temperatures at which polycrystalline silicon is formed, and thus, the highest temperature in the manufacturing process can be lowered.

Accordingly, low heat-resistance materials can be used for a substrate, a conductive layer, an insulating layer, and the like.

[0202]

Furthermore, silicon with crystallinity such as microcrystalline silicon, polycrystalline silicon, or a single crystal silicon can be used as a semiconductor material used for the transistor. In particular, polycrystalline silicon can be formed at a lower temperature than a temperature at which single crystal silicon is formed and has higher field-effect mobility and higher reliability than those of amorphous silicon.

[0203]

Furthermore, an oxide semiconductor, which is a kind of a metal oxide, can be used as a semiconductor material used for the transistor. As a typical example, an oxide semiconductor containing indium can be given. An oxide semiconductor enables higher field-effect mobility and higher reliability than those of amorphous silicon. Moreover, an oxide semiconductor is easily mass-produced and provided over a large-sized substrate.

[0204]

An oxide semiconductor, which is a kind of a metal oxide, has a wider bandgap and lower carrier density than those of silicon; thus, an oxide semiconductor is preferably used for the semiconductor layer of the transistor. The use of an oxide semiconductor for the semiconductor layer of the transistor is preferable in terms of reducing current flowing between a source and a drain of the transistor in an off state.

[0205]

An oxide semiconductor, which is a kind of a metal oxide, preferably has an energy gap of 2 eV or more, further preferably 2.5 eV or more, still further preferably 3 eV or more. The use of such an oxide semiconductor having a wide energy gap leads to a reduction in off-state current of the transistor.

[0206]

An oxide semiconductor, which is a kind of a metal oxide, preferably includes, for example, a material represented by an In-M-Zn-based oxide that contains at least indium, zinc, and M (a metal such as aluminum, titanium, gallium, germanium, yttrium, zirconium, lanthanum, cerium, tin, neodymium, or hafnium). In order to reduce variations in electrical characteristics of the transistor including the oxide semiconductor, the oxide semiconductor preferably contains a stabilizer in addition to indium, zinc, and M.

[0207]

Examples of the stabilizer, including metals that can be used as M, are gallium, tin, hafnium, aluminum, and zirconium. As another stabilizer, lanthanoid such as lanthanum,

cerium, praseodymium, neodymium, samarium, europium, gadolinium, terbium, dysprosium, holmium, erbium, thulium, ytterbium, or lutetium can be given.

[0208]

As a metal oxide included in the semiconductor layer, any of the following can be used, for example: an In-Ga-Zn-based oxide, an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, an In-Hf-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, an In-Lu-Zn-based oxide, an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, and an In-Hf-Al-Zn-based oxide.

[0209]

Note that here, for example, an "In-Ga-Zn-based oxide" means an oxide containing In, Ga, and Zn as its main components and there is no limitation on the ratio of In:Ga:Zn. Further, a metal element in addition to In, Ga, and Zn may be contained.

[0210]

Note that a metal oxide that can be used for the semiconductor layer of the transistor is described in detail in other embodiments.

[0211]

[Methods for forming layers]

Note that insulating layers, semiconductor layers, conductive layers for forming electrodes and wirings, and the like included in the display device can be formed by any of a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, and the like. As the CVD method, a plasma-enhanced chemical vapor deposition (PECVD) method or a thermal CVD method may be used. As the thermal CVD method, for example, a metal organic chemical vapor deposition (MOCVD) method may be used.

[0212]

The insulating layers, the semiconductor layers, the conductive layers for forming the electrodes and the wirings, and the like included in the display device may be formed by a method such as spin coating, dipping, spray coating, ink-jetting, dispensing, screen printing, or offset printing, or with a slit coater, a roll coater, a curtain coater, or a knife coater.

[0213]

In the case of a PECVD method, a high quality film can be obtained at relatively low temperature. By using a deposition method that does not use plasma for deposition, such as the MOCVD method, the ALD method, or the thermal CVD method, damage is not easily caused on a surface on which the film is deposited. For example, a wiring, an electrode, an element (e.g., transistor or capacitor), or the like included in a semiconductor device might be charged up by receiving charges from plasma. In that case, accumulated charges might break the wiring, electrode, element, or the like included in the semiconductor device. Such plasma damage is not caused in the case of using a deposition method without using plasma, and thus the yield of a semiconductor device can be increased. In addition, since plasma damage does not occur in the deposition, a film with few defects can be obtained.

[0214]

Unlike in a deposition method in which particles ejected from a target or the like are deposited, in a CVD method and an ALD method, a film is formed by reaction at a surface of an object. Thus, a CVD method and an ALD method enable favorable step coverage almost regardless of the shape of an object. In particular, an ALD method enables excellent step coverage and excellent thickness uniformity and can be favorably used for covering a surface of an opening with a high aspect ratio, for example. On the other hand, an ALD method has a relatively low deposition rate; thus, it is sometimes preferable to combine an ALD method with another deposition method with a high deposition rate such as a CVD method.

[0215]

When a CVD method or an ALD method is used, composition of a film to be formed can be controlled with a flow rate ratio of the source gases. For example, by a CVD method or an ALD method, a film with a certain composition can be formed depending on a flow rate ratio of the source gases. Moreover, with a CVD method or an ALD method, by changing the flow rate ratio of the source gases while forming the film, a film whose composition is continuously changed can be formed. In the case where the film is formed while changing the flow rate ratio of the source gases, as compared to the case where the film is formed using a plurality of deposition chambers, time taken for the film formation can be reduced because time taken for transfer and pressure adjustment is omitted. Thus, semiconductor devices can be manufactured with improved productivity.

[0216]

The layers (thin films) included in the display device can be processed by a photolithography method or the like. Alternatively, island-shaped layers may be formed by a film formation method using a blocking mask. Alternatively, the layers may be processed by a nanoimprinting method, a sandblasting method, a lift-off method, or the like. Examples of the

photolithography method include a method in which a resist mask is formed over a layer (thin film) to be processed, part of the layer (thin film) is selectively removed by using the resist mask as a mask, and the resist mask is removed, and a method in which a photosensitive layer is formed and exposed to light and developed to be processed into a desired shape.

[0217]

In the case of using light in the photolithography method, any of an *i*-line (light with a wavelength of 365 nm), a *g*-line (light with a wavelength of 436 nm), and an *h*-line (light with a wavelength of 405 nm), or combined light of any of them can be used for exposure. Alternatively, ultraviolet light, KrF laser light, ArF laser light, or the like can be used. Exposure may be performed by liquid immersion exposure technique. As the light for the exposure, extreme ultra-violet light (EUV) or X-rays may be used. Instead of the light for the exposure, an electron beam can be used. It is preferable to use EUV, X-rays, or an electron beam because extremely minute processing can be performed. Note that in the case of performing exposure by scanning of a beam such as an electron beam, a photomask is not needed.

[0218]

For the removal (etching) of the layers (thin films), a dry etching method, a wet etching method, a sandblast method, or the like can be used. Alternatively, these etching methods may be employed in combination.

[0219]

This embodiment can be implemented in an appropriate combination with any of the structures described in the other embodiments and the like.

[0220]

(Embodiment 4)

In this embodiment, a metal oxide that can be used for the semiconductor layer of the transistor is described.

[0221]

<Composition of metal oxide>

Described in this section is the composition of a cloud-aligned composite oxide semiconductor (CAC-OS) or a cloud-aligned composite (CAC) metal oxide, which is one embodiment of a metal oxide that can be used for the semiconductor device, e.g., the transistor, disclosed in one embodiment of the present invention.

[0222]

Note that in this specification and the like, CAC or c-axis-aligned crystal (CAAC) might be stated. In this case, CAC refers to an example of a function or a material composition, and CAAC refers to an example of a structure.

[0223]

A CAC-OS or a CAC metal oxide has a conducting function in a part of the material and has an insulating function in another part of the material; as a whole, the CAC-OS or the CAC metal oxide has a function of a semiconductor. In the case where the CAC-OS or the CAC metal oxide is used in an active layer of a transistor, the conducting function is to allow electrons (or holes) serving as carriers to flow, and the insulating function is to not allow electrons serving as carriers to flow. By the complementary action of the conducting function and the insulating function, the CAC-OS or the CAC metal oxide can have a switching function (on/off function). In the CAC-OS or CAC metal oxide, separation of the functions can maximize each function.

[0224]

Thus, the CAC-OS or the CAC metal oxide includes conductive regions and insulating regions. The conductive regions have the above-described conducting function, and the insulating regions have the above-described insulating function. In some cases, the conductive regions and the insulating regions in the material are separated at the nanoparticle level. In some cases, the conductive regions and the insulating regions are unevenly distributed in the material. The conductive regions are observed to be connected in a cloud-like manner with their boundaries blurred, in some cases.

[0225]

Note that in the CAC-OS or the CAC metal oxide, the conductive regions and the insulating regions each have a size of more than or equal to 0.5 nm and less than or equal to 10 nm, preferably more than or equal to 0.5 nm and less than or equal to 3 nm and are dispersed in the material, in some cases.

[0226]

The CAC-OS or the CAC metal oxide includes components having different bandgaps. For example, the CAC-OS or the CAC metal oxide includes a component having a wide gap due to the insulating region and a component having a narrow gap due to the conductive region. In the case of such a composition, carriers mainly flow in the component having a narrow gap. The component having a narrow gap complements the component having a wide gap, and carriers also flow in the component having a wide gap in conjunction with the component having a narrow gap. Therefore, in the case where the above-described CAC-OS or the CAC metal oxide is used in a channel formation region of a transistor, high current drive capability in the on

state of the transistor, that is, high on-state current and high field-effect mobility, can be obtained.

[0227]

In other words, a CAC-OS or a CAC metal oxide can be called a matrix composite or a metal matrix composite.

[0228]

<Structure of metal oxide>

Described in this section is a structure of a metal oxide that can be used for the semiconductor device, e.g., the transistor, disclosed in one embodiment of the present invention.

[0229]

Metal oxides are classified into a metal oxide made of a single crystal material and a metal oxide made of a non-single-crystal material. A single crystal material has a single crystal structure. A non-single-crystal material has one or more of an amorphous structure, a microcrystalline structure, and a polycrystalline structure.

[0230]

As a non-single-crystal material, a semi-crystalline material is given. A semi-crystalline material has a structure intermediate between a single crystal structure and an amorphous structure.

[0231]

In the structure of a single crystal of a metal oxide, oxygen polyhedrons each having a metal atom at the center are connected to each other with particular regularity. Specifically, an $InGaZnO_4$ single crystal has a layered crystalline structure in which oxygen octahedrons each having an In atom at the center and oxygen trigonal bipyramids each having a Ga atom or a Zn atom at the center are connected to each other with particular regularity.

[0232]

In the structure of a semi-crystalline material, a plurality of oxygen polyhedrons each having a metal atom at the center is included and the polyhedrons are connected to each other without particular regularity. A polyhedron included in a semi-crystalline material is significantly broken compared with a polyhedron included in a single crystal structure and is not observed in a single crystal. Note that in some cases, part of a semi-crystalline material includes a polyhedron included in a single crystal structure, a region in which polyhedrons included in a single crystal structure are connected to each other with regularity, or the like.

[0233]

A structure of a semi-crystalline material in which polyhedrons are connected to each other without particular regularity is more stable than a structure of what is called an amorphous material.

[0234]

In the case where metal oxides are oxide semiconductors, for example, metal oxides are classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of the non-single-crystal oxide semiconductor include a c-axis-aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

[0235]

As an example of a semi-crystalline oxide semiconductor, an oxide semiconductor having a CAAC structure and a CAC composition (hereinafter also referred to as CAAC/CAC) is given.

[0236]

A CAAC-OS is an oxide semiconductor having a CAAC structure having c-axis alignment, its nanocrystals are connected to each other in the a-b plane direction, and the crystal structure has distortion. Note that the distortion is a portion where the direction of a lattice arrangement changes between a region with a regular lattice arrangement and another region with a regular lattice arrangement in a region in which nanocrystals are connected.

[0237]

The shape of the nanocrystal is basically hexagon. However, the shape is not always a regular hexagon and is a non-regular hexagon in some cases. A pentagonal lattice arrangement, a heptagonal lattice arrangement, and the like are included in the distortion in some cases. Note that a clear crystal grain boundary cannot be observed even in the vicinity of distortion in the CAAC-OS. That is, formation of a grain boundary is inhibited due to the distortion of lattice arrangement. This is probably because the CAAC-OS can tolerate distortion owing to a low density of arrangement of oxygen atoms in the a-b plane direction, an interatomic bond distance changed by substitution of a metal element, and the like.

[0238]

The CAAC-OS tends to have a layered crystal structure (also referred to as a stacked-layer structure) in which a layer containing indium and oxygen (hereinafter, In layer) and a layer containing the element M, zinc, and oxygen (hereinafter, (*M*,Zn) layer) are stacked. Note that indium and the element M can be replaced with each other, and when the elements M of the (M,Zn) layer are partly replaced with indium, the layer can also be referred to as an

(In,M,Zn) layer. Also, when indium in the In layer is partly replaced with the element M, the layer can be referred to as an (In,M) layer.

[0239]

The CAAC-OS is an oxide semiconductor with high crystallinity. In the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur because a clear grain boundary cannot be observed. Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancies). Thus, a CAAC-OS is physically stable. Therefore, a CAAC-OS is resistant to heat and has high reliability.

[0240]

An nc-OS is an oxide semiconductor having a structure in which a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different nanocrystals in the nc-OS. Thus, the orientation of the whole film is not observed. Accordingly, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor, depending on an analysis method.

[0241]

An a-like OS is an oxide semiconductor having a structure intermediate between those of the nc-OS and the amorphous oxide semiconductor. The a-like OS contains a void or a low-density region. That is, the a-like OS has low crystallinity as compared with the nc-OS and the CAAC-OS.

[0242]

An oxide semiconductor can have various structures which show various different properties. Two or more of the amorphous oxide semiconductor, the polycrystalline oxide semiconductor, the a-like OS, the nc-OS, and the CAAC-OS may be included in an oxide semiconductor of one embodiment of the present invention.

[0243]

This embodiment can be implemented in an appropriate combination with any of the structures described in the other embodiments and the like.

[0244]

(Embodiment 5)

In this embodiment, an example of a transistor which can be used for the display device and the like described in the above embodiments is described with reference to drawings.

Specifically, structure examples of a transistor that can be preferably used as an OS transistor will be described.

[0245]

<Structure examples of transistor>

[STRUCTURE EXAMPLE 1]

To show a structure example of the transistor, a transistor 500a is described with reference to FIGS. 11A to 11C. FIG. 11A is a top view of the transistor 500a. FIG. 11B is a cross-sectional view taken along dashed-dotted line X1-X2 in FIG. 11A, and FIG. 11C is a cross-sectional view taken along dashed-dotted line Y1-Y2 in FIG. 11A. Note that in FIG. 11A, some components of the transistor 500a (e.g., an insulating layer having a function as a gate insulating layer) are not illustrated for easy understanding. Note that hereinafter, the direction of the dashed-dotted line X1-X2 may be called the channel length direction, and the direction of the dashed-dotted line Y1-Y2 may be called the channel width direction. As in FIG. 11A, some components might not be illustrated in some top views of transistors described below.

[0246]

The transistor 500a includes a conductive layer 521 over an insulating layer 524, an insulating layer 511 over the insulating layer 524 and over the conductive layer 521, a semiconductor layer 531 over the insulating layer 511, a conductive layer 522a over the semiconductor layer 531 and over the insulating layer 511, a conductive layer 522b over the semiconductor layer 531 and over the insulating layer 511, an insulating layer 512 over the semiconductor layer 531 and over the conductive layers 522a and 522b, and a conductive layer 523 over the insulating layer 512.

[0247]

Note that the insulating layer 524 may be a substrate. When the insulating layer 524 is a substrate, the substrate can include a material similar to that of the substrate 371 described in Embodiment 3.

[0248]

The conductive layer 521 and the conductive layer 523 can include a material similar to that of the electrode 322 described in Embodiment 3, for example. The insulating layer 511 can include a material similar to that of the insulating layer 326 described in Embodiment 3, for example. The conductive layers 522a and 522b can include a material similar to that of the electrodes 344a and 344b described in Embodiment 3, for example. The insulating layer 512 can include a material similar to that of the insulating layer 328 described in Embodiment 3.

[0249]

The semiconductor layer 531 can include a material similar to that of the semiconductor layer 324 described in Embodiment 3, for example. In this embodiment, the case where the semiconductor layer 531 is a semiconductor layer including a metal oxide is described.

[0250]

The insulating layer 511 and the insulating layer 512 have an opening portion 535. The conductive layer 523 is electrically connected to the conductive layer 521 through the opening portion 535.

[0251]

The insulating layer 511 has a function as a first gate insulating layer of the transistor 500a, and the insulating layer 512 has a function as a second gate insulating layer of the transistor 500a. In the transistor 500a, the conductive layer 521 has a function as a first gate. The conductive layer 522a has a function as one of a source and a drain and the conductive layer 522b has a function as the other of the source and the drain. In the transistor 500a, the conductive layer 523 has a function as a second gate.

[0252]

Note that the transistor 500a is a channel-etched transistor, and has a dual-gate structure.

[0253]

In the transistor 500a, the conductive layer 523 may be omitted. In that case, the transistor 500a is a channel-etched transistor, and has a bottom-gate structure.

[0254]

As illustrated in FIGS. 11B and 11C, the semiconductor layer 531 faces the conductive layer 521 and the conductive layer 523, and is between two conductive layers having functions as the gates. The length of the conductive layer 523 in the channel length direction is longer than the length of the semiconductor layer 531 in the channel length direction. The length of the conductive layer 523 in the channel width direction is longer than the length of the semiconductor layer 531 in the channel width direction. The whole semiconductor layer 531 is covered with the conductive layer 523 with the insulating layer 512 positioned therebetween.

[0255]

In other words, the conductive layers 521 and 523 are connected to each other in the opening portion 535 provided in the insulating layers 511 and 512, and have a region located outside a side end portion of the semiconductor layer 531.

[0256]

With this structure, the semiconductor layer 531 included in the transistor 500a can be electrically surrounded by electric fields of the conductive layers 521 and 523. A device structure of a transistor in which electric fields of a first gate and a second gate electrically

surround a semiconductor layer where a channel formation region is formed, like in the transistor 500a, can be referred to as a surrounded channel (S-channel) structure.

[0257]

Since the transistor 500a has the S-channel structure, an electric field for inducing a channel can be effectively applied to the semiconductor layer 531 by the conductive layer 521 having a function as the first gate; therefore, the current drive capability of the transistor 500a can be improved and high on-state current characteristics can be obtained. Since the on-state current can be increased, it is possible to reduce the size of the transistor 500a.

[0258]

In addition, since the transistor 500a has a structure in which the semiconductor layer 531 is surrounded by the conductive layer 521 having a function as a first gate and the conductive layer 523 having a function as a second gate, the mechanical strength of the transistor 500a can be increased.

[0259]

Since the transistor 500a having the S-channel structure has high field-effect mobility and high driving capability, the use of the transistor 500a in a driver circuit, a typical example of which is a gate driver, allows the display device to have a narrow bezel.

[0260]

[STRUCTURE EXAMPLE 2]

Next, to show a structure example of a transistor, a transistor 500b is described with reference to FIGS. 12A to 12C. FIG. 12A is a top view of the transistor 500b. FIG. 12B is a cross-sectional view taken along dashed-dotted line X1-X2 in FIG. 12A, and FIG. 12C is a cross-sectional view taken along dashed-dotted line Y1-Y2 in FIG. 12A.

[0261]

The transistor 500b is different from the transistor 500a in that the semiconductor layer 531, the conductive layer 522a, the conductive layer 522b, and the insulating layer 512 each have a multi-layer structure.

[0262]

The insulating layer 512 includes an insulating layer 512a over the semiconductor layer 531 and over the conductive layers 522a and 522b and an insulating layer 512b over the insulating layer 512a. The insulating layer 512 has a function of supplying oxygen to the semiconductor layer 531. That is, the insulating layer 512 contains oxygen. The insulating layer 512a is an insulating layer that allows oxygen to pass therethrough. Note that the insulating layer 512a also functions as a film that relieves damage to the semiconductor layer 531 at the time of forming the insulating layer 512b in a later step.

[0263]

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 5 nm and less than or equal to 150 nm, preferably greater than or equal to 5 nm and less than or equal to 50 nm can be used as the insulating layer 512a.

[0264]

In addition, it is preferable that the number of defects in the insulating layer 512a be small and typically, the spin density corresponding to a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than or equal to 3×10^{17} spins/cm^3 by electron spin resonance (ESR) measurement. This is because if the density of defects in the insulating layer 512a is high, oxygen is bonded to the defects and the property of transmitting oxygen of the insulating layer 512a is lowered.

[0265]

Note that all oxygen entering the insulating layer 512a from the outside does not move to the outside of the insulating layer 512a and some oxygen remains in the insulating layer 512a. Furthermore, movement of oxygen occurs in the insulating layer 512a in some cases in such a manner that oxygen enters the insulating layer 512a and oxygen included in the insulating layer 512a moves to the outside of the insulating layer 512a. When an oxide insulating layer that can transmit oxygen is formed as the insulating layer 512a, oxygen released from the insulating layer 512b provided over the insulating layer 512a can be moved to the semiconductor layer 531 through the insulating layer 512a.

[0266]

Note that the insulating layer 512a can be formed using an oxide insulating layer having a low density of states due to nitrogen oxide. Note that the density of states due to nitrogen oxide can be formed between the energy of the valence band maximum and the energy of the conduction band minimum of the metal oxide layer. A silicon oxynitride film that releases less nitrogen oxide, an aluminum oxynitride film that releases less nitrogen oxide, or the like can be used as the above oxide insulating layer.

[0267]

Note that a silicon oxynitride film that releases less nitrogen oxide is a film which releases ammonia more than nitrogen oxide in thermal desorption spectroscopy (TDS) analysis; the amount of released ammonia is typically greater than or equal to 1×10^{18} /cm^3 and less than or equal to 5×10^{19} /cm^3. Note that the amount of released ammonia is the amount of ammonia released by heat treatment with which the surface temperature of a film becomes higher than or

equal to 50 °C and lower than or equal to 650 °C, preferably higher than or equal to 50 °C and lower than or equal to 550 °C.

[0268]

Nitrogen oxide (NO_x; x is greater than 0 and less than or equal to 2, preferably greater than or equal to 1 and less than or equal to 2), typically NO_2 or NO, forms levels in the insulating layer 512a, for example. The level is positioned in the energy gap of the semiconductor layer 531. Therefore, when nitrogen oxide is diffused to the interface between the insulating layer 512a and the semiconductor layer 531, an electron is in some cases trapped by the level on the insulating layer 512a side. As a result, the trapped electron remains in the vicinity of the interface between the insulating layer 512a and the semiconductor layer 531; thus, the threshold voltage of the transistor is shifted in the positive direction.

[0269]

Nitrogen oxide reacts with ammonia and oxygen in heat treatment. Since nitrogen oxide included in the insulating layer 512a reacts with ammonia included in the insulating layer 512b in heat treatment, nitrogen oxide included in the insulating layer 512a is reduced. Therefore, an electron is hardly trapped at the interface between the insulating layer 512a and the semiconductor layer 531.

[0270]

By using such an oxide insulating layer for the insulating layer 512a, the shift in the threshold voltage of the transistor can be reduced, which leads to a smaller change in the electrical characteristics of the transistor.

[0271]

The concentration of nitrogen of the above oxide insulating layer measured by SIMS is lower than or equal to 6×10^{20} atoms/cm^3.

[0272]

The above oxide insulating layer is formed by a PECVD method at a substrate temperature higher than or equal to 220 °C and lower than or equal to 350 °C using silane and dinitrogen monoxide, whereby a dense and hard film can be formed.

[0273]

The insulating layer 512b is an oxide insulating layer which contains oxygen at a higher proportion than the stoichiometric composition. Part of oxygen is released from the above oxide insulating layer by heating. The amount of oxygen released from the oxide insulating layer in TDS is greater than or equal to 1.0×10^{19} atoms/cm^3, preferably greater than or equal to 3.0×10^{20} atoms/cm^3. Note that the amount of released oxygen is the total amount of oxygen

released by heat treatment in a temperature range of 50 °C to 650 °C or 50 °C to 550 °C in TDS. In addition, the amount of released oxygen is the total amount of released oxygen converted into oxygen atoms in TDS. In this specification and the like, oxygen released from the insulating layer and the like by heating is also referred to as excess oxygen.

[0274]

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 30 nm and less than or equal to 500 nm, preferably greater than or equal to 50 nm and less than or equal to 400 nm can be used as the insulating layer 512b.

[0275]

It is preferable that the number of defects in the insulating layer 512b be small and typically, the spin density corresponding to a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than 1.5×10^{18} spins/cm^3, preferably lower than or equal to 1×10^{18} spins/cm^3 by ESR measurement. Note that the insulating layer 512b is provided more apart from the semiconductor layer 531 than the insulating layer 512a is; thus, the insulating layer 512b may have higher density of defects than the insulating layer 512a.

[0276]

Furthermore, the insulating layer 512 can be formed using insulating layers formed of the same kinds of materials; thus, a boundary between the insulating layers 512a and 512b cannot be clearly observed in some cases. Thus, in this embodiment, the boundary between the insulating layers 512a and 512b is shown by a dashed line. Although a two-layer structure of the insulating layers 512a and 512b is described in this embodiment, the present invention is not limited to this. For example, a single-layer structure of only the insulating layer 512a or a layered structure of three or more layers may be employed.

[0277]

The semiconductor layer 531 in the transistor 500b includes a semiconductor layer 531_1 over the insulating layer 511 and a semiconductor layer 531_2 over the semiconductor layer 531_1. The semiconductor layers 531_1 and 531_2 contain the same kind of element. For example, it is preferable that the semiconductor layers 531_1 and 531_2 each independently contain the same element as the element in the semiconductor layer 531 described above.

[0278]

Each of the semiconductor layers 531_1 and 531_2 preferably contains a region where the atomic proportion of In is higher than the atomic proportion of *M*. For example, the atomic ratio of In to *M* and Zn in each of the semiconductor layers 531_1 and 531_2 is preferably In:*M*:Zn = 4:2:3 or in the neighborhood thereof. As for the range expressed by the term

"neighborhood" here, when In is 4, *M* ranges from 1.5 to 2.5 and Zn ranges from 2 to 4. Alternatively, the atomic ratio of In to *M* and Zn in each of the semiconductor layers 531_1 and 531_2 is preferably In:*M*:Zn = 5:1:6 or in the neighborhood thereof. The semiconductor layers 531_1 and 531_2 having substantially the same composition as described above can be formed using the same sputtering target; thus, the manufacturing cost can be reduced. When the same sputtering target is used, the semiconductor layers 531_1 and 531_2 can be formed successively in the same vacuum chamber. This can suppress entry of impurities into the interface between the semiconductor layers 531_1 and 531_2.

[0279]

Here, the semiconductor layer 531_1 may include a region whose crystallinity is lower than that of the semiconductor layer 531_2. Note that the crystallinity of the semiconductor layers 531_1 and 531_2 can be determined by analysis by X-ray diffraction (XRD) or with a transmission electron microscope (TEM), for example.

[0280]

The region with low crystallinity in the semiconductor layer 531_1 serves as a diffusion path of oxygen, through which oxygen can be diffused into the semiconductor layer 531_2 having higher crystallinity than the semiconductor layer 531_1. When a multi-layer structure including the semiconductor layers having different crystal structures is employed and the region with low crystallinity is used as a diffusion path of oxygen as described above, the transistor can be highly reliable.

[0281]

The semiconductor layer 531_2 having a region with higher crystallinity than the semiconductor layer 531_1 can prevent impurities from entering the semiconductor layer 531. In particular, the increased crystallinity of the semiconductor layer 531_2 can reduce damage at the time of processing into the conductive layers 522a and 522b. The surface of the semiconductor layer 531, i.e., the surface of the semiconductor layer 531_2 is exposed to an etchant or an etching gas at the time of processing into the conductive layers 522a and 522b. However, when the semiconductor layer 531_2 has a region with high crystallinity, the semiconductor layer 531_2 has higher etching resistance than the semiconductor layer 531_1. Thus, the semiconductor layer 531_2 has a function as an etching stopper.

[0282]

By including a region having lower crystallinity than the semiconductor layer 531_2, the semiconductor layer 531_1 sometimes has a high carrier density.

[0283]

When the semiconductor layer 531_1 has a high carrier density, the Fermi level is sometimes high relative to the conduction band of the semiconductor layer 531_1. This lowers the conduction band minimum of the semiconductor layer 531_1, so that the energy difference between the conduction band minimum of the semiconductor layer 531_1 and the trap level, which might be formed in a gate insulating layer (here, the insulating layer 511), is increased in some cases. The increase of the energy difference can reduce trap of charges in the gate insulating layer and reduce variation in the threshold voltage of the transistor, in some cases. In addition, when the semiconductor layer 531_1 has a high carrier density, the semiconductor layer 531 can have high field-effect mobility.

[0284]

Although the semiconductor layer 531 in the transistor 500b has a multi-layer structure including two layers in this example, the structure is not limited thereto, and the semiconductor layer 531 may have a multi-layer structure including three or more layers.

[0285]

The conductive layer 522a in the transistor 500b includes a conductive layer 522a_1, a conductive layer 522a_2 over the conductive layer 522a_1, and a conductive layer 522a_3 over the conductive layer 522a_2. The conductive layer 522b in the transistor 500b includes a conductive layer 522b_1, a conductive layer 522b_2 over the conductive layer 522b_1, and a conductive layer 522b_3 over the conductive layer 522b_2.

[0286]

For example, it is preferable that the conductive layers 522a_1, 522b_1, 522a_3, and 522b_3 contain one or more elements selected from titanium, tungsten, tantalum, molybdenum, indium, gallium, tin, and zinc. Furthermore, it is preferable that the conductive layers 522a_2 and 522b_2 contain one or more elements selected from copper, aluminum, and silver.

[0287]

Specifically, the conductive layers 522a_1, 522b_1, 522a_3, and 522b_3 can contain an In-Sn oxide or an In-Zn oxide and the conductive layers 522a_2 and 522b_2 can contain copper.

[0288]

An end portion of the conductive layer 522a_1 has a region located outside an end portion of the conductive layer 522a_2. The conductive layer 522a_3 covers a top surface and a side surface of the conductive layer 522a_2 and has a region that is in contact with the conductive layer 522a_1. An end portion of the conductive layer 522b_1 has a region located

outside an end portion of the conductive layer 522b_2. The conductive layer 522b_3 covers a top surface and a side surface of the conductive layer 522b_2 and has a region that is in contact with the conductive layer 522b_1.

[0289]

The above structure is preferred because the structure can reduce the wiring resistance of the conductive layers 522a and 522b and inhibit diffusion of copper to the semiconductor layer 531.

[0290]

[STRUCTURE EXAMPLE 3]

To show a structure example of a transistor, a transistor 500c is described with reference to FIGS. 13A to 13C. FIG. 13A is a top view of the transistor 500c. FIG. 13B is a cross-sectional view taken along dashed-dotted line X1-X2 in FIG. 13A, and FIG. 13C is a cross-sectional view taken along dashed-dotted line Y1-Y2 in FIG. 13A.

[0291]

The transistor 500c includes the conductive layer 521 over the insulating layer 524, the insulating layer 511 over the conductive layer 521 and over the insulating layer 524, the semiconductor layer 531 over the insulating layer 511, an insulating layer 516 over the semiconductor layer 531 and over the insulating layer 511, the conductive layer 522a over the semiconductor layer 531 and over the insulating layer 516, the conductive layer 522b over the semiconductor layer 531 and over the insulating layer 516, the insulating layer 512 over the insulating layer 516 and over the conductive layers 522a and 522b, and the conductive layer 523 over the insulating layer 512.

[0292]

The insulating layers 511, 516, and 512 have the opening portion 535. The conductive layer 521 having a function as the first gate of the transistor 500c is electrically connected to the conductive layer 523 having a function as the second gate of the transistor 500c through the opening portion 535. The insulating layer 516 has an opening portion 538a and an opening portion 538b. The conductive layer 522a having a function as one of a source and a drain of the transistor 500c is electrically connected to the semiconductor layer 531 through the opening portion 538a. The conductive layer 522b having a function as the other of the source and the drain of the transistor 500c is electrically connected to the semiconductor layer 531 through the opening portion 538b.

[0293]

The insulating layer 516 has a function as a channel protective layer of the transistor 500c. Without the insulating layer 516, a channel formation region of the semiconductor layer

531 might be damaged by an etching method or the like at the time of the formation of the conductive layers 522a and 522b. This might make the electrical characteristics of the transistor unstable. The damage to the channel formation region of the semiconductor layer 531 can be prevented when the insulating layer 516 is formed, the opening portions 538a and 538b are provided, and a conductive layer is then formed and processed to form the conductive layers 522a and 522b by an etching method or the like. Accordingly, the electrical characteristics of the transistor can be stabilized to achieve high reliability of the transistor.

[0294]

The insulating layer 516 can include a material similar to that of the insulating layer 512, for example.

[0295]

The insulating layer 516 preferably contains excess oxygen. When the insulating layer 516 contains excess oxygen region, oxygen can be supplied to the channel formation region in the semiconductor layer 531. As a result, oxygen vacancies formed in the channel formation region can be filled with oxygen, which can provide a highly reliable display device.

[0296]

After the opening portions 538a and 538b are formed, an impurity element is preferably added to the semiconductor layer 531. Specifically, an element that forms an oxygen vacancy or an element that is bonded to an oxygen vacancy is preferably added. This can increase the conductivity of a region of the semiconductor layer 531 which overlaps with the conductive layer 522a (one of a source region and a drain region) and a region of the semiconductor layer 531 which overlaps with the conductive layer 522b (the other of the source region and the drain region), as described in detail later. Accordingly, the current drive capability of the transistor 500c is improved, so that a high on-state current can be obtained.

[0297]

Note that the transistor 500c is a channel-protective transistor, and has a dual-gate structure.

[0298]

As with the transistors 500a and 500b, the transistor 500c has the S-channel structure. With this structure, the semiconductor layer 531 included in the transistor 500c can be electrically surrounded by electric fields of the conductive layers 521 and 523.

[0299]

Since the transistor 500c has the S-channel structure, an electric field for inducing a channel can be effectively applied to the semiconductor layer 531 by the conductive layer 521 or 523. Thus, the current drive capability of the transistor 500c can be improved and high on-state

current characteristics can be obtained. As a result of the high on-state current, it is possible to reduce the size of the transistor 500c. Furthermore, since the transistor 500c has a structure in which the semiconductor layer 531 is surrounded by the conductive layers 521 and 523, the mechanical strength of the transistor 500c can be increased.

[0300]

In the transistor 500c, the conductive layer 523 may be omitted. In that case, the transistor 500c is a channel-protective transistor, and has a bottom-gate structure.

[0301]

[STRUCTURE EXAMPLE 4]

Next, to show structure examples of a transistor, a transistor 500d and a transistor 500e are described with reference to FIGS. 14A to 14D.

[0302]

FIGS. 14A and 14B are cross-sectional views of the transistor 500d and FIGS. 14C and 14D are cross-sectional views of the transistor 500e. The transistor 500d is a modification example of the transistor 500b described above and the transistor 500e is a modification example of the transistor 500c described above. In FIGS. 14A to 14D, therefore, common reference numerals are used for the components having functions similar to those in the transistor 500b and the transistor 500c, and a detailed description of the components is omitted.

[0303]

FIG. 14A is a cross-sectional view of the transistor 500d in the channel length direction, and FIG. 14B is a cross-sectional view of the transistor 500d in the channel width direction. FIG. 14C is a cross-sectional view of the transistor 500e in the channel length direction, and FIG. 14D is a cross-sectional view of the transistor 500e in the channel width direction.

[0304]

The transistor 500d illustrated in FIGS. 14A and 14B is different from the transistor 500b in that the conductive layer 523 and the opening portion 535 are not provided. The transistor 500d is different from the transistor 500b in the structures of the insulating layer 512, the conductive layer 522a, and the conductive layer 522b.

[0305]

The insulating layer 512 of the transistor 500d includes an insulating layer 512c and an insulating layer 512d over the insulating layer 512c. The insulating layer 512c has a function of supplying oxygen to the semiconductor layer 531 and function of preventing impurities (typically, water, hydrogen, and the like) from entering the semiconductor layer 531. As the insulating layer 512c, an aluminum oxide film, an aluminum oxynitride film, or an aluminum nitride oxide film can be used. In particular, the insulating layer 512c is preferably an

aluminum oxide film formed by a reactive sputtering method. As an example of a method of forming an aluminum oxide by a reactive sputtering method, the following method can be given.

[0306]

First, a mixed gas of an inert gas (typically, an Ar gas) and an oxygen gas is introduced into a sputtering chamber. Subsequently, a voltage is applied to an aluminum target provided in the sputtering chamber, whereby the aluminum oxide film can be deposited. Electric power used for applying a voltage to the aluminum target is supplied from a DC power source, an AC power source, or an RF power source. The DC power source is particularly preferably used to improve the productivity.

[0307]

The insulating layer 512d has a function of preventing the entry of impurities (typically, water, hydrogen, and the like). As the insulating layer 512d, a silicon nitride film, a silicon nitride oxide film, or a silicon oxynitride film can be used. In particular, a silicon nitride film formed by a PECVD method is preferably used as the insulating layer 512d. The silicon nitride film formed by a PECVD method is preferable because the film is likely to have a high film density. Note that the hydrogen concentration in the silicon nitride film formed by a PECVD method is high in some cases.

[0308]

Since the insulating layer 512c is provided below the insulating layer 512d in the transistor 500d, hydrogen in the insulating layer 512d does not or is less likely to diffuse into the semiconductor layer 531 side.

[0309]

The transistor 500d is a single-gate transistor, unlike the transistor 500b. The use of a single-gate transistor can reduce the number of masks, leading to increased productivity.

[0310]

The transistor 500e illustrated in FIGS. 14C and 14D is different from the transistor 500c in the structures of the insulating layer 516 and the insulating layer 512. Specifically, the transistor 500e includes an insulating layer 516a instead of the insulating layer 516 and the insulating layer 512d instead of the insulating layer 512.

[0311]

The insulating layer 516a has a function similar to that of the insulating layer 512c.

[0312]

The structure of the transistor 500d or 500e can be formed using the existing production line without high capital investment. For example, a manufacturing plant for an oxide

semiconductor can be simply substituted for a manufacturing plant for hydrogenated amorphous silicon.

[0313]

[STRUCTURE EXAMPLE 5]

To show a structure example of a transistor, a transistor 500f is described with reference to FIGS. 15A to 15C. FIG. 15A is a top view of the transistor 500f. FIG. 15B is a cross-sectional view taken along dashed-dotted line X1-X2 in FIG. 15A, and FIG. 15C is a cross-sectional view taken along dashed-dotted line Y1-Y2 in FIG. 15A.

[0314]

The transistor 500f illustrated in FIGS. 15A to 15C includes the conductive layer 521 over the insulating layer 524, the insulating layer 511 over the conductive layer 521 and over the insulating layer 524, the semiconductor layer 531 over the insulating layer 511, the insulating layer 512 over the semiconductor layer 531, the conductive layer 523 over the insulating layer 512, and an insulating layer 515 over the insulating layer 511, over the semiconductor layer 531, and over the conductive layer 523. The semiconductor layer 531 includes a channel formation region 531i overlapping with the conductive layer 523, a source region 531s in contact with the insulating layer 515, and a drain region 531d in contact with the insulating layer 515.

[0315]

The insulating layer 515 contains nitrogen or hydrogen. The insulating layer 515 is in contact with the source region 531s and the drain region 531d, so that nitrogen or hydrogen that is contained in the insulating layer 515 is added to the source region 531s and the drain region 531d. The source region 531s and the drain region 531d each have a high carrier density when nitrogen or hydrogen is added thereto.

[0316]

The transistor 500f may include the conductive layer 522a electrically connected to the source region 531s through an opening portion 536a provided in the insulating layer 515. The transistor 500f may further include the conductive layer 522b electrically connected to the drain region 531d through an opening portion 536b provided in the insulating layer 515.

[0317]

The insulating layer 511 has a function as a first gate insulating layer, and the insulating layer 512 has a function as a second gate insulating layer. The insulating layer 515 serves as a protective insulating layer.

[0318]

The insulating layer 512 preferably contains excess oxygen. When the insulating layer 512 contains excess oxygen, oxygen can be supplied to the channel formation region 531i

included in the semiconductor layer 531. As a result, oxygen vacancies that might be formed in the channel formation region 531i can be filled with oxygen, which can provide a highly reliable display device.

[0319]

To supply oxygen to the semiconductor layer 531, the insulating layer 511 that is formed below the semiconductor layer 531 may contain excess oxygen. However, in that case, oxygen contained in the insulating layer 511 might also be supplied to the source region 531s and the drain region 531d included in the semiconductor layer 531. When oxygen is supplied to the source region 531s and the drain region 531d, the resistance of the source region 531s and the drain region 531d might be increased.

[0320]

By contrast, in the structure in which the insulating layer 512 formed over the semiconductor layer 531 contains excess oxygen, oxygen can be selectively supplied only to the channel formation region 531i. Alternatively, the carrier density of the source and drain regions 531s and 531d can be selectively increased after oxygen is supplied to the channel formation region 531i and the source and drain regions 531s and 531d, in which case an increase in the resistance of the source and drain regions 531s and 531d can be prevented.

[0321]

Furthermore, each of the source region 531s and the drain region 531d included in the semiconductor layer 531 preferably contains an element that forms an oxygen vacancy or an element that is bonded to an oxygen vacancy. Typical examples of the element that forms an oxygen vacancy or the element that is bonded to an oxygen vacancy include hydrogen, boron, carbon, nitrogen, fluorine, phosphorus, sulfur, chlorine, titanium, and a rare gas. Typical examples of the rare gas element include helium, neon, argon, krypton, and xenon. In the case where one or more of the elements that form oxygen vacancies are contained in the insulating layer 515, the one or more of the elements are diffused from the insulating layer 515 to the source region 531s and the drain region 531d, and/or may be added to the source region 531s and the drain region 531d by impurity addition treatment.

[0322]

An impurity element added to the metal oxide cuts a bond between a metal element and oxygen in the metal oxide, so that an oxygen vacancy is formed. Alternatively, when the impurity element is added to the metal oxide, oxygen bonded to a metal element in the metal oxide is bonded to the impurity element, and the oxygen is released from the metal element, whereby an oxygen vacancy is formed. As a result, the metal oxide has a higher carrier density and thus the conductivity thereof becomes higher.

[0323]

The conductive layer 521 functions as a first gate and the conductive layer 523 functions as a second gate. The conductive layer 522a has a function as a source and the conductive layer 522b has a function as a drain.

[0324]

As illustrated in FIG. 15C, an opening portion 537 is formed in the insulating layers 511 and 512. The conductive layer 521 is electrically connected to the conductive layer 523 through the opening portion 537. Thus, the conductive layers 521 and 523 are supplied with the same potential. Note that different potentials may be applied to the conductive layers 521 and 523 without providing the opening portion 537. Alternatively, the conductive layer 521 may be used as a light-blocking film without providing the opening portion 537. For example, light irradiating the channel formation region 531i from the bottom can be reduced by the conductive layer 521 formed with a light-blocking material.

[0325]

As illustrated in FIGS. 15B and 15C, while facing the conductive layer 521 having a function as the first gate and the conductive layer 523 having a function as the second gate, the semiconductor layer 531 is positioned between the two conductive layers having functions as the gates.

[0326]

As with the transistors 500a, 500b, and 500c, the transistor 500f has the S-channel structure. Such a structure enables the semiconductor layer 531 included in the transistor 500f to be electrically surrounded by electric fields of the conductive layer 521 having a function as the first gate and the conductive layer 523 having a function as the second gate.

[0327]

Since the transistor 500f has the S-channel structure, an electric field for inducing a channel can be effectively applied to the semiconductor layer 531 by the conductive layer 521 or 523. Thus, the current drive capability of the transistor 500f can be improved and high on-state current characteristics can be obtained. As a result of the high on-state current, it is possible to reduce the size of the transistor 500f. Furthermore, since the transistor 500f has a structure in which the semiconductor layer 531 is surrounded by the conductive layers 521 and 523, the mechanical strength of the transistor 500f can be increased.

[0328]

The transistor 500f may be called a top-gate self-aligned (TGSA) FET from the position of the conductive layer 523 relative to the semiconductor layer 531 or the formation method of the conductive layer 523.

[0329]

The semiconductor layer 531 in the transistor 500f may have a multi-layer structure including two or more layers, as in the transistor 500b.

[0330]

Although the insulating layer 512 is provided only in a portion overlapping with the conductive layer 523 in the transistor 500f, the structure is not limited thereto, and the insulating layer 512 may cover the semiconductor layer 531. Alternatively, the conductive layer 521 may be omitted.

[0331]

At least part of this embodiment can be implemented in combination with any of the other embodiments described in this specification as appropriate.

[0332]

(Embodiment 6)

In this embodiment, a structure examples of a display device including a liquid crystal element and a structure example of a display device including an EL element are described. In FIG. 16A, a sealant 4005 is provided so as to surround the display portion 113 provided over a first substrate 4001, and the display portion 113 is sealed by the sealant 4005 and a second substrate 4006.

[0333]

In FIG. 16A, a data driver 111a, a data driver 111b, a gate driver 112a, and a gate driver 112b each include a plurality of integrated circuits 4042 provided over a printed circuit board 4041. The integrated circuits 4042 are each formed using a single crystal semiconductor or a polycrystalline semiconductor. The data drivers 111a and 111b function in a manner similar to that of the data driver 111 (signal line driver circuit) described in the above embodiments. The gate drivers 112a and 112b function in a manner similar to that of the gate driver 112 (scan line driver circuit) described in the above embodiments.

[0334]

The display device 110 is electrically connected to the display controller 100 and/or the processor 120 described in the above embodiments through an FPC 4018 (FPC: flexible printed circuit). A variety of signals and potentials are supplied to the gate drivers 112a and 112b and the data drivers 111a and 111b through the FPC 4018.

[0335]

The integrated circuits 4042 included in the gate drivers 112a and 112b each have a function of supplying a selection signal to the display portion 113. The integrated circuits 4042 included in the data drivers 111a and 111b each have a function of supplying a video signal to the

display portion 113. The integrated circuits 4042 are mounted by a tape automated bonding (TAB) method in a region different from a region surrounded by the sealant 4005 over the first substrate 4001.

[0336]

Note that the connection method of the integrated circuit 4042 is not particularly limited; a wire bonding method, a chip on glass (COG) method, a tape carrier package (TCP) method, a chip on film (COF) method, or the like can be used.

[0337]

FIG. 16B illustrates an example of mounting the integrated circuits 4042 included in the data drivers 111a and 111b by a COG method. With the use of any of the transistors described in the above embodiments, some or all of driver circuits can be formed over a substrate over which the display portion 113 is formed, whereby a system-on-panel can be obtained.

[0338]

In the example illustrated in FIG. 16B, the gate drivers 112a and 112b are formed over the substrate over which the display portion 113 is formed. When the driver circuits are formed concurrently with the pixel circuit in the display portion 113, the number of components can be reduced. Accordingly, the productivity can be increased.

[0339]

In FIG. 16B, the sealant 4005 is provided to surround the display portion 113, the gate driver 112a, and the gate driver 112b over the first substrate 4001. The second substrate 4006 is provided over the display portion 113, the gate driver 112a, and the gate driver 112b. Consequently, the display portion 113, the gate driver 112a, and the gate driver 112b are sealed together with a display element by the first substrate 4001, the sealant 4005, and the second substrate 4006.

[0340]

Although the data drivers 111a and 111b are formed separately and mounted on the first substrate 4001 in the example illustrated in FIG. 16B, one embodiment of the present invention is not limited to this structure. The gate driver may be separately formed and then mounted, or part of the data driver or part of the gate driver may be separately formed and then mounted.

[0341]

In some cases, the display device encompasses a panel in which a display element is sealed, and a module in which an IC or the like including a controller is mounted on the panel.

[0342]

The display portion and the gate driver over the first substrate each include a plurality of transistors. Any of the transistors described in the above embodiments can be applied to the transistors.

[0343]

A transistor included in a peripheral driver circuit and a transistor included in the pixel circuit of the display portion may have the same structure or different structures. Transistors included in the peripheral driver circuit may have the same structure or a combination of two or more kinds of structures. Similarly, transistors included in the pixel circuit may have the same structure or a combination of two or more kinds of structures.

[0344]

FIGS. 17A and 17B correspond to cross-sectional views taken along the chain line N1-N2 in FIG. 16B. Display devices illustrated in FIGS. 17A and 17B each have an electrode 4015, and the electrode 4015 is electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive layer 4019. In FIGS. 17A and 17B, the electrode 4015 is electrically connected to a wiring 4014 in an opening formed in insulating layers 4112, 4111, and 4110.

[0345]

The electrode 4015 is formed of the same conductive layer as a first electrode layer 4030, and the wiring 4014 is formed of the same conductive layer as a source and drain electrodes of transistors 4010 and 4011.

[0346]

The display portion 113 and the gate driver 112a provided over the first substrate 4001 include a plurality of transistors. In FIGS. 17A and 17B, the transistor 4010 included in the display portion 113 and the transistor 4011 included in the gate driver 112a are illustrated as an example. In the examples illustrated in FIGS. 17A and 17B, the transistors 4010 and 4011 are bottom-gate transistors.

[0347]

In FIGS. 17A and 17B, the insulating layer 4112 is provided over the transistors 4010 and 4011. A bank 4510 is provided over the insulating layer 4112 in FIG. 17B.

[0348]

The transistors 4010 and 4011 are provided over an insulating layer 4102. The transistors 4010 and 4011 each include an electrode 4017 formed over the insulating layer 4111. The electrode 4017 can serve as a back gate electrode.

[0349]

Any of the transistors described in the above embodiments can be used as the transistors 4010 and 4011.

[0350]

The display devices illustrated in FIGS. 17A and 17B each include a capacitor 4020. The capacitor 4020 includes an electrode 4021 formed in the same step as that for forming a gate electrode of the transistor 4010, and an electrode formed in the same step as that for forming a source electrode and a drain electrode of the transistor 4010. The electrodes overlap with each other with the insulating layer 4103 provided therebetween.

[0351]

In general, the capacitance of a capacitor provided in a pixel portion of a display device is set in consideration of leakage current or the like of transistors provided in a pixel portion so that charges can be held for a predetermined period. The capacitance of the capacitor may be set in consideration of off-state current of the transistor or the like.

[0352]

The transistor 4010 included in the display portion 113 is electrically connected to the display element. An example of a liquid crystal display device using a liquid crystal element as a display element is illustrated in FIG. 17A. In FIG. 17A, a liquid crystal element 4013 which is a display element includes the first electrode layer 4030, a second electrode layer 4031, and a liquid crystal layer 4008. Insulating films 4032 and 4033 serving as alignment films are provided so that the liquid crystal layer 4008 is sandwiched therebetween. The second electrode layer 4031 is provided on the second substrate 4006 side, and the first electrode layer 4030 and the second electrode layer 4031 overlap with each other with the liquid crystal layer 4008 positioned therebetween.

[0353]

A spacer 4035 is a columnar spacer obtained by selective etching of an insulating layer and is provided in order to control a distance between the first electrode layer 4030 and the second electrode layer 4031 (a cell gap). Alternatively, a spherical spacer may be used.

[0354]

A black matrix (a light-blocking layer); a coloring layer (a color filter); an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member; and the like may be provided as appropriate as needed. For example, circular polarization may be employed by using a polarizing substrate and a retardation substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0355]

In the display device illustrated in FIG. 17A, a light-blocking layer 4132, a coloring layer 4131, and an insulating layer 4133 are provided between the substrate 4006 and the second electrode layer 4031.

[0356]

Examples of a material that can be used for the light-blocking layer include carbon black, titanium black, a metal, a metal oxide, and a composite oxide containing a solid solution of a plurality of metal oxides. The light-blocking layer may be a film containing a resin material or a thin film of an inorganic material such as a metal. Stacked films containing the material of the coloring layer can also be used for the light-blocking layer. For example, a stacked-layer structure of a film containing a material of a coloring layer which transmits light of a certain color and a film containing a material of a coloring layer which transmits light of another color can be employed. It is preferable that the coloring layer and the light-blocking layer be formed using the same material because the same manufacturing apparatus can be used and the process can be simplified.

[0357]

As examples of a material that can be used for the coloring layer, a metal material, a resin material, and a resin material containing a pigment or dye can be given. The light-blocking layer and the coloring layer may be formed by a method similar to the above-described methods for forming the layers. For example, an inkjet method may be used.

[0358]

The display devices illustrated in FIGS. 17A and 17B include the insulating layers 4111 and 4104. As the insulating layers 4111 and 4104, insulating layers through which an impurity element does not easily pass are used. A semiconductor layer of the transistor is sandwiched between the insulating layers 4111 and 4104, whereby entry of impurities from the outside can be prevented.

[0359]

As the display element included in the display device, a light-emitting element utilizing electroluminescence (also referred to as an "EL element") can be used. An EL element includes a layer containing a light-emitting compound (also referred to as an "EL layer") between a pair of electrodes. By generating a potential difference between the pair of electrodes that is greater than the threshold voltage of the EL element, holes are injected to the EL layer from the anode side and electrons are injected to the EL layer from the cathode side. The injected electrons and holes are recombined in the EL layer and a light-emitting substance contained in the EL layer emits light.

[0360]

EL elements are classified depending on whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element.

[0361]

In an organic EL element, by voltage application, electrons are injected from one electrode to the EL layer and holes are injected from the other electrode to the EL layer. The carriers (electrons and holes) are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, this light-emitting element is referred to as a current-excitation light-emitting element.

[0362]

In addition to the light-emitting compound, the EL layer may further include any of a substance with a high hole-injection property, a substance with a high hole-transport property, a hole-blocking material, a substance with a high electron-transport property, a substance with a high electron-injection property, a substance with a bipolar property (a substance with a high electron- and hole-transport property), and the like.

[0363]

The EL layer can be formed by an evaporation method (including a vacuum evaporation method), a transfer method, a printing method, an inkjet method, a coating method, or the like.

[0364]

The inorganic EL elements are classified according to their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. A dispersion-type inorganic EL element includes a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission that utilizes a donor level and an acceptor level. A thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localization type light emission that utilizes inner-shell electron transition of metal ions. Here, the case will be described in which an organic EL element is used as a light-emitting element.

[0365]

In order to extract light emitted from the light-emitting element, at least one of a pair of electrodes needs to be transparent. The transistor and the light-emitting element are formed over a substrate. The light-emitting element can have a top emission structure in which light emission is extracted from the side opposite to the substrate; a bottom emission structure in

which light emission is extracted from the substrate side; or a dual emission structure in which light emission is extracted from both the side opposite to the substrate and the substrate side.

[0366]

FIG. 17B illustrates an example of a light-emitting display device (also referred to as an "EL display device") using a light-emitting element as a display element. The light-emitting element 4513 which is a display element is electrically connected to the transistor 4010 provided in the display portion 113. The structure of the light-emitting element 4513 is the stacked-layer structure including the first electrode layer 4030, a light-emitting layer 4511, and the second electrode layer 4031; however, this embodiment is not limited to this structure. The structure of the light-emitting element 4513 can be changed as appropriate depending on a direction in which light is extracted from the light-emitting element 4513, or the like.

[0367]

The bank 4510 is formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the bank 4510 be formed using a photosensitive resin material to have an opening over the first electrode layer 4030 so that a side surface of the opening slopes with continuous curvature.

[0368]

The light-emitting layer 4511 may be formed using a single layer or a plurality of layers stacked.

[0369]

The emission color of the light-emitting element 4513 can be changed to white, red, green, blue, cyan, magenta, yellow, or the like depending on the material that forms the light-emitting layer 4511.

[0370]

As a color display method, there are a method in which the light-emitting element 4513 whose emission color is white is combined with a coloring layer and a method in which the light-emitting element 4513 with a different emission color is provided in each pixel. The former method is more productive than the latter method. On the other hand, the latter method, which requires separate formation of the light-emitting layer 4511 pixel by pixel, is less productive than the former method. However, the latter method can produce the emission color with higher color purity than that of the emission color produced by the former method. When the light-emitting element 4513 has a microcavity structure in the latter method, the color purity can be further increased.

[0371]

The light-emitting layer 4511 may contain an inorganic compound such as quantum dots. For example, when used for the light-emitting layer, the quantum dot can serve as a light-emitting material.

[0372]

A protective layer may be formed over the second electrode layer 4031 and the bank 4510 in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element 4513. For the protective layer, a silicon nitride, a silicon nitride oxide, an aluminum oxide, an aluminum nitride, an aluminum oxynitride, an aluminum nitride oxide, diamond like carbon (DLC), or the like can be used. In a space which is formed with the first substrate 4001, the second substrate 4006, and the sealant 4005, a filler 4514 is provided for sealing. It is preferable that the panel be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover member with high air-tightness and little degasification so that the panel is not exposed to the outside air, in this manner.

[0373]

As the filler 4514, an ultraviolet curable resin or a thermosetting resin can be used as well as an inert gas such as nitrogen or argon; for example, polyvinyl chloride (PVC), an acrylic resin, polyimide, an epoxy resin, a silicone resin, polyvinyl butyral (PVB), ethylene vinyl acetate (EVA), or the like can be used. A drying agent may be contained in the filler 4514.

[0374]

For example, a glass material such as a glass frit, or a resin that is curable at room temperature such as a two-component-mixture-type resin, a light curable resin, a thermosetting resin, and the like can be used for the sealant 4005. A drying agent may be contained in the sealant 4005.

[0375]

If necessary, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate for a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment by which reflected light can be diffused by projections and depressions on a surface to reduce the glare can be performed.

[0376]

When the light-emitting element has a microcavity structure, light with high color purity can be extracted. Furthermore, when a microcavity structure and a color filter are used in combination, the glare can be reduced and visibility of a display image can be increased.

[0377]

The first electrode layer and the second electrode layer (each of which is also referred to as a pixel electrode layer, a common electrode layer, a counter electrode layer, or the like) for applying voltage to the display element may have light-transmitting properties or light-reflecting properties, which depends on the direction in which light is extracted, the position where the electrode layer is provided, and the pattern structure of the electrode layer.

[0378]

The first electrode layer 4030 and the second electrode layer 4031 can be formed using a light-transmitting conductive material such as an indium oxide containing a tungsten oxide, an indium zinc oxide containing a tungsten oxide, an indium oxide containing a titanium oxide, an indium tin oxide, an indium tin oxide containing a titanium oxide, an indium zinc oxide, or an indium tin oxide to which a silicon oxide is added.

[0379]

The first electrode layer 4030 and the second electrode layer 4031 each can also be formed using one or more kinds selected from a metal such as tungsten (W), molybdenum (Mo), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), cobalt (Co), nickel (Ni), titanium (Ti), platinum (Pt), aluminum (Al), copper (Cu), or silver (Ag); an alloy thereof; and a nitride thereof.

[0380]

A conductive composition containing a conductive high molecule (also referred to as conductive polymer) can be used for the first electrode layer 4030 and the second electrode layer 4031. As the conductive high molecule, what is called a π electron conjugated conductive high molecule can be used. For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, a copolymer of two or more of aniline, pyrrole, and thiophene or a derivative thereof can be given.

[0381]

Since the transistor is easily broken owing to static electricity or the like, a protective circuit for protecting the driver circuit is preferably provided. The protective circuit is preferably formed using a nonlinear element.

[0382]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and the like.

[0383]

(Embodiment 7)

In this embodiment, electronic devices to which the display system of one embodiment of the present invention can be applied are described with reference to FIGS. 18A to 18F and FIGS. 19A to 19F.

[0384]

FIGS. 18A to 18F and FIGS. 19A to 19F illustrate examples of an electronic device. According to one embodiment of the present invention, a display device having an increased size and/or definition can have favorable display quality and high visibility. Thus, the display device can be suitably used for a television device, digital signage, a mobile electronic device, a wearable electronic device (a wearable device), an electronic book terminal, and the like. In addition, the display device can be suitably used for virtual reality (VR) devices, augmented reality (AR) devices, and the like.

[0385]

The electronic device using the display system of one embodiment of the present invention may include a secondary battery. It is preferable that the secondary battery be capable of being charged by non-contact power transmission.

[0386]

Examples of the secondary battery include a lithium ion secondary battery such as a lithium polymer battery using a gel electrolyte (lithium ion polymer battery), a nickel-hydride battery, a nickel-cadmium battery, an organic radical battery, a lead-acid battery, an air secondary battery, a nickel-zinc battery, and a silver-zinc battery.

[0387]

The electronic device using the display system of one embodiment of the present invention may include an antenna. When a signal is received by the antenna, the electronic device can display an image, data, or the like on a display portion. When the electronic device includes the antenna and a secondary battery, the antenna may be used for contactless power transmission.

[0388]

The electronic device using the display system of one embodiment of the present invention may include a sensor (a sensor having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, electric current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, odor, or infrared rays).

[0389]

The electronic device using the display system of one embodiment of the present invention can have a variety of functions such as a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of executing a variety of software (programs), a wireless communication function, and a function of reading out a program or data stored in a recording medium.

[0390]

With the use of the display system of one embodiment of the present invention, the display quality and the like of an electronic device can be improved.

[0391]

Furthermore, the electronic device including a plurality of display portions can have a function of displaying image information mainly on one display portion while displaying text information mainly on another display portion, a function of displaying a three-dimensional image by displaying images where parallax is considered on a plurality of display portions, or the like. Furthermore, the electronic device including an image receiving portion can have a function of photographing a still image or a moving image, a function of automatically or manually correcting a photographed image, a function of storing a photographed image in a recording medium (an external recording medium or a recording medium incorporated in the electronic device), a function of displaying a photographed image on a display portion, or the like. Note that the functions of the electronic devices of embodiments of the present invention are not limited thereto, and the electronic devices can have a variety of functions.

[0392]

FIG. 18A illustrates a television device 1810 using the display system of one embodiment of the present invention. The television device 1810 includes a display portion 1811, a housing 1812, a speaker 1813, and the like. Also, the television device can include an LED lamp, operation keys (including a power switch or an operation switch), a connection terminal, a variety of sensors, a microphone, and the like.

[0393]

The television device 1810 can be controlled with a remote controller 1814.

[0394]

The television device 1810 can receive airwaves such as a ground wave and a wave transmitted from a satellite. The television device 1810 can receive airwaves for analog broadcasting, digital broadcasting, and the like, and image-sound-only broadcasting, sound-only broadcasting, and the like. For example, the television device 1810 can receive airwaves transmitted in a certain frequency band, such as a UHF band (about 300 MHz to 3 GHz) or a

VHF band (30 MHz to 300 MHz). When a plurality of pieces of data received in a plurality of frequency bands is used, the transfer rate can be increased and thus more information can be obtained. Accordingly, the display portion 1831 can display an image with a resolution higher than the full high definition, such as 4K, 8K, 16K, or more.

[0395]

An image to be displayed on the display portion 1831 may be generated using broadcasting data transmitted with technology for transmitting data through a computer network such as the Internet, a local area network (LAN), or Wi-Fi (registered trademark). In that case, the television device 1810 does not necessarily include a tuner.

[0396]

FIG. 18B illustrates a digital signage 1820 using the display system of one embodiment of the present invention. The digital signage 1820 is mounted on a cylindrical pillar 1822 and includes a display portion 1821.

[0397]

The larger the display portion 1821 is, the more information the display portion 1821 can provide at a time. In addition, the larger the display portion 1821 is, the more the display portion 1821 attracts attention, so that the effectiveness of the advertisement can be increased, for example.

[0398]

It is preferable to use a touch panel in the display portion 1821 because a device with such a structure does not just display a still or moving image, but can be operated by users intuitively. Alternatively, in the case where the display system of one embodiment of the present invention is used for providing information such as route information or traffic information, usability can be enhanced by intuitive operation.

[0399]

FIG. 18C illustrates a notebook personal computer 1830 using the display system of one embodiment of the present invention. The personal computer 1830 includes a display portion 1831, a housing 1832, a touch pad 1833, a connection port 1834, and the like.

[0400]

The touch pad 1833 functions as an input unit such as a pointing device or a pen tablet and can be controlled with a finger, a stylus, or the like.

[0401]

Furthermore, a display element is incorporated in the touch pad 1833. As illustrated in FIG. 18C, when an input key 1835 is displayed on a surface of the touch pad 1833, the touch pad 1833 can be used as a keyboard. In that case, a vibration module may be incorporated in the

touch pad 1833 so that sense of touch is achieved by vibration when a user touches the input key 1835.

[0402]

FIG. 18D illustrates an example of a portable information terminal using the display system of one embodiment of the present invention. A portable information terminal 1840 illustrated in FIG. 18D includes a housing 1841, a display portion 1842, an operation button 1843, an external connection port 1844, a speaker 1845, a microphone 1846, a camera 1847, and the like.

[0403]

The portable information terminal 1840 includes a touch sensor in the display portion 1842. Moreover, operations such as making a call and inputting a letter can be performed by touch on the display portion 1842 with a finger, a stylus, or the like.

[0404]

The power can be turned on or off with the operation button 1843. In addition, types of images displayed on the display portion 1842 can be switched; for example, switching images from a mail creation screen to a main menu screen is performed with the operation button 1843.

[0405]

When a detection device such as a gyroscope sensor or an acceleration sensor is provided inside the portable information terminal 1840, the direction of display on the screen of the display portion 1842 can be automatically changed by determining the orientation of the portable information terminal 1840 (whether the portable information terminal 1840 is placed horizontally or vertically). Furthermore, the direction of display on the screen can be changed by touch on the display portion 1842, operation with the operation button 1843, sound input using the microphone 1846, or the like.

[0406]

The portable information terminal 1840 has one or more of a telephone function, a notebook function, an information browsing function, and the like, for example. Specifically, the portable information terminal can be used as a smartphone. The portable information terminal 1840 is capable of executing a variety of applications such as mobile phone calls, e-mailing, viewing and editing texts, music reproduction, reproducing a moving image, Internet communication, and computer games, for example.

[0407]

FIGS. 18E and 18F illustrate an example of a portable information terminal 1850 using the display system of one embodiment of the present invention. The portable information

terminal 1850 includes a housing 1851, a housing 1852, a display portion 1853, a display portion 1854, a hinge portion 1855, and the like.

[0408]

The housing 1851 and the housing 1852 are joined together with the hinge portion 1855. The portable information terminal 1850 folded as in FIG. 18E can be changed into the state illustrated in FIG. 18F, in which the housing 1851 and the housing 1852 are opened.

[0409]

For example, text information can be displayed on the display portion 1853 and the display portion 1854; thus, the portable information terminal 1850 can be used as an e-book reader. Furthermore, still images and moving images can be displayed on the display portions 1853 and 1854.

[0410]

In this manner, the portable information terminal 1850 has high versatility because it can be folded when carried.

[0411]

Note that the housing 1851 and the housing 1852 may have a power button, an operation button, an external connection port, a speaker, a microphone, and the like.

[0412]

FIG. 19A is an external view of a camera 1860 using the display system of one embodiment of the present invention to which a finder 1861 is attached.

[0413]

The camera 1860 includes a housing 1869, a display portion 1862, an operation button 1863, a shutter button 1864, and the like. Furthermore, a detachable lens 1865 is attached to the camera 1860.

[0414]

Although the lens 1865 of the camera 1860 here is detachable from the housing 1869 for replacement, the lens 1865 may be integrated with the housing.

[0415]

Images can be taken with the camera 1860 at the press of the shutter button 1864. In addition, images can be taken at the touch of the display portion 1862 which serves as a touch panel.

[0416]

The housing 1869 of the camera 1860 includes a mount including an electrode, so that the finder 1861, a stroboscope, or the like can be connected to the housing 1869.

[0417]

The finder 1861 includes a housing 1866, a display portion 1867, a button 1868, and the like. The display system of one embodiment of the present invention may be used for the finder 1861.

[0418]

The housing 1866 includes a mount for engagement with the mount of the camera 1860 so that the finder 1861 can be connected to the camera 1860. The mount includes an electrode, and an image or the like received from the camera 1860 through the electrode can be displayed on the display portion 1867.

[0419]

The button 1868 serves as a power button. The display portion 1867 can be turned on and off using the button 1868.

[0420]

The display device of one embodiment of the present invention can be used for the display portion 1862 of the camera 1860 and the display portion 1867 of the finder 1861.

[0421]

Although the camera 1860 and the finder 1861 are separate and detachable electronic devices in FIG. 19A, the housing 1869 of the camera 1860 may include a finder having the display device of one embodiment of the present invention.

[0422]

FIG. 19B is an external view of a head-mounted display 1870 using the display system of one embodiment of the present invention.

[0423]

The head-mounted display 1870 includes a mounting portion 1871, a lens 1872, a main body 1873, a display portion 1874, a cable 1875, and the like. The mounting portion 1871 includes a battery 1876.

[0424]

Power is supplied from the battery 1876 to the main body 1873 through the cable 1875. The main body 1873 includes a wireless receiver or the like to receive video data, such as image data, and display it on the display portion 1874. The movement of the eyeball and the eyelid of a user is captured by a camera in the main body 1873 and then coordinates of a user's sight line are calculated using the captured data to utilize the user's sight line as an input means.

[0425]

The mounting portion 1871 may include a plurality of electrodes to be in contact with the user. The main body 1873 may be configured to sense current flowing through the electrodes with the movement of the user's eyeball to recognize the user's sight line. The main

body 1873 may be configured to sense current flowing through the electrodes to monitor the user's pulse. The mounting portion 1871 may include sensors, such as a temperature sensor, a pressure sensor, or an acceleration sensor so that the user's biological information can be displayed on the display portion 1874. The main body 1873 may be configured to sense the movement of the user's head or the like to move an image displayed on the display portion 1874 in synchronization with the movement of the user's head or the like.

[0426]

FIGS. 19C and 19D are external views of a head-mounted display 1880 using the display system of one embodiment of the present invention.

[0427]

The head-mounted display 1880 includes a housing 1881, two display portions 1882, an operation button 1883, and an object for fixing, such as a band, 1884.

[0428]

The head-mounted display 1880 has the functions of the above-described head-mounted display 1880 and further includes two display portions.

[0429]

With the two display portions 1882, the user can see one display portion with one eye and the other display portion with the other eye. Thus, a high-resolution image can be displayed even when a three-dimensional display using parallax or the like is performed. The display portion 1882 is curved around an arc with the user's eye as an approximate center. Thus, distances between the user's eye and display surfaces of the display portion become equal; thus, the user can see a more natural image. Even when the luminance or chromaticity of light from the display portion is changed depending on the angle at which the user see it, since the user's eye is positioned in a normal direction of the display surface of the display portion, the influence of the change can be substantially ignorable and thus a more realistic image can be displayed.

[0430]

The operation button 1883 serves as a power button or the like. A button other than the operation button 1883 may be included.

[0431]

As illustrated in FIG. 19E, lenses 1885 may be provided between the display portions 1882 and the user's eyes. The user can see magnified images on the display portion 1882 through the lenses 1885, leading to higher sense of presence. In this case, as illustrated in FIG. 19E, a dial 1886 for adjusting the position of the lenses may be included to adjust visibility.

[0432]

The display device of one embodiment of the present invention can be used for the display portion 1882. Since the display device of one embodiment of the present invention has extremely high definition, even when an image is magnified using the lenses 1885 as illustrated in FIG. 19E, the pixels are not perceived by the user, and thus a more realistic image can be displayed.

[0433]

FIG. 19F illustrates an example of a television set using the display system of one embodiment of the present invention. In a television set 1890, a display portion 1892 is incorporated in a housing 1891. Note that the housing 1891 is supported by a stand 1893 here.

[0434]

The television set 1890 illustrated in FIG. 19F can be operated by an operation switch of the housing 1891 or a separate remote controller 1894. The display portion 1892 may include a touch sensor. The television set 1890 can be operated by touching the display portion 1892 with a finger or the like. The remote controller 1894 may be provided with a display portion for displaying data output from the remote controller 1894. With an operation key or a touch panel of the remote controller 1894, channels and volume can be controlled and images displayed on the display portion 1892 can be controlled.

[0435]

Note that the television set 1890 is provided with a receiver, a modem, or the like. With the use of the receiver, general television broadcasting can be received. When the television set is connected to a communication network with or without wires via the modem, one-way (from a transmitter to a receiver) or two-way (between a transmitter and a receiver or between receivers) data communication can be performed.

[0436]

This embodiment can be implemented in an appropriate combination with any of the structures described in the other embodiments and the like.

REFERENCE NUMERALS

[0437]

100: display controller; 102: master controller; 103: data processing circuit; 104: frame memory; 106: timing controller; 107: register chain; 108: setup register; 109: touch sensor controller; 110: display device; 111: data driver; 112: gate driver; 113: display portion; 114: pixel; 115: pixel; 116: wiring; 117: wiring; 120: processor; 121: data processing circuit; 122: register value generation circuit; 123: processor controller; 130: DRAM; 131: DRAM controller; 140: touch sensor; 150: optical sensor; 160: clock generation circuit; 220: latch; 221: latch group; 222: latch

group; 223: latch group; 224: latch group; 227: insulating layer; 229: setup register; 230: selector; 240: context generation circuit; and 241: internal context generation circuit.

This application is based on Japanese Patent Application Serial No. 2017-045775 filed with Japan Patent Office on March 10, 2017, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A display system comprising:

a display device comprising a plurality of scan lines arranged in the row direction; and

a display controller comprising a context generation circuit, a setup register, and a data processing circuit,

wherein the context generation circuit is configured to supply a context signal to the setup register in accordance with the row number of the scan line,

wherein the setup register is configured to retain a plurality of setting parameters, and to transmit one of the plurality of setting parameters to the data processing circuit in accordance with the context signal, and

wherein the data processing circuit is configured to process first image data to second image data based on the one of the plurality of setting parameters, and to supply the second image data to the display device.

2. A display system comprising:

a display device comprising a plurality of scan lines arranged in the row direction; and

a display controller comprising a context generation circuit, a setup register, and a data processing circuit,

wherein the context generation circuit is configured to supply a context signal to the setup register in accordance with the row number of the scan line,

wherein the setup register is configured to retain a plurality of setting parameters, and to transmit one of the plurality of setting parameters to the data processing circuit in accordance with the context signal,

wherein the data processing circuit is configured to process first image data to second image data based on the one of the plurality of setting parameters, and to supply the second image data to the display device, and

wherein the setup register comprises:

a latch group comprising a plurality of latches and configured to retain the plurality of setting parameters; and

a selector between the latch group and the data processing circuit and configured to be supplied with the context signal.

3. The display system according to claim 1 or 2, wherein the display device further comprises a plurality of pixels and a plurality of signal lines.

4. The display system according to claim 1 or 2,

wherein the display device further comprises a first pixel for a first color, a second pixel for a second color, and a signal line,

wherein the first pixel and the second pixel are electrically connected to the signal line, and

wherein the first color is different from the second color.

5. The display system according to claim 1 or 2,

wherein the display device further comprises a plurality of pixels, and

wherein the plurality of pixels each comprises a transistor and one of a liquid crystal element and an EL element.

6. The display system according to claim 1 or 2,

wherein the display device further comprises a plurality of pixels, and

wherein the plurality of pixels each comprises a transistor comprising silicon or metal oxide in a channel formation region.

7. The display system according to claim 1 or 2, wherein the context generation circuit is included in a master controller.

8. An electronic device using the display system according to claim 1 or 2.

FIG. 1

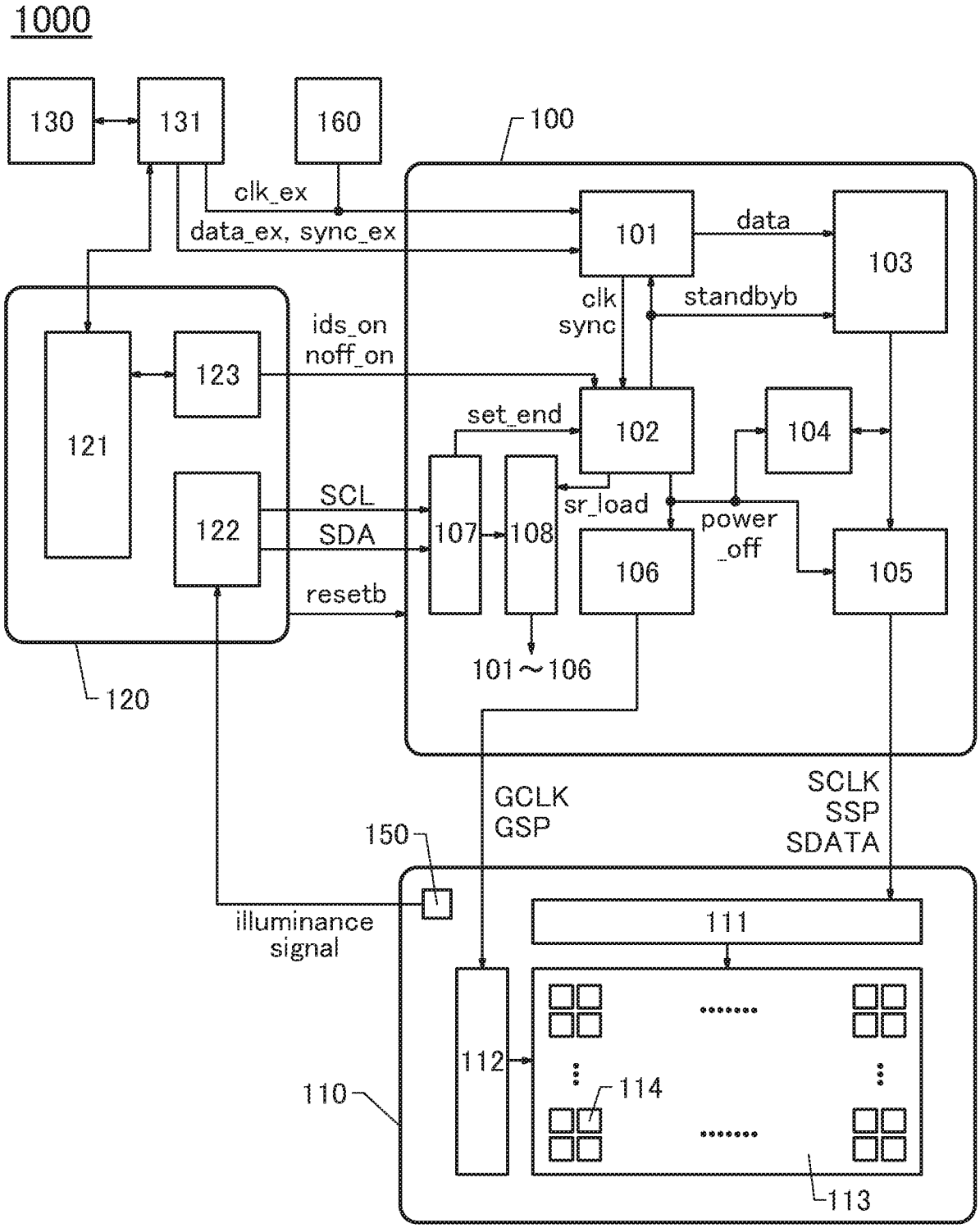

1000
130
131
160
100
clk_ex
data_ex, sync_ex
101
data
103
clk
sync
standbyb
ids_on
noff_on
123
121
set_end
102
104
SCL
SDA
122
107
108
sr_load
power
_off
106
105
resetb
101～106
120
GCLK
GSP
SCLK
SSP
SDATA
150
illuminance
signal
111
112
114
110
113

FIG. 2A

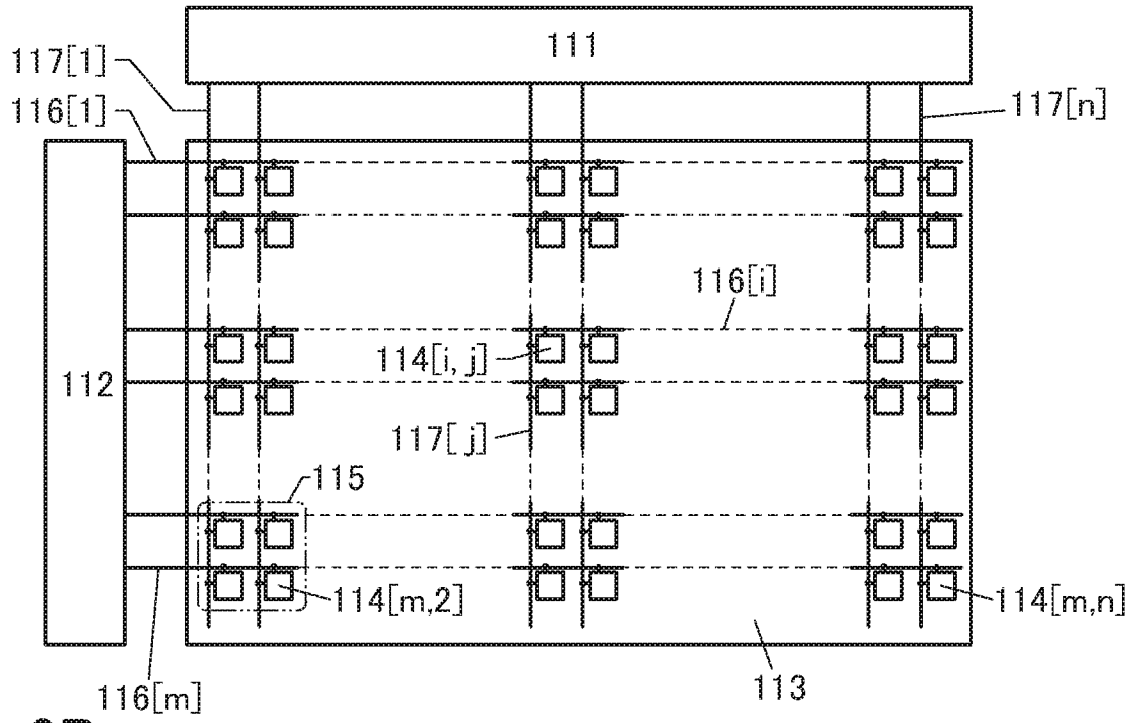


FIG. 2B

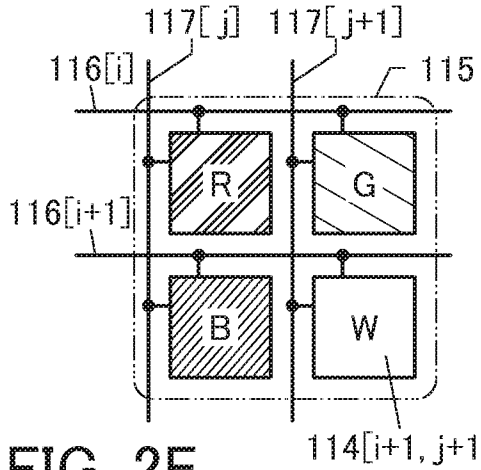


FIG. 2C

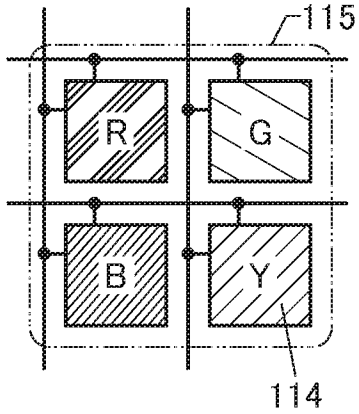


FIG. 2D

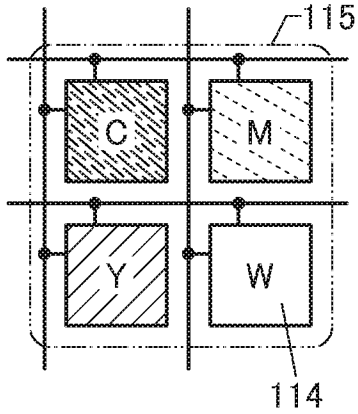


FIG. 2E

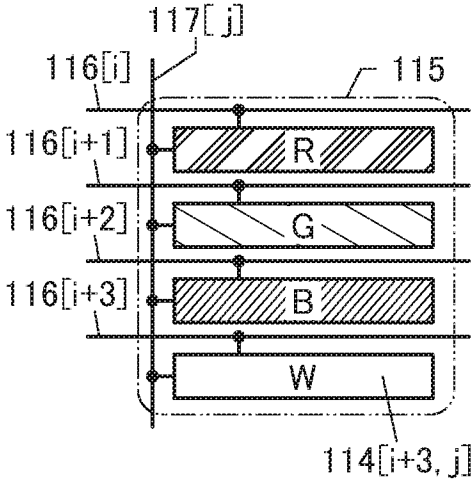


FIG. 2F

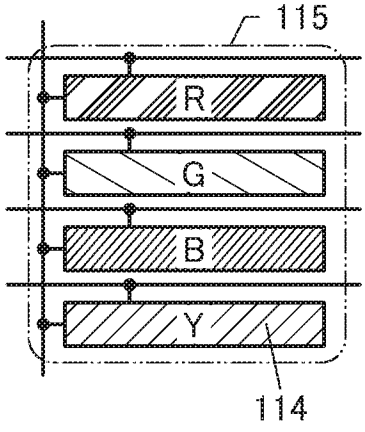


FIG. 2G

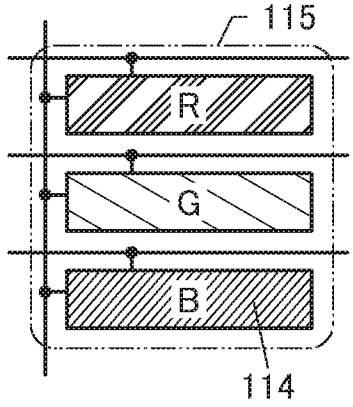


FIG. 3

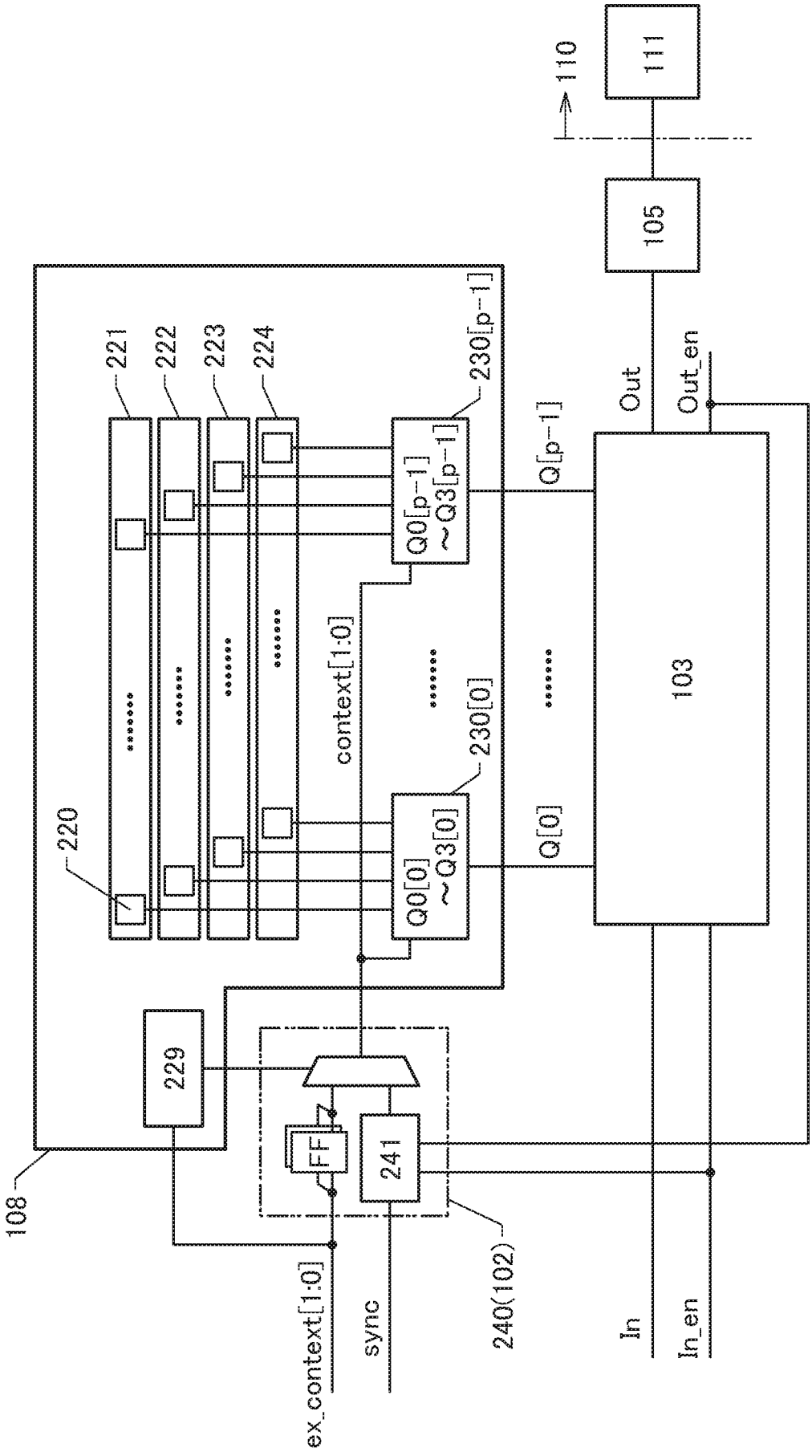

108
220
221
222
223
224
230[p-1]
230[0]
Q0[p-1] ~Q3[p-1]
Q0[0] ~Q3[0]
Q[p-1]
Q[0]
context[1:0]
229
FF
241
240(102)
ex_context[1:0]
sync
In
In_en
Out
Out_en
103
105
110
111

FIG. 4

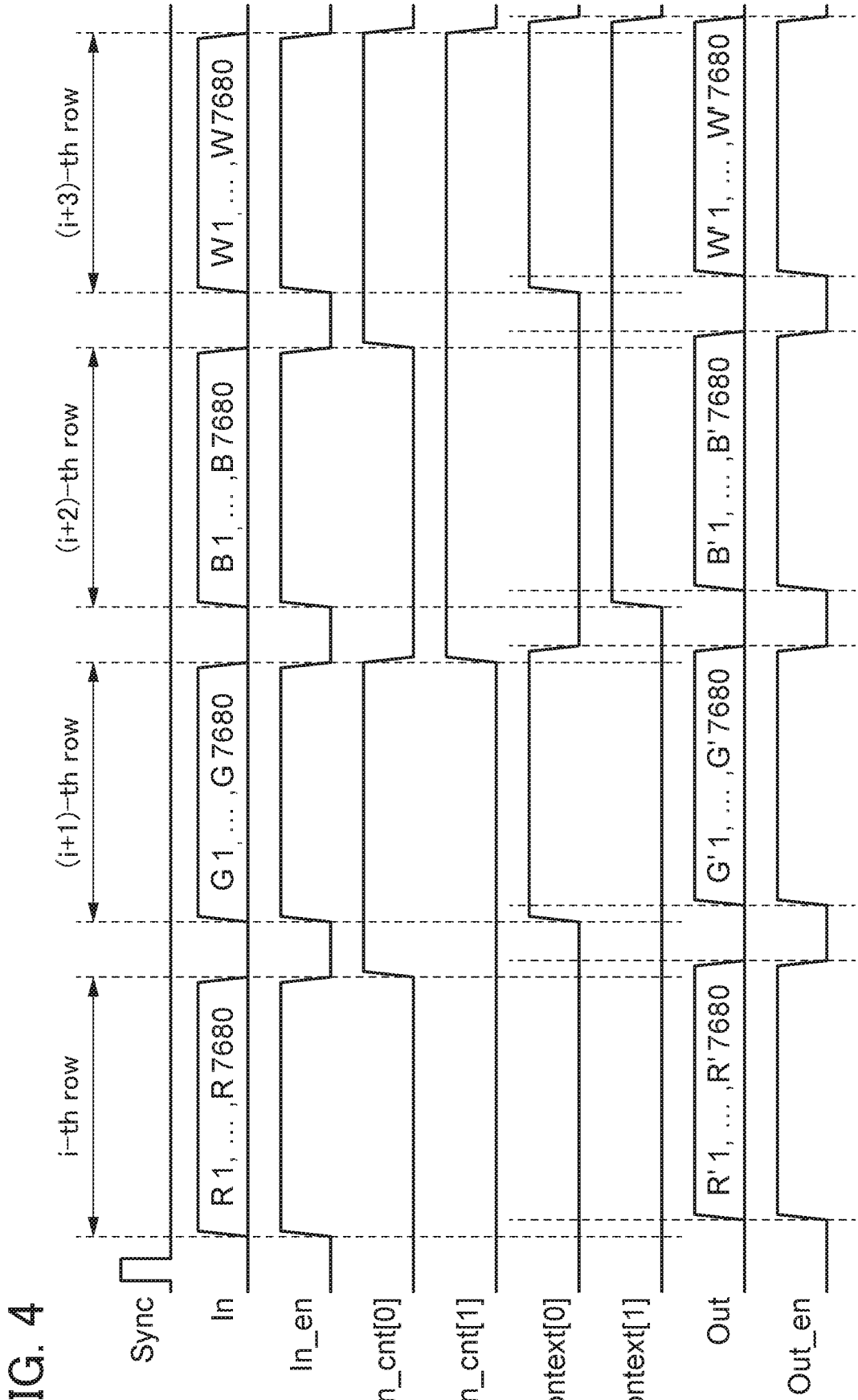

i-th row
(i+1)-th row
(i+2)-th row
(i+3)-th row
Sync
In
In_en
In_en_cnt[0]
In_en_cnt[1]
context[0]
context[1]
Out
Out_en
R 1, ... ,R 7680
G 1, ... ,G 7680
B 1, ... ,B 7680
W 1, ... ,W 7680
R' 1, ... ,R' 7680
G' 1, ... ,G' 7680
B' 1, ... ,B' 7680
W' 1, ... ,W' 7680

FIG. 5

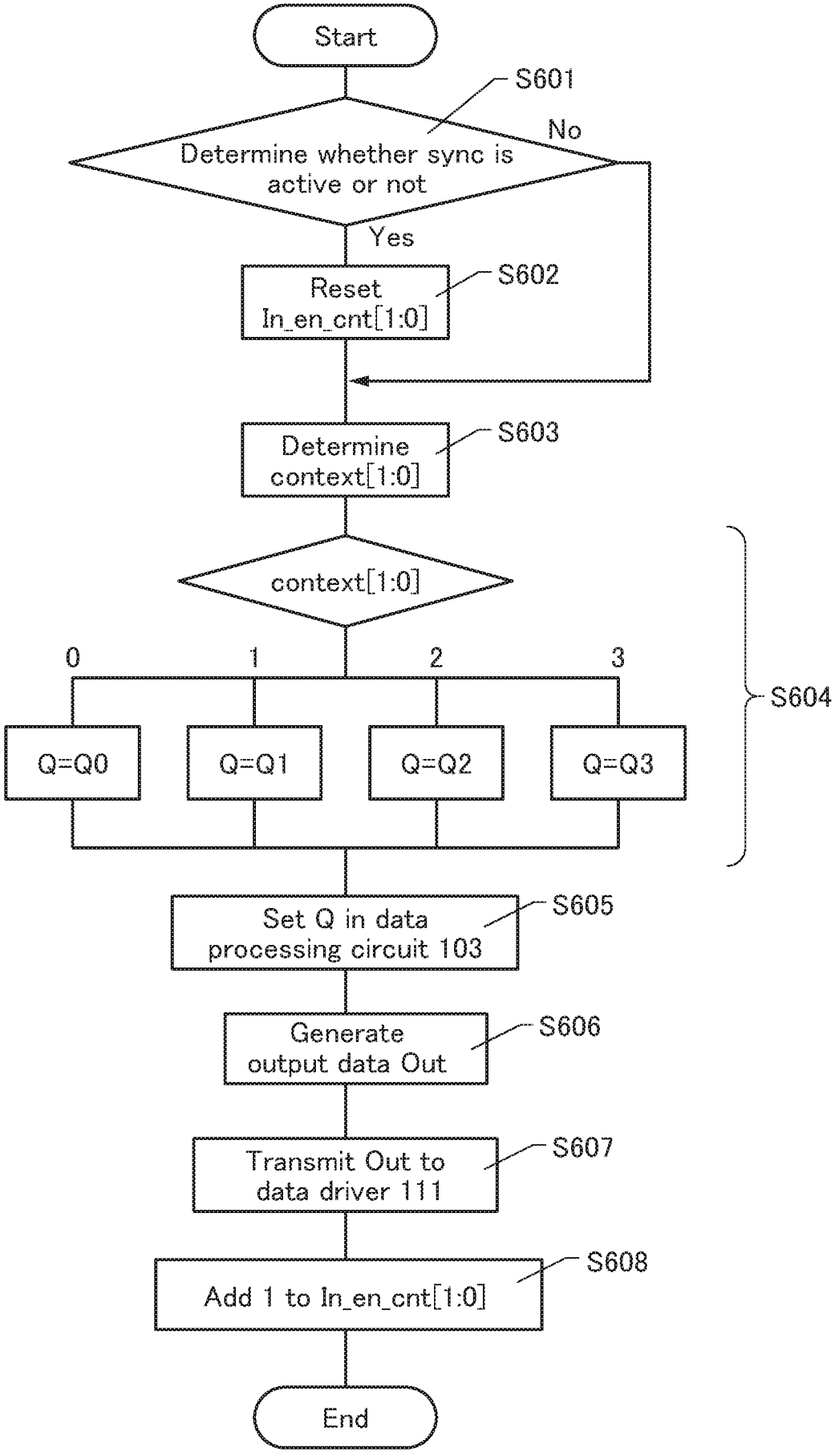

Start
S601
Determine whether sync is active or not
No
Yes
Reset In_en_cnt[1:0]
S602
Determine context[1:0]
S603
context[1:0]
0
1
2
3
Q=Q0
Q=Q1
Q=Q2
Q=Q3
S604
Set Q in data processing circuit 103
S605
Generate output data Out
S606
Transmit Out to data driver 111
S607
Add 1 to In_en_cnt[1:0]
S608
End

FIG. 6

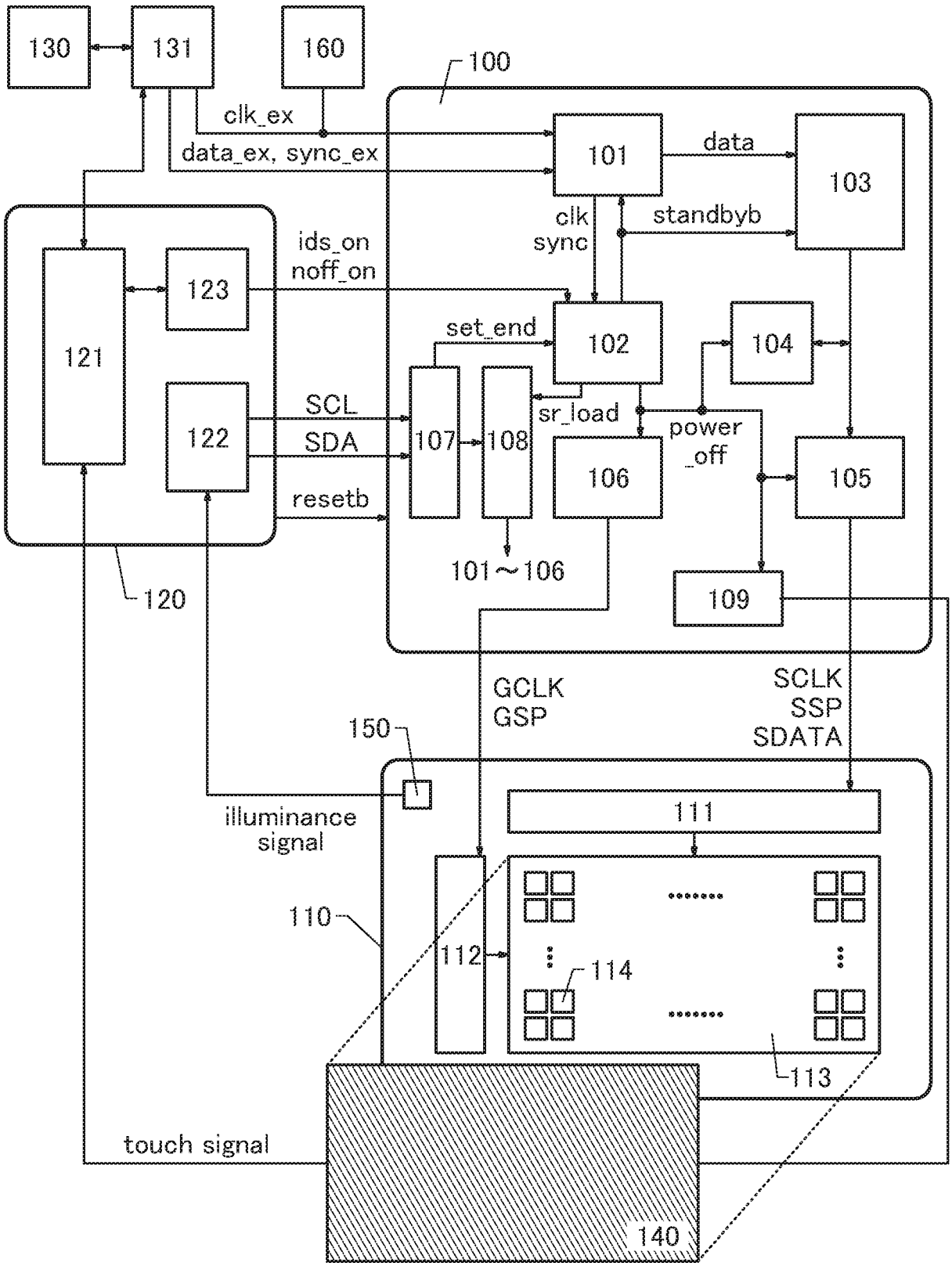

1000A
130
131
160
100
clk_ex
data_ex, sync_ex
101
data
103
clk
sync
standbyb
ids_on
noff_on
123
121
set_end
102
104
SCL
SDA
122
107
108
sr_load
power
_off
106
105
resetb
101～106
120
109
GCLK
GSP
SCLK
SSP
SDATA
150
illuminance
signal
111
110
112
114
113
touch signal
140

FIG. 7A

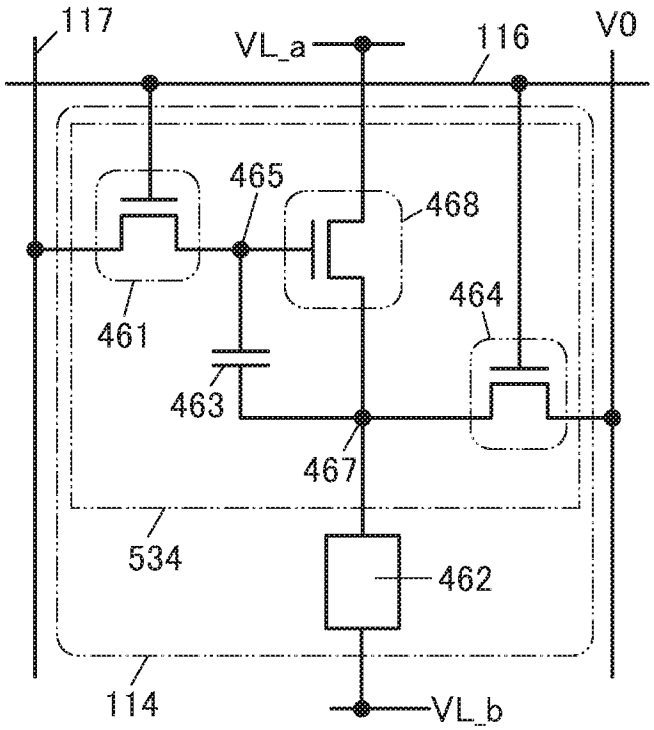


FIG. 7B

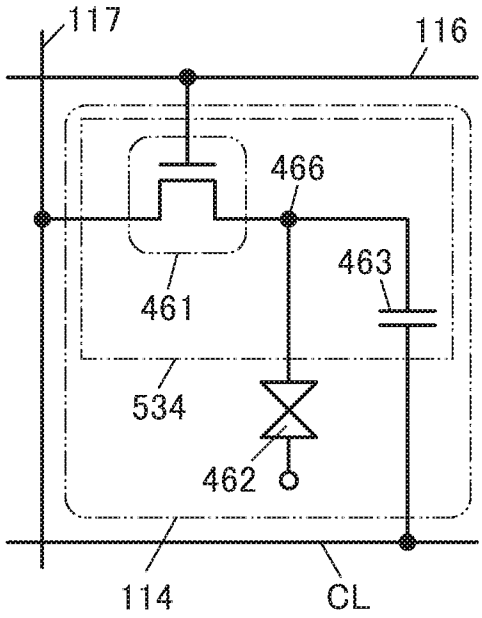


FIG. 7C

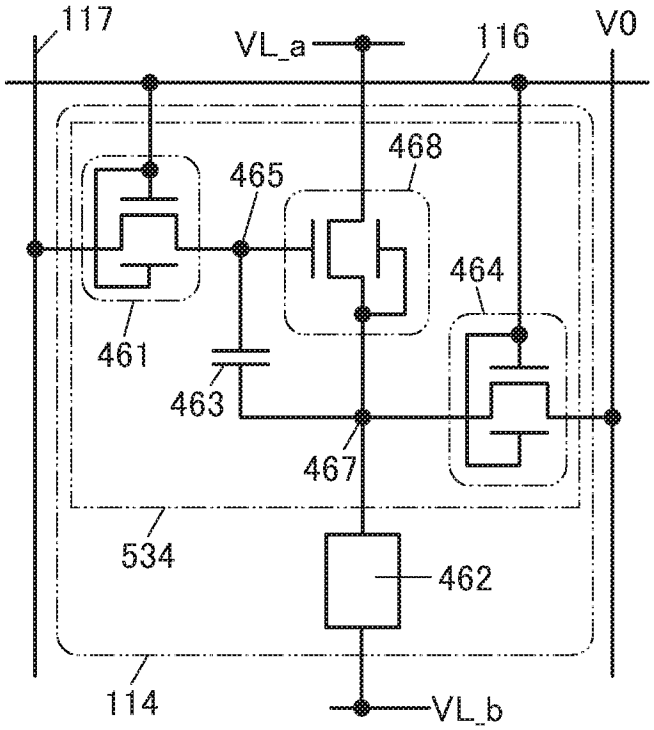


FIG. 7D

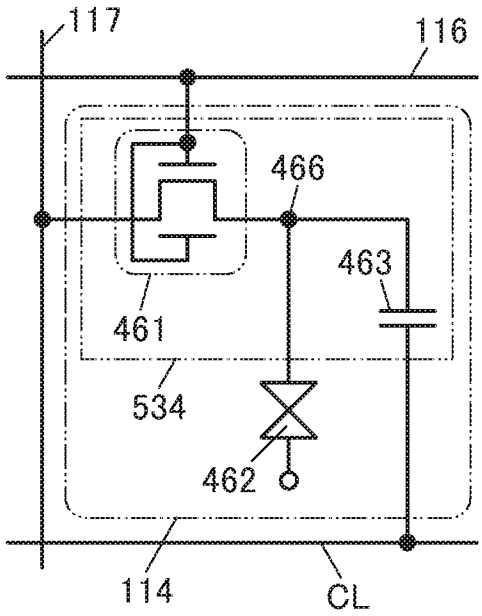


FIG. 8A1

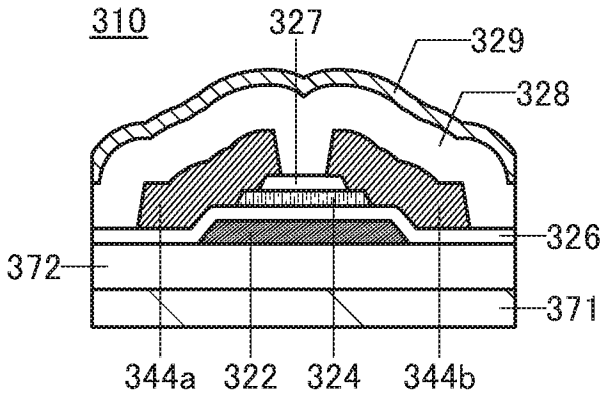


FIG. 8A2

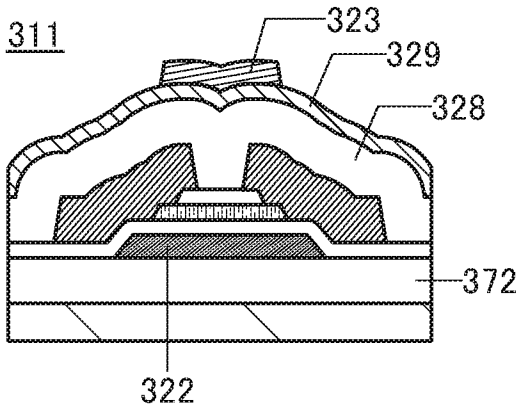


FIG. 8B1

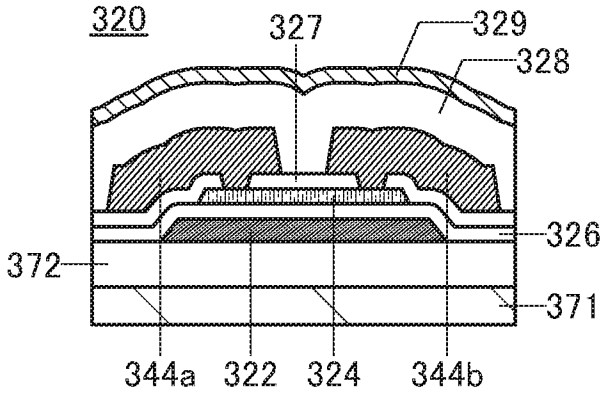


FIG. 8B2

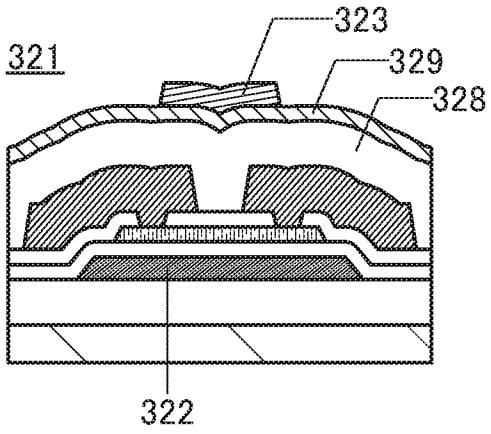


FIG. 8C1

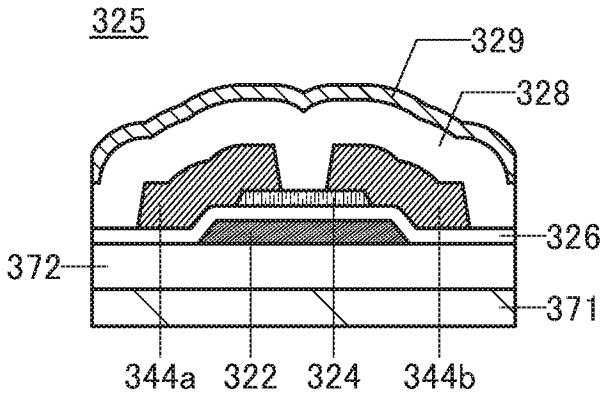


FIG. 8C2

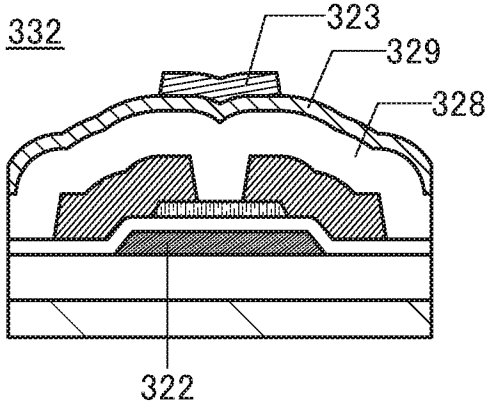


FIG. 9A1

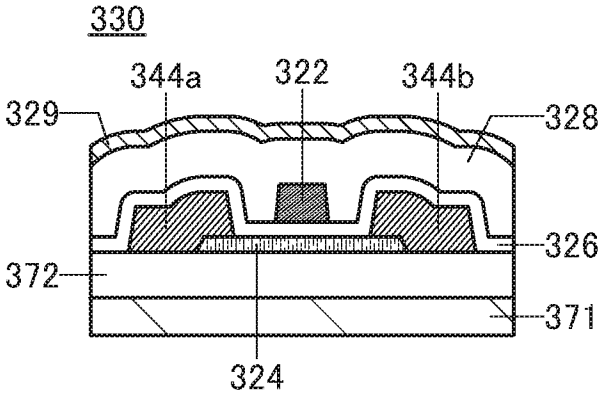


FIG. 9A2

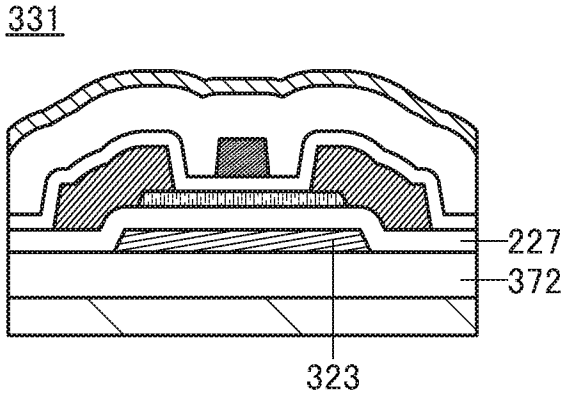


FIG. 9A3

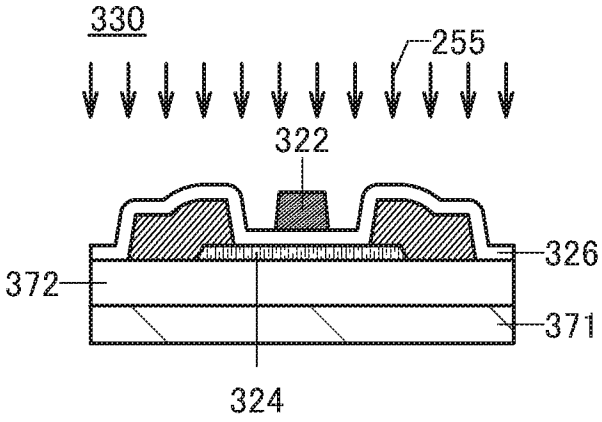


FIG. 9B1

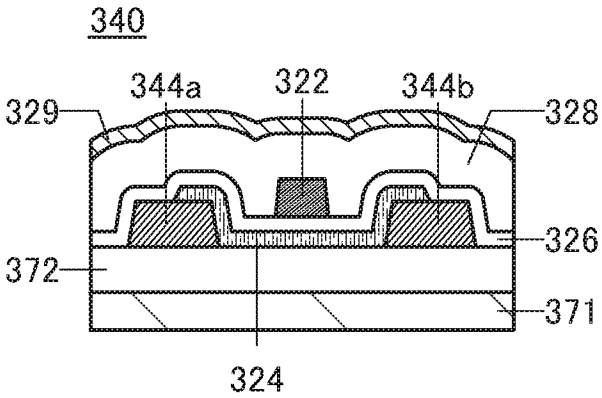


FIG. 9B2

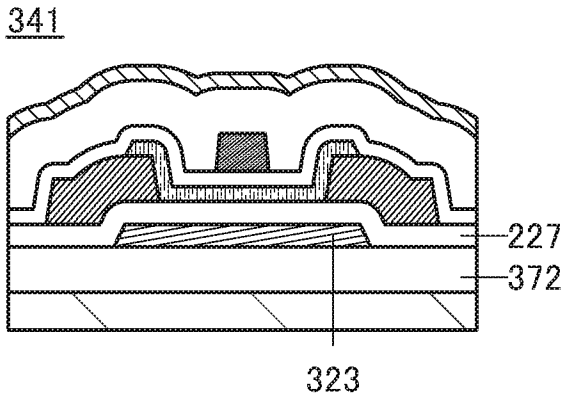


FIG. 10A1

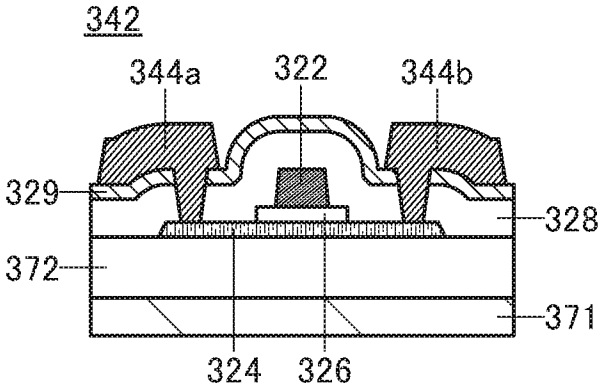


FIG. 10A2

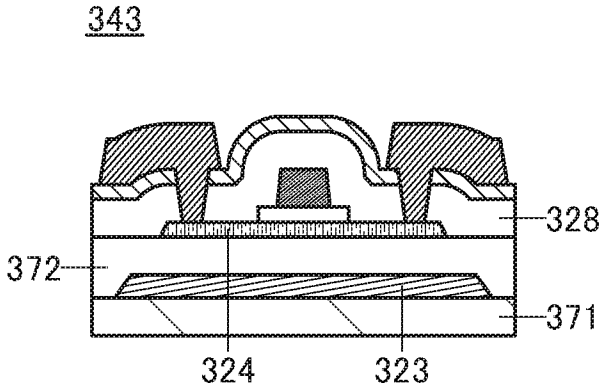


FIG. 10A3

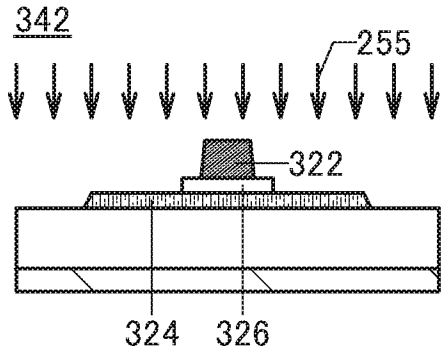


FIG. 10B1

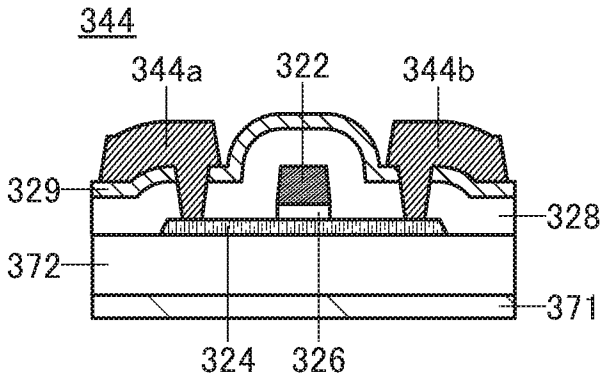


FIG. 10B2

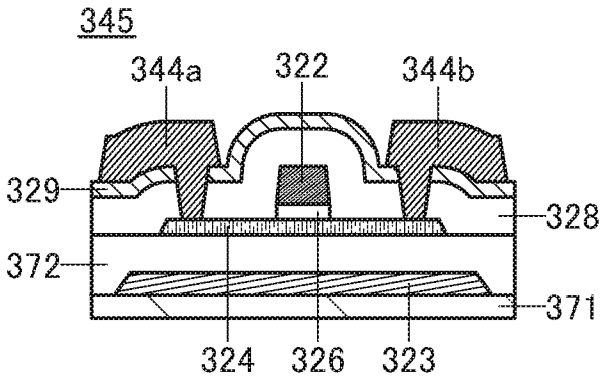


FIG. 10C1

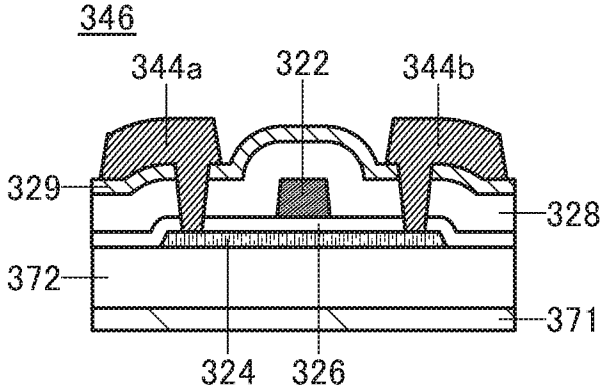


FIG. 10C2

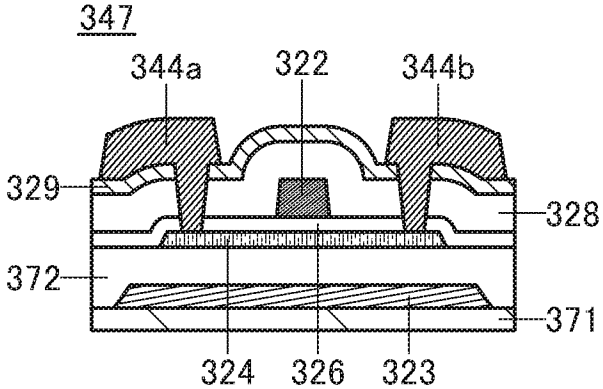


FIG. 11A

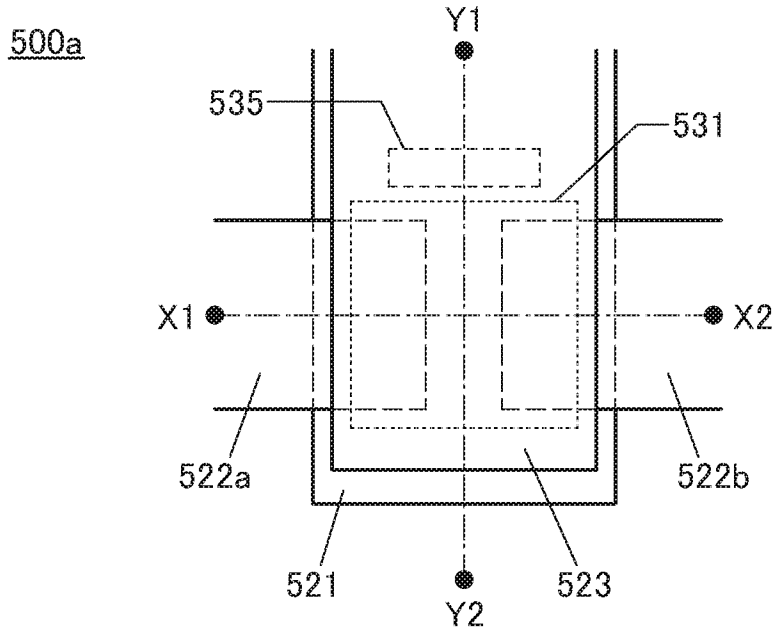


FIG. 11B

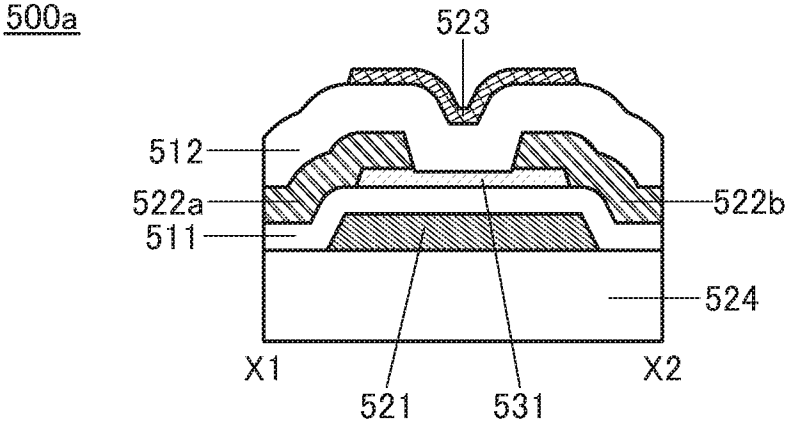


FIG. 11C

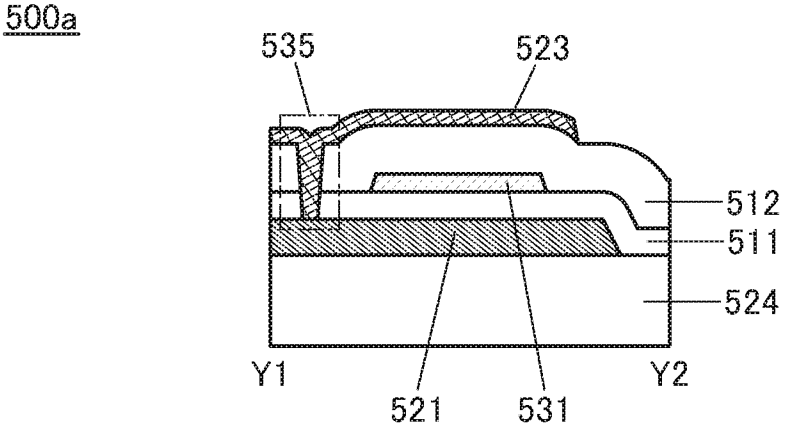


FIG. 12A

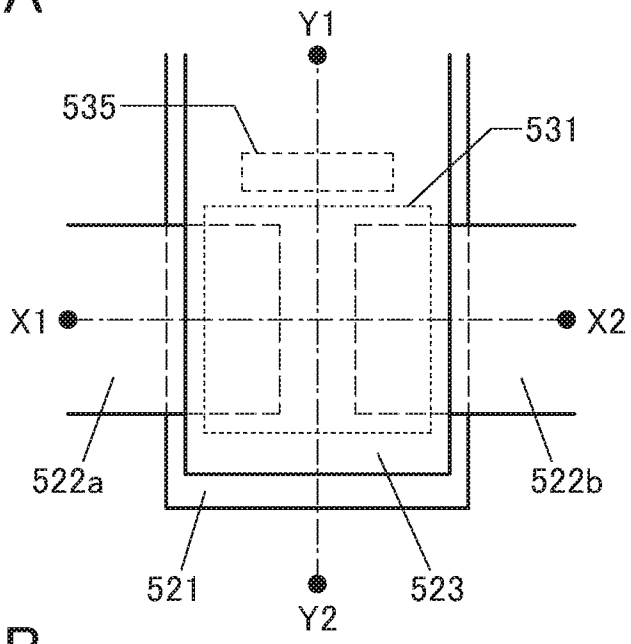


FIG. 12B

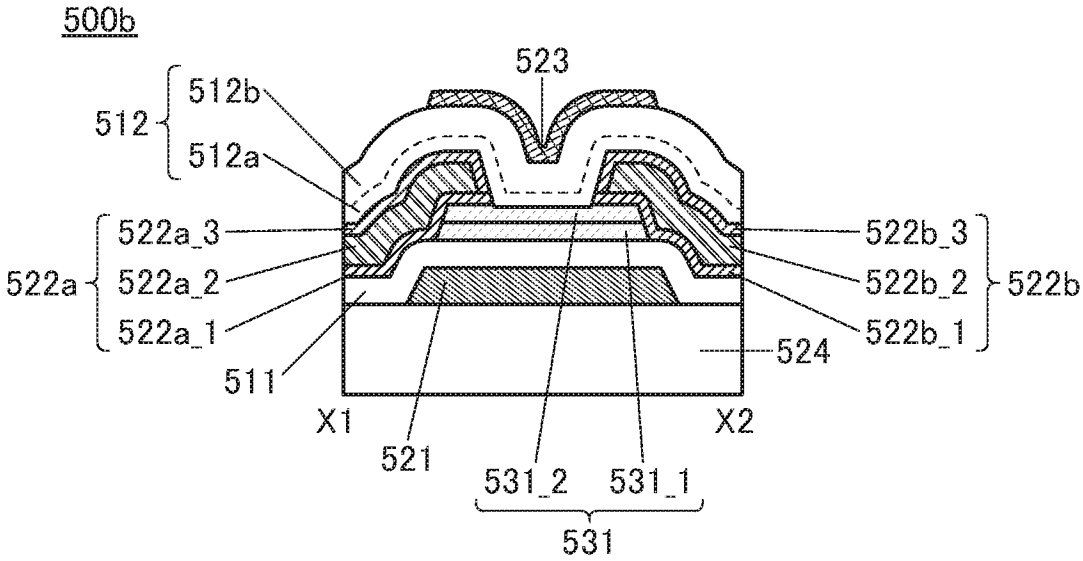


FIG. 12C

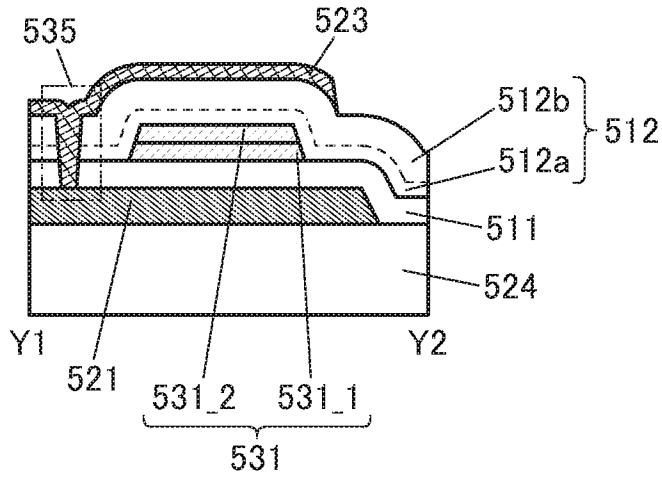


FIG. 13A

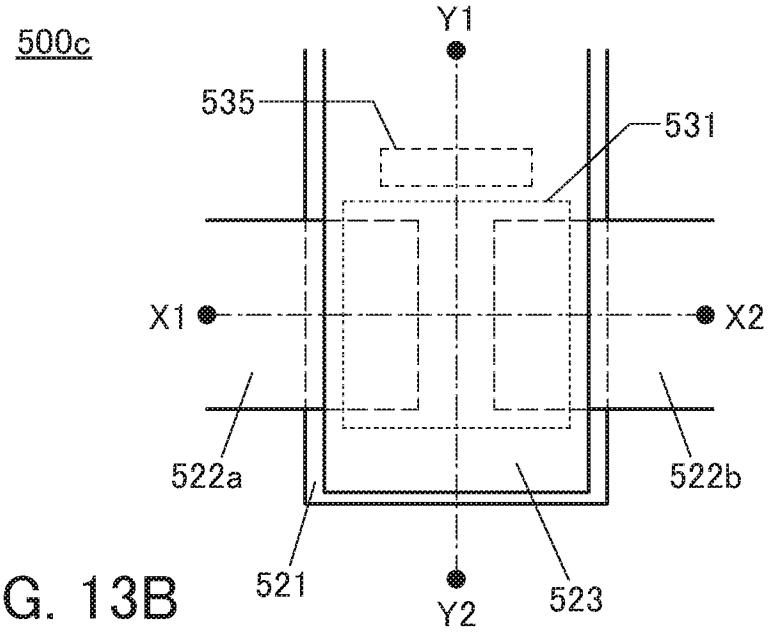


FIG. 13B

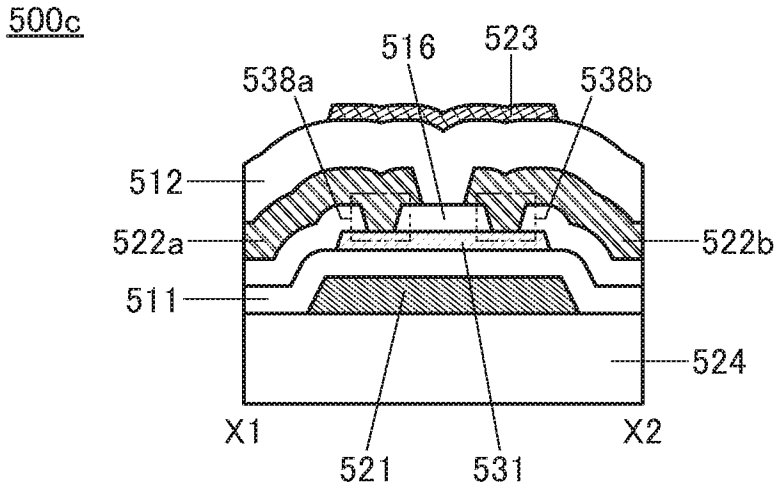


FIG. 13C

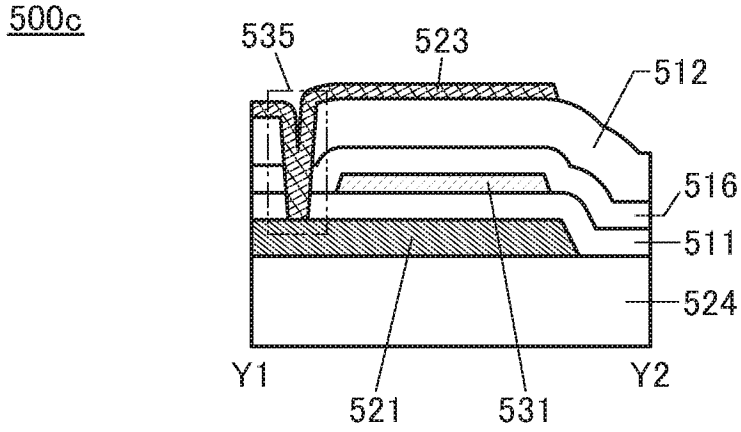


FIG. 14A

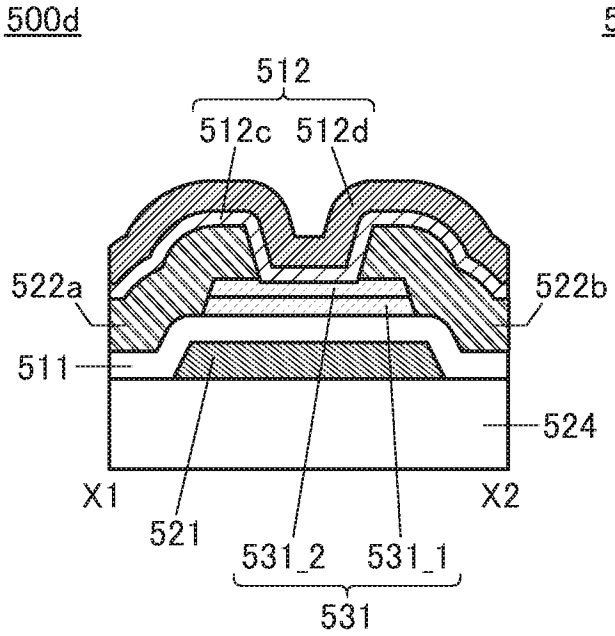


FIG. 14B

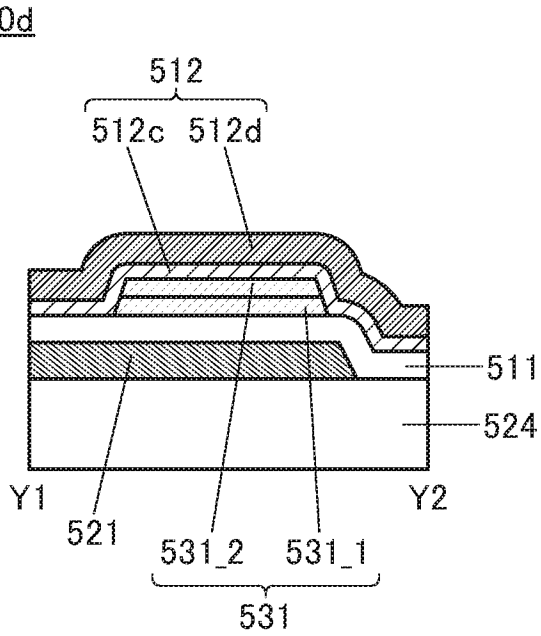


FIG. 14C

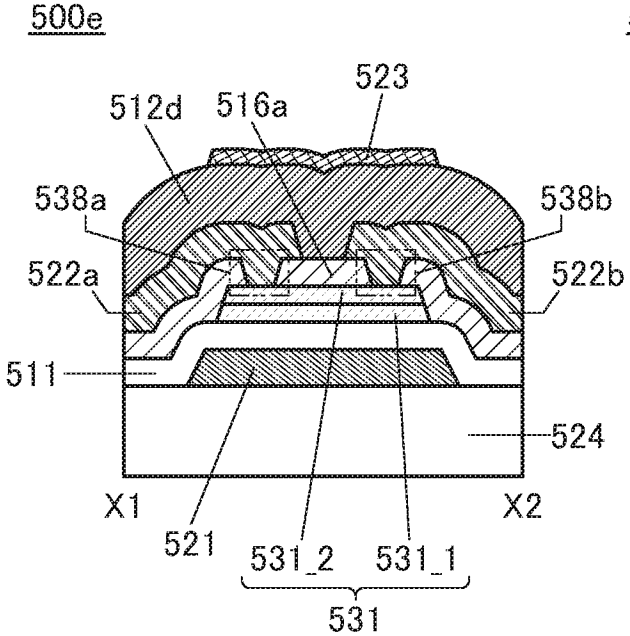


FIG. 14D

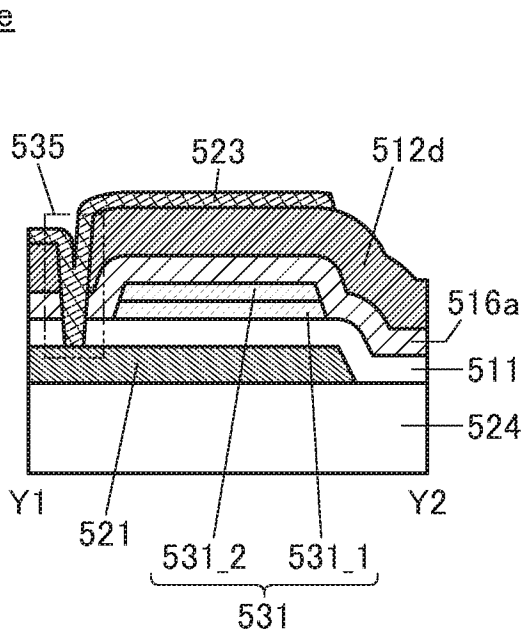


FIG. 15A

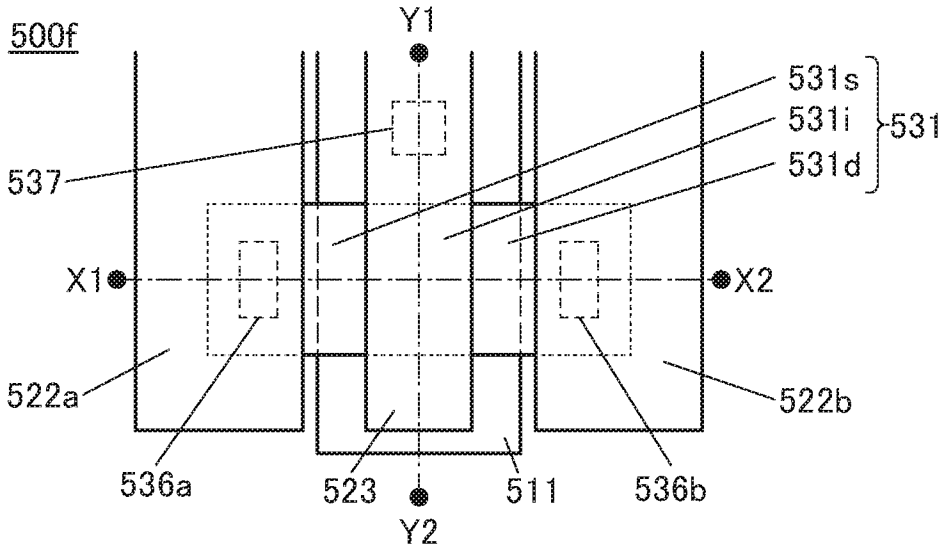


FIG. 15B

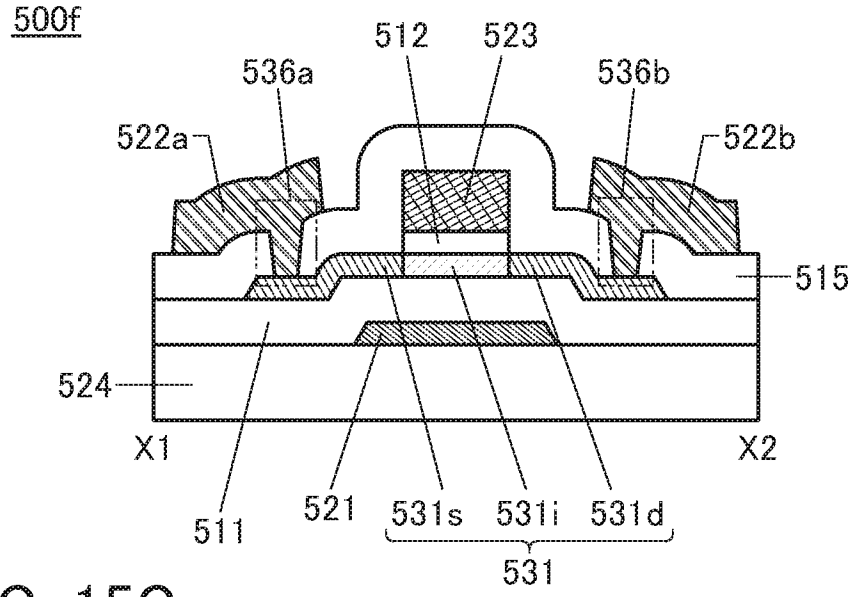


FIG. 15C

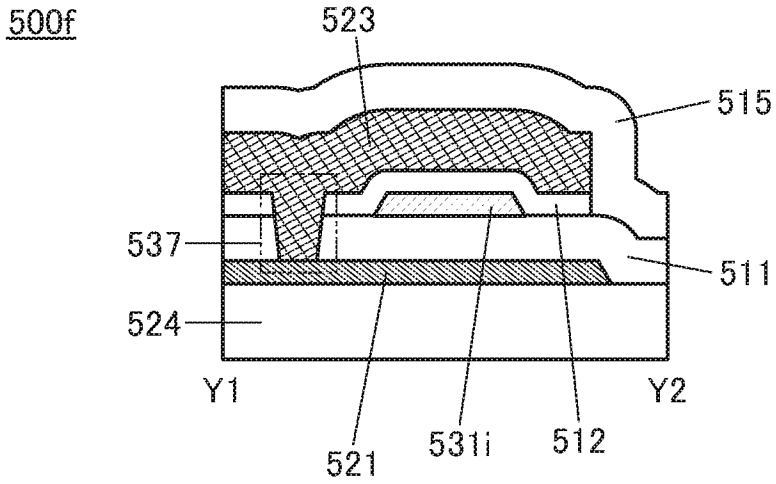


FIG. 16A

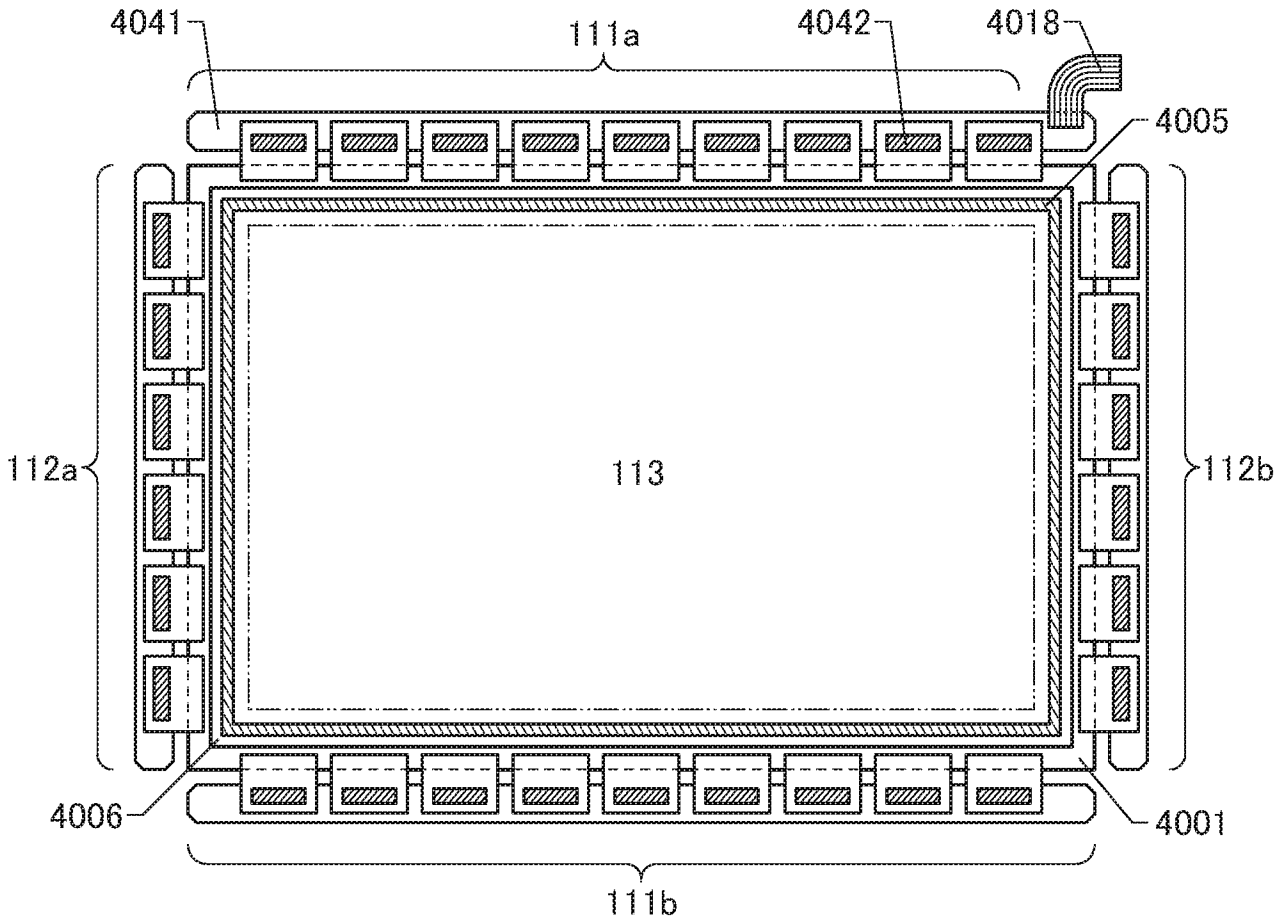


FIG. 16B

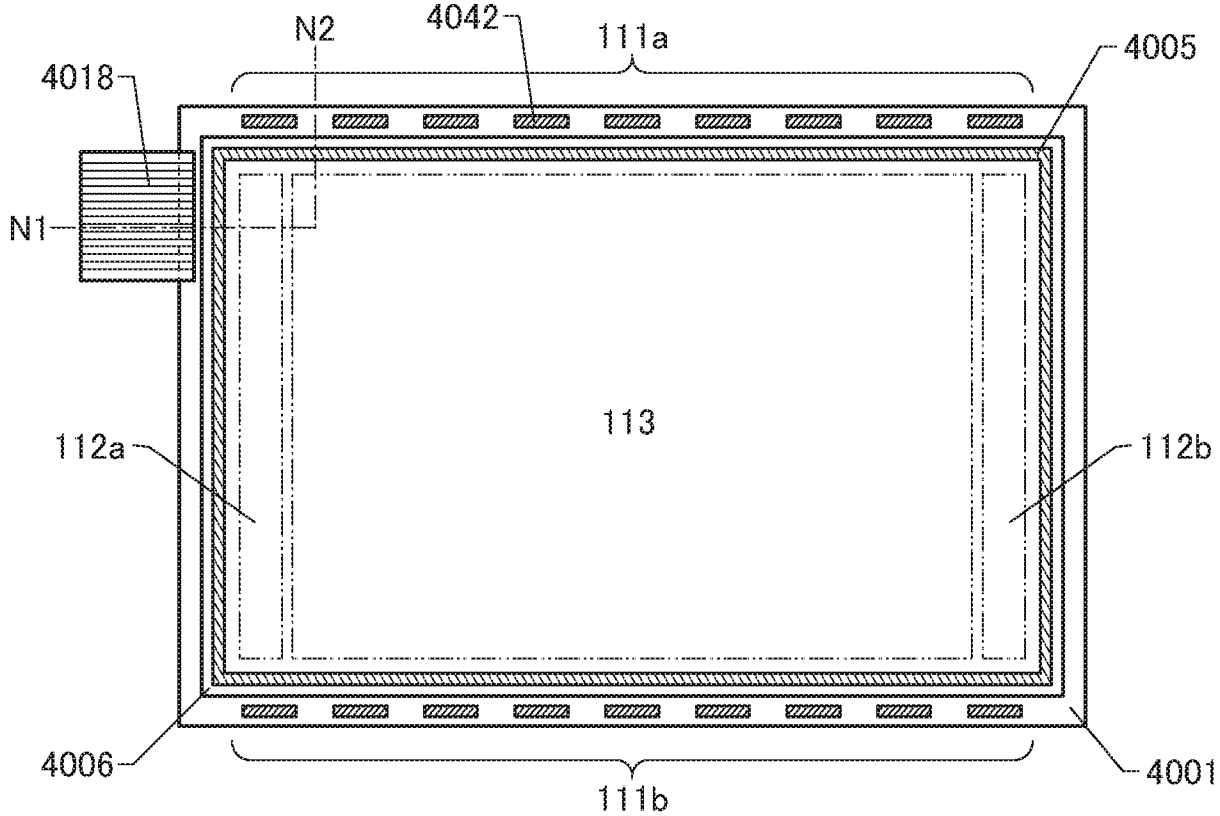


FIG. 17A

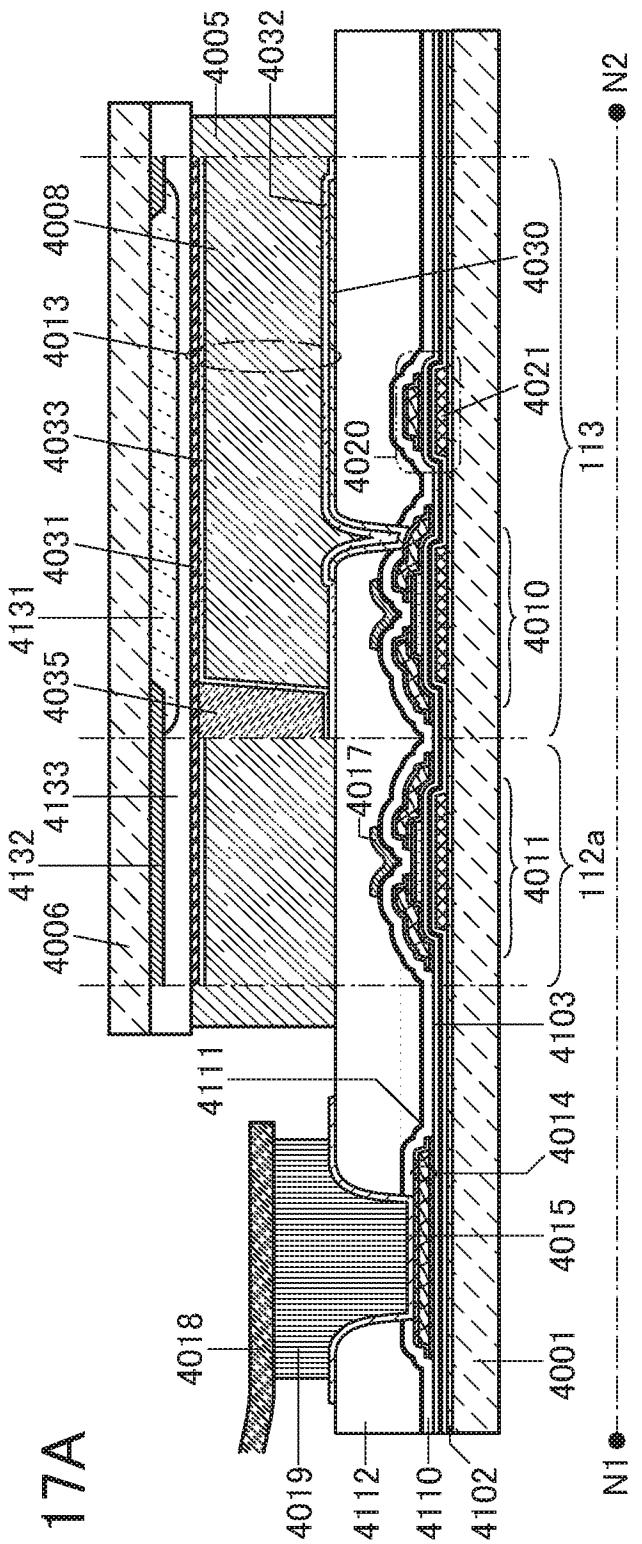


FIG. 17B

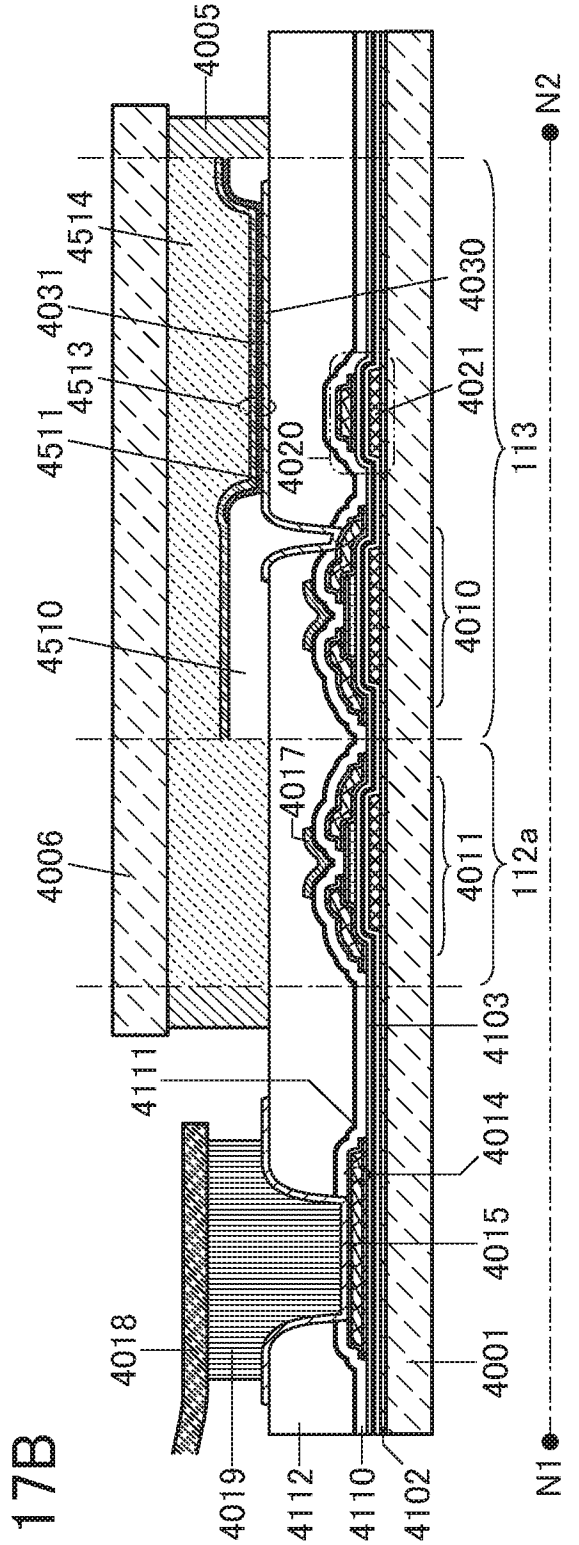


FIG. 18A

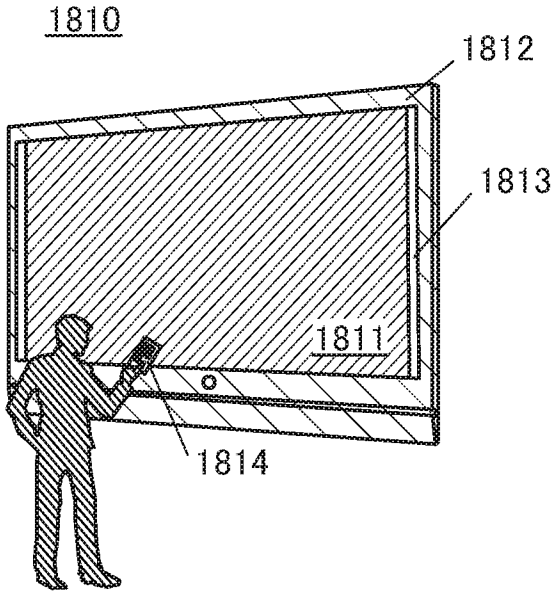


FIG. 18B

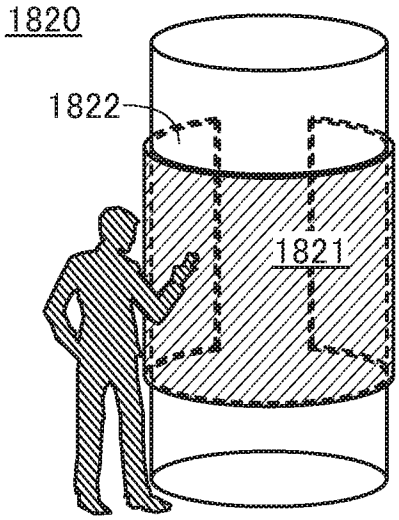


FIG. 18C

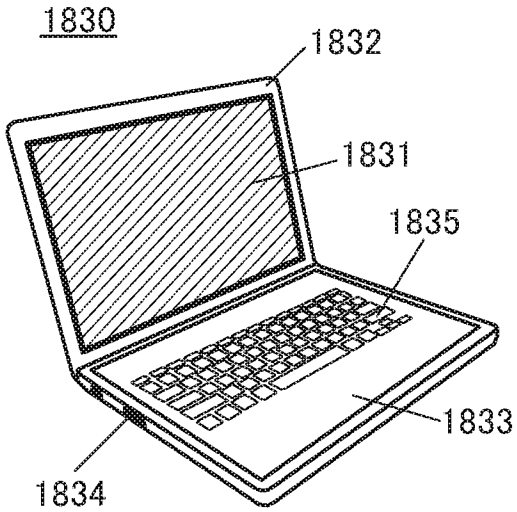


FIG. 18D

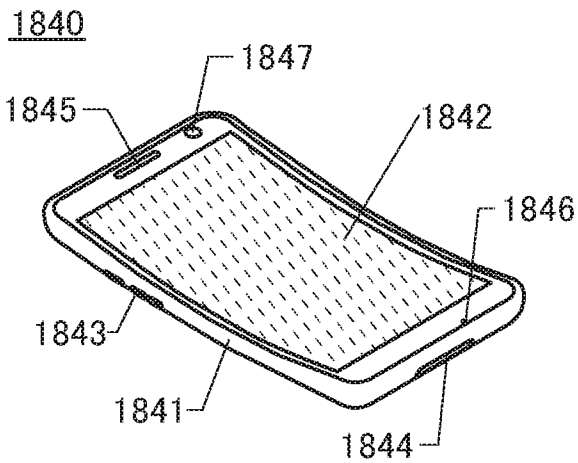


FIG. 18E

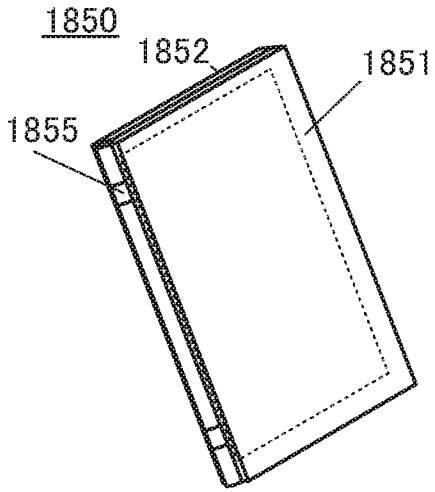


FIG. 18F

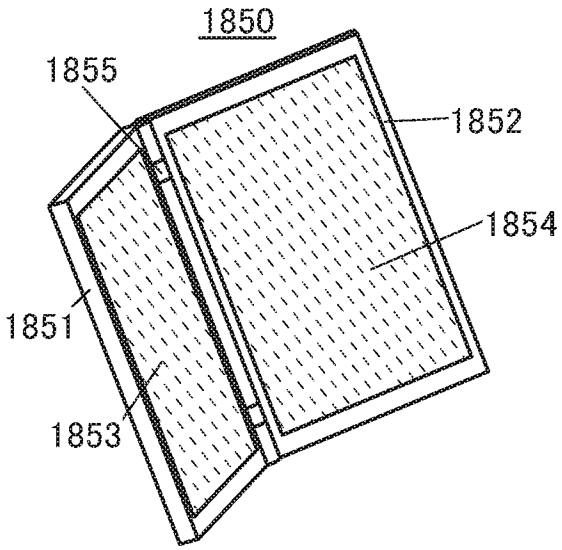


FIG. 19A

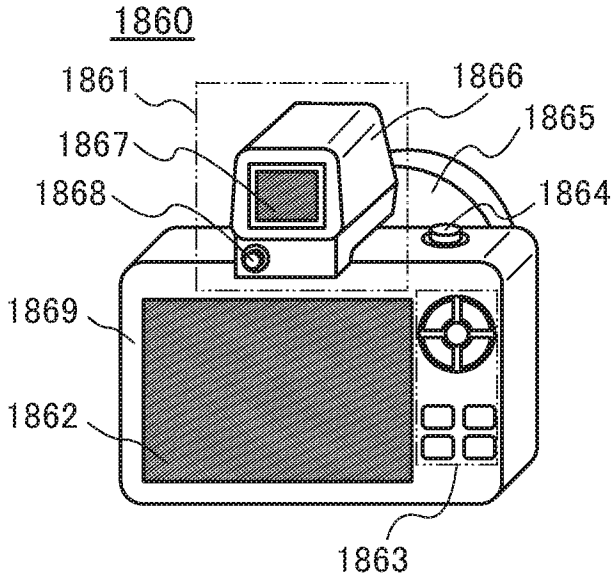


FIG. 19B

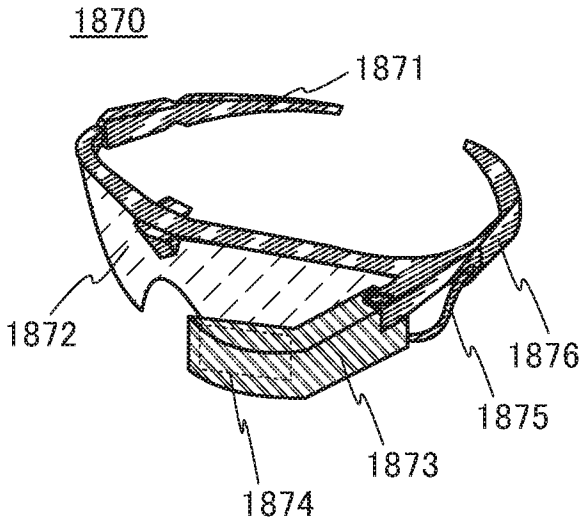


FIG. 19C

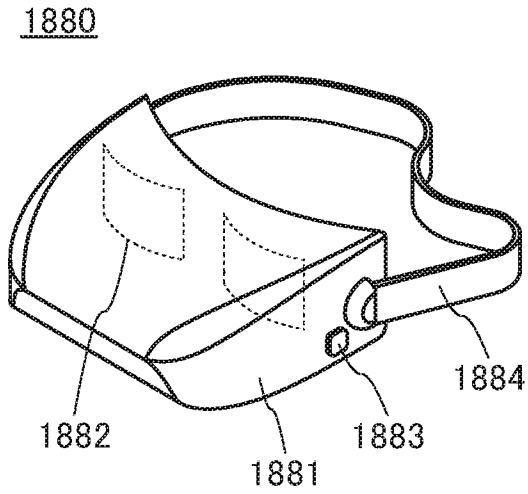


FIG. 19D

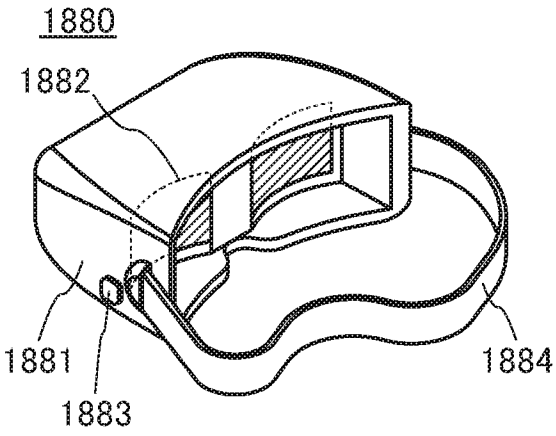


FIG. 19E

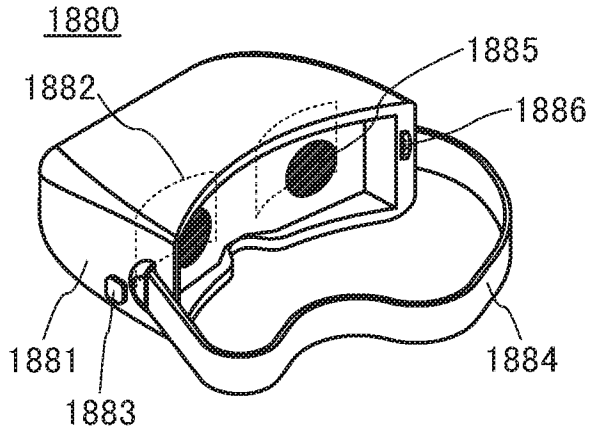
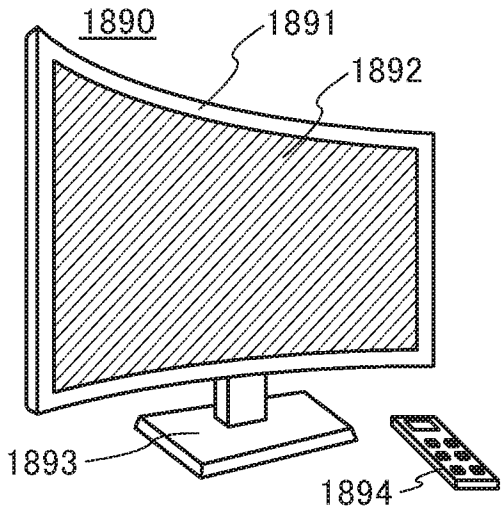


FIG. 19F



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2018/051250

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G09G3/20(2006.01)i, G09G3/3233(2016.01)i, G09G3/36(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G09G3/20, G09G3/3233, G09G3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2018
Registered utility model specifications of Japan 1996-2018
Published registered utility model applications of Japan 1994-2018

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2006-317566 A (SANYO EPSON IMAGING DEVICES CORPORATION) 2006.11.24, Paragraphs 0006-0022, 0042, Figs. 1-6 (No Family)	1-8
Y	JP 6-230760 A (HITACHI, LTD.) 1994.08.19, Paragraphs 0015-0037, Figs. 1-3 (No Family)	1-8
A	JP 2003-280615 A (SHARP KABUSHIKI KAISHA) 2003.10.02, & US 2003/0132906 A1 & TW 200302449 A & CN 1432993 A & KR 10-0520861 B1	1-8
A	US 2009/0278866 A1 (KIM, Jong-Soo) 2009.11.12, & KR 10-2009-0116874 A	1-8

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12.06.2018	26.06.2018

Name and mailing address of the ISA/JP	Authorized officer
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