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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

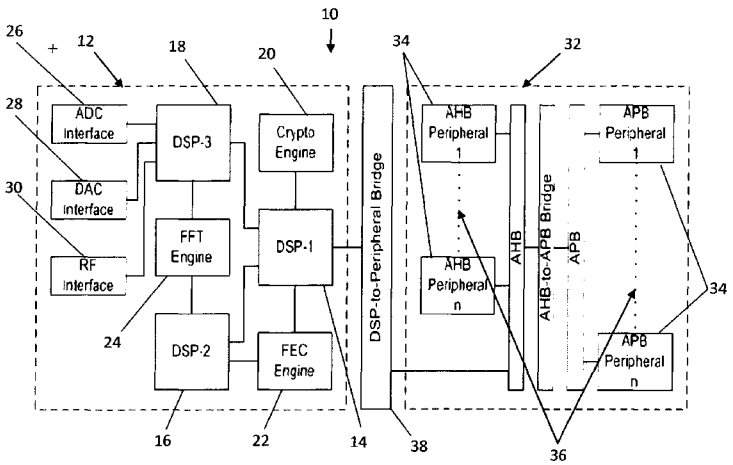
— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: A SYSTEM-ON-CHIP FOR BASEBAND PROCESSING

FIG. 1



(57) **Abstract**: The present invention provides a System-on-Chip which consists of a plurality of DSPs (Digital Signal Processor) coupled with a plurality of hardware accelerators capable of providing high performance computational function and flexibility for future updates. A master processor [14] coordinates MAC and PHY layer operation and subdivides frequency and time domain operation to two secondary processors [16, 18]. An embodiment of the SoC architecture according to the present invention further includes a crypto engine, FEC (Forward-Error-Correction) engine and FFT (Fast-Fourier-Transform) engine, ADC (Analog-to-Digital converter) interface, DAC (Digital-to-Analog converter) interface, and RF (Radio-frequency) interface; a peripheral subsystem in which consist of a plurality of controllers connected through system bus; and a DSP-to-Peripheral bridge which coupled to DSP-1 and the peripheral subsystem wherein said bridge is responsible for critical protocol conversion and eliminates contention in data path.

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A SYSTEM-ON-CHIP FOR BASEBAND PROCESSING

The present invention relates to chip processors. More particularly, the invention relates to chip processors for wireless baseband processing.

BACKGROUND ART

Advances in semiconductor technology have provided high performance, miniaturized processors coupled with wireless communications connectivity. SoC (System-on-chip) architecture refers to an integrated circuit formed on a single chip substrate which consists of a plurality of processors, system buses, hardware accelerators, interface controller and other necessary elements of a desired electronic system where it may contain digital, analog, mixed-signal, or radio-frequency functions. SoC technology is integrated into the wireless communications systems such as baseband processing system.

Baseband processing refers to the execution of digital communication functions that occur within the frequency range around zero before modulation during transmission and after demodulation during reception.

Good desirable SoC architecture for wireless applications such as baseband processing has to be flexible and possess powerful real-time processing capabilities.

However, existing SoC architecture for wireless applications has a fixed structure which only enables certain wireless applications and not flexible for multiple wireless system solutions. Existing SoC architecture uses shared memory and system bus to connect processors and external peripherals which results bottleneck and contentions in data flow which affects the prompt response to real-time data and is not suitable for real-time signal processing.

The present invention is made in view of the problems cited. It is an object of the invention to provide an improved SoC architecture for wireless applications by improving prompt response real-time data.

SUMMARY OF INVENTION

The present invention provides a SoC architecture which is capable of eliminating the contentions in data flow and flexible for multiple wireless system solutions. The SoC architecture consists of a DSP (Digital-Signal-Processors) subsystem in which consist of a plurality of DSPs coupled with a plurality of hardware accelerators, capable of providing high performance computational function and flexibility for future updates. The SoC architecture also consists of dedicated connections between its components on the critical data path to avoid contentions.

An embodiment of the SoC architecture according to the present invention includes a DSP (Digital-Signal-Processors) subsystem in which consists of a master processor, two secondary processors, a crypto engine, FEC (Forward-Error-Correction) engine, FFT (Fast-Fourier-Transform) engine, ADC (Analog-to-Digital converter) interface, DAC (Digital-to-Analog converter) interface, and RF (Radio-frequency) interface; a peripheral subsystem in which consist of a plurality of controllers connected through system bus; and a DSP-to-Peripheral bridge which is coupled to master processor and the peripheral subsystem wherein said bridge is responsible for critical protocol conversion and eliminates contention in data path.

Master processor is coupled directly with secondary processors to improve responsiveness of real-time data between the DSPs. Master processor functions to coordinate the whole chip operation and MAC (Media Access Control) layer operation. Both secondary processors are configured to be slave processors, each performing PHY (Physical) layer frequency domain operation, or performing the PHY layer time domain operation. The dedicated channels that links the modules together, enables a seamless data flow for both the transmitter and receiver flows.

BRIEF DESCRIPTION OF DRAWINGS

Further characteristics and advantages of the present invention will become better apparent from the following detail description of a preferred but not exclusive embodiment thereof, illustrated by way of non-limiting example in the accompanying drawings, wherein:

FIG. 1 is a top level block diagram of the SoC architecture for wireless applications according to the invention;

+

FIG. 2 is a flow chart showing a typical data transmission and reception flow of a typical wireless system; and

FIG. 3 is a diagram showing the processing task distribution between DSPs through the connections of DSPs as shown in FIG. 1.

DESCRIPTION OF EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention which is intended to provide a thorough understanding of the present invention. However, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

In an embodiment of the present invention, a block diagram of SoC architecture [10] fabricated on a single integrated chip such as silicon is as shown in FIG. 1. A SoC architecture [10] comprising a DSP (Digital Signal Processor) subsystem [12] includes a master processor DSP-1 [14], a first secondary processor DSP-2 [16], a second secondary processor DSP-3 [18], a crypto engine [20], a FEC (Forward-Error-Correction) engine [22], a FFT (Fast-Fourier-Transform) engine [24], an ADC (Analog-to-Digital converter) interface [26], a DAC (Digital-to-Analog converter) interface [28], and a RF (Radio-frequency) interface [30]; a peripheral subsystem [32] includes a plurality of controllers [34] connected through system bus [36]; and a DSP-to-Peripheral bridge [38] which coupled to DSP-1 [14] and the peripheral subsystem [32] where said bridge [38] is responsible for critical protocol conversion.

DSP-1 [14] is in direct connection with secondary processors such as DSP-2 [16] and DSP-3 [18] and is supported by accelerators such as crypto engine [20] and FEC engine [22]. The crypto engine [20] encrypts higher layer data into MAC layer data, as well as decrypts MAC layer data into higher layer data. FEC engine [22] transfers encoded data from master processor DSP-1 to first secondary processor DSP-2, as well as transfers

error corrected data from first secondary processor DSP-2 to master processor DSP-1. The first secondary processor DSP-2 [16] provides PHY layer frequency domain operation; and the second secondary processor DSP-3 [18] provides PHY layer time domain operation. DSP-2 [16] is coupled to fast-Fourier-transform (FFT) engine [24], said engine perform frequency domain processing for transmission of MAC protocol. Fast Fourier Transform operation is performed on frequency domain signal or frequency domain signal is delivered from Inverse Fast Fourier Transform. DSP-3 [18] is coupled to a fast-Fourier-transform (FFT) engine [24], said engine perform time domain processing for transmission of MAC protocol. Inverse Fourier Transform operation is performed on time domain signal or time domain signal is delivered from Fast Fourier Transform operation. This configuration of the DSP subsystem [10] component result in a faster processing speed compared to existing system solution. DSP-1 [14] is also in direct connection with peripheral subsystem [32] via DSP-to-Peripheral bridge [38] and this provides a dedicated path for critical protocol conversion and eliminates the problem of contentions in data path occurred in system bus connections.

A method of SoC architecture for wireless application involves transforming data from MAC layer [44] to PHY layer [50] for transmission and from PHY layer [50] to MAC layer [44] for reception.

FIG. 2 shows a typical data transmission flow [40] and reception flow [42] of a typical system. The data transmission flow [40] starts from the DSP-1 [14] wherein DSP-1 [14] collects higher layer data from peripheral subsystem [32] via DSP-to-Peripheral Bridge [38]. The higher layer data is transformed to MAC protocol data units by executing stored program at DSP-1 and encryption at crypto engine [20]. The MAC protocol data units are then transferred to FEC engine [22] for transformation of data to the frequency domain data and are then transferred to DSP-2 [16] for executing stored program. The frequency domain data is then transfered to FFT engine [24] to be transformed to time domain data. DSP-3 [18] collects and processes the time domain data from FFT engine [24] by means of stored program before transferring the binary encoded air interface data to DAC interface [28]. Reception flow [42] follows the reverse path of transmission flow [40] where the binary encoded air interface data is collected at ADC interface [26]. The dedicated channels that link the components together provide a capability of seamless data flow in the SoC architecture [10].

FIG. 3 shows the equal distribution of MAC layer [44] and PHY layer [50] operations from DSP-1 [14] to DSP-2 [16] and DSP-3 [18]. The distributed processing capability doubles the processing power and enables a particular task can be completed in half the time.

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Accordingly, this solution reduces the problems related to inflexible of SoC architecture for multiple wireless system solutions, bottlenecks and contentions in data flow which affects the prompt response to real-time data.

CLAIMS

1. A system-on-chip for baseband processing [10], comprising:
   + a digital-signal-processor (DSP) subsystem [12], having at least a master processor DSP-1 [14] coupled with a plurality of secondary processors and hardware accelerators;
   a peripheral subsystem [32], having a plurality of peripheral controllers being inter-connected;
   a DSP-to-peripheral bridge [38] coupling the master processor DSP-1 [14] with the peripheral subsystem [32].

2. A system-on-chip [10] according to claim 1, wherein the master processor DSP-1 [14] is coupled to a first secondary processor DSP-2, and a second secondary processor DSP-3;
   the master processor DSP-1 [14] coordinates MAC and PHY layer operation;
   the first secondary processor DSP-2 [16] provides PHY layer frequency domain operation; and
   the second secondary processor DSP-3 [18] provides PHY layer time domain operation.

3. A system-on-chip [10] according to claim 2, wherein the master processor DSP-1 [14] is coupled to a crypto engine [20], said crypto engine [20] encrypts higher layer data into MAC layer data, as well as decrypts MAC layer data into higher layer data.

4. A system-on-chip [10] according to claim 2, wherein the master processor DSP-1 [14] and first secondary processor DSP-2 [16] is coupled to a forward-error-correction (FEC) engine [22], said engine transfers encoded data from master processor DSP-1 to first secondary processor DSP-2, as well as transfers error corrected data from first secondary processor DSP-2 to master processor DSP-1..

5. A system-on-chip [10] according to claim 2, wherein the first secondary processor DSP-2 [16] is coupled to a fast-Fourier-transform (FFT) engine [24], said engine performs Fast Fourier Transform operation on frequency domain signal from said

processor or delivers frequency domain signal from Inverse Fast Fourier Transform operation to said processor.

6. A system-on-chip [10] according to claim 2, wherein the second secondary processor DSP-3 [18] is coupled to a fast-Fourier-transform (FFT) engine [24], said engine perform Inverse Fourier Transform operation on time domain signal from said processor or delivers time domain signal from Fast Fourier Transform operation to said processor.

7. A system-on-chip [10] according to claim 2, wherein the second secondary processor DSP-3 [18] is coupled to interfaces comprising analog-to-digital converter (ADC) interface, digital-to-analog converter (DAC) interface, and radio-frequency (RF) interface.

8. A method of transmitting signal in a chip, comprising:
collecting higher layer data from a plurality of peripherals via DSP to peripheral bridge;
encrypting the data into MAC protocol data units;
performing frequency domain processing for transmission of MAC protocol;
performing time domain processing for transmission of MAC protocol; and
transmitting binary encoded air interface data at interface.

9. A method of receiving signal in a chip, comprising:
collecting binary encoded air interface data from interface;
performing time domain processing for reception of MAC protocol;
performing frequency domain processing for reception of MAC protocol;
decrypting the data into higher layer data units; and
transferring the higher layer data to peripherals via DSP to peripherals bridge.

FIG. 1

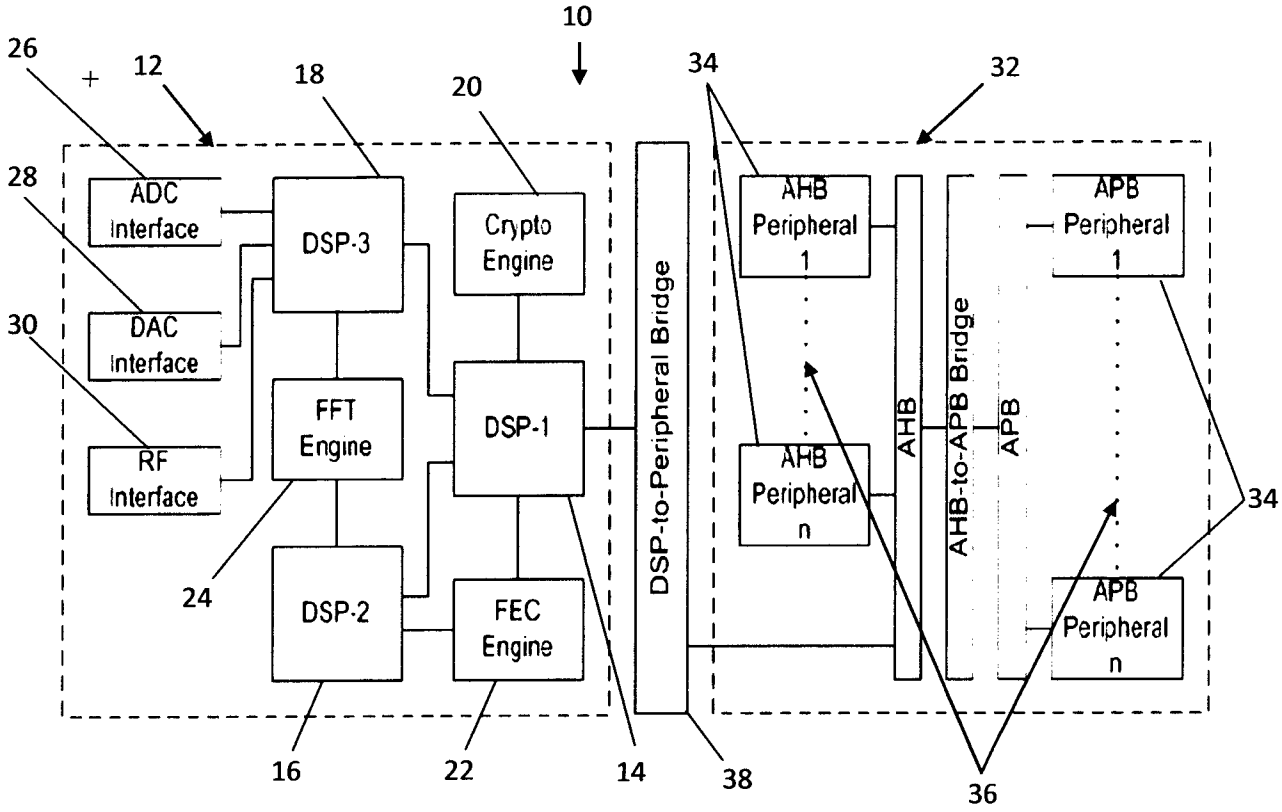

10
26
12
18
20
34
32
28
30
ADC Interface
DAC Interface
RF Interface
DSP-3
FFT Engine
DSP-2
Crypto Engine
DSP-1
FEC Engine
DSP-to-Peripheral Bridge
AHB Peripheral 1
AHB Peripheral n
AHB
AHB-to-APB Bridge
APB
APB Peripheral 1
APB Peripheral n
24
16
22
14
38
36
34

FIG. 2

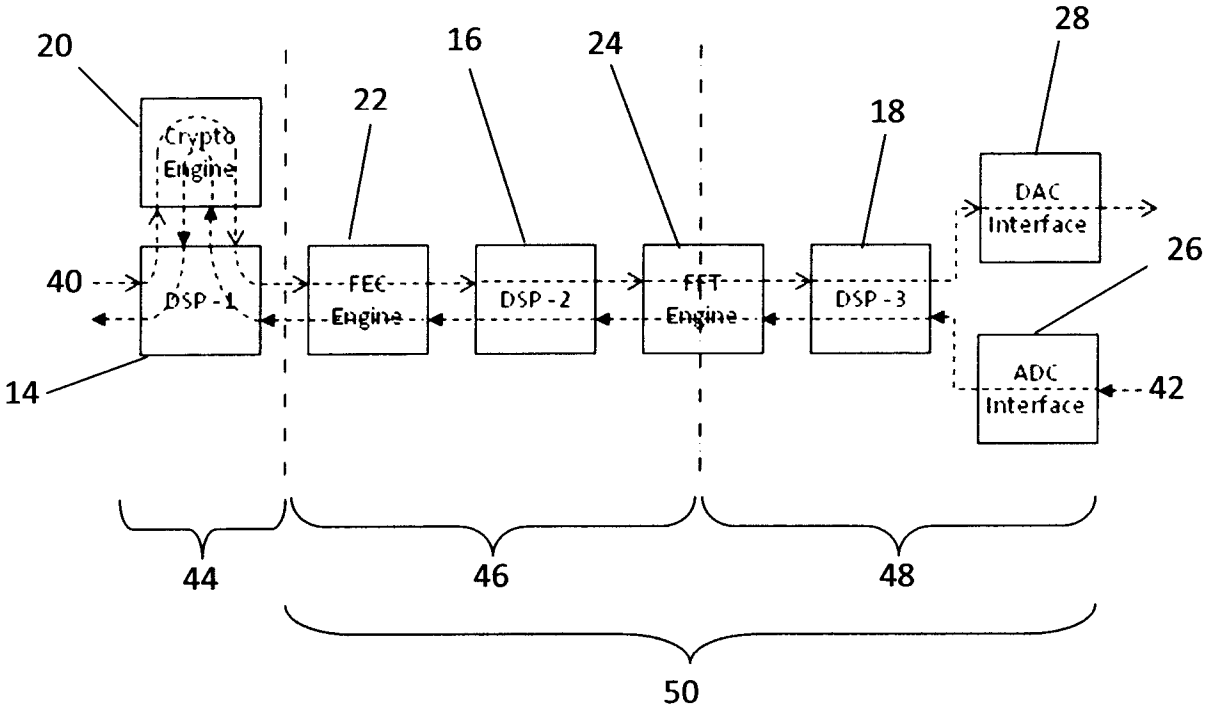
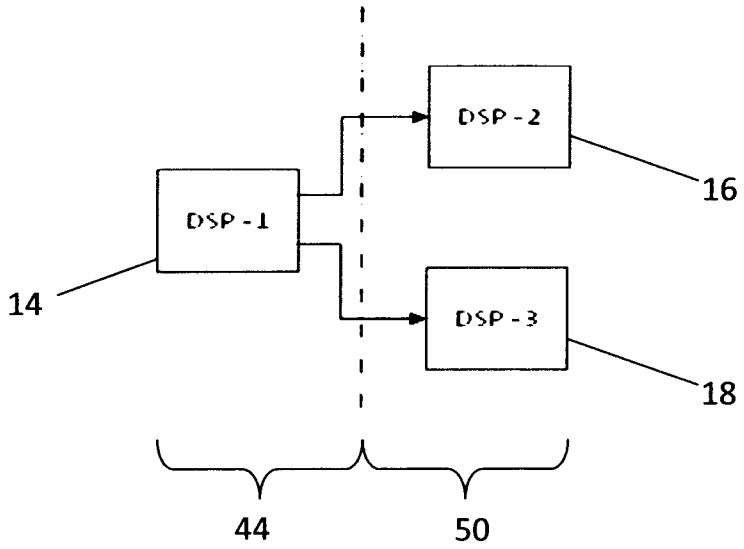

20
Crypto Engine
22
16
24
18
28
DAC Interface
26
40
DSP - 1
FEC Engine
DSP - 2
FFT Engine
DSP - 3
14
ADC Interface
42
44
46
48
50

FIG. 3



INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2011/000113

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H04L 25/00 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPODOC and WPI, Google, Google Scholar, Google Patents, www.freepatentsonline.com, ESPACE: system on chip, SOC, baseband, processing, digital, signal, MAC, bridge and other similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0021871 A1 (GEORGIUO et al) 27 January 2005 (see, for example, the abstract and paragraph [0042], [0046], figures 6-7)	1
X	Texas Instruments - TMS320TCI6488 W-CDMA DSP SoC [Retrieved 20 September 2011] Retrieved from the Internet <URL: http://www.ti.com/lit/wp/spraam8/spraam8.pdf> published May 2007 as per second page (see, for example, figure 1 and section 'Introduction to TMS320TCI6488' and page 17 lines 1-2)	1

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 October 2011	11/10/2011
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **ANDREW MUNRO** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 3 9935 9620

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2011/000113

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See Supplemental Box 1

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2011/000113

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Octasic – OCT2224W Technical Product Brief [Retrieved 27 September 2011] Retrieved from the Internet <URL: http://www.octasic.com/documents/en/products/oct2200/oct2200pb2010-100_technical_brief_oct2224w.pdf> published 19 June 2010 as per document (see, for example, page 1 lines 1-2, section 'OCT2224W Block Diagram' (page 2), section 'Hardware Acceleration Blocks (HABs) (page 1), section 'Peripheral Interfaces' (page 1), 'High-performance Multi-core DSP' (page 1), 'Channel Decoder Engine (CDE)' (page 2) and section 'Parallel Interface Port – RF Interfaces' (page 4))	1-9
A	US 2007/0073953 A1 (COFFEE et al) 29 March 2007 (see, for example, the abstract)	
A	US 2005/0216702 A1 (PAOLUCCI et al) 29 September 2005 (see, for example, the abstract and figure 1)	
A	Zigbee System-On-Chip (SoC) Design [Retrieved on 29 September 2011] Retrieved from the Internet <URL: http://www.highfrequencyelectronics.com/Archives/Jan06/HFE0105_Khanh.pdf> published 2006 as per front page (see, for example, section 'SoC Design' and figure 4)	

Supplemental Box 1
(To be used when the space in any of Boxes I to IV is not sufficient)

Continuation of Box No III:

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

In assessing whether there is more than one invention claimed, I have given consideration to those features which can be considered to potentially distinguish the claimed combination of features from the prior art. Where different claims have different distinguishing features they define different inventions.

This International Searching Authority has found that there are different inventions as follows:

- Claims 1-7 are directed towards a system-on-chip for baseband processing comprising a digital-signal-processor (DSP) having at least a master processor, a peripheral subsystem and a DSP-to-peripheral bridge. It is considered that a *system-on-chip for baseband processing comprising a digital-signal-processor (DSP) having at least a master processor, a peripheral subsystem and a DSP-to-peripheral bridge* a first distinguishing feature.
- Claims 8-9 are directed towards a method transmitting/receiving a signal in a chip, comprising collecting/transmitting binary encoded air interface data from an interface, performing time domain processing for reception/transmission of MAC protocol, performing frequency domain processing for reception/transmission of MAC protocol, decrypting/encrypting the data into higher layer data units and transferring/collecting higher layer data to peripherals via DSP to peripherals bridge. It is considered that a method of method *transmitting/receiving a signal in a chip, comprising collecting/transmitting binary encoded air interface data from an interface, performing time domain processing for reception/transmission of MAC protocol, performing frequency domain processing for reception/transmission of MAC protocol, decrypting/encrypting the data into higher layer data units and transferring/collecting higher layer data to/from peripherals via DSP to peripherals bridge* comprises a second distinguishing feature.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

Each of the abovementioned groups of claims has a different distinguishing feature and they do not share any feature which could satisfy the requirement for being a special technical feature. Because there is no common special technical feature it follows that there is no technical relationship between the identified inventions. Therefore the claims do not satisfy the requirement of unity of invention a priori.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/MY2011/000113

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2005021871	CN	1910571	EP	1654669	JP	2005216283
		JP	2005044361	KR	20050013076	KR	20050012677
		KR	20060110858	US	7353362	US	2005021874
		US	7412588	US	2007239966	US	7917729
		US	2009059955	WO	2005013143		
US	2007073953	CN	101313290	US	7376777	WO	2007037930
US	2005216702	CN	101095103	EP	1728171	IT	MI20040600
		US	7437540	US	2007168908	WO	2005103922

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX