

[54] PULSE DISTRIBUTION SYSTEM

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[51] Int. Cl.² H05B 37/02

[58] Field of Search 315/176, 211, 312, 324; 340/166 C, 324 M, 339, 378 R, 347 P

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Primary Examiner—Nathan Kaufman

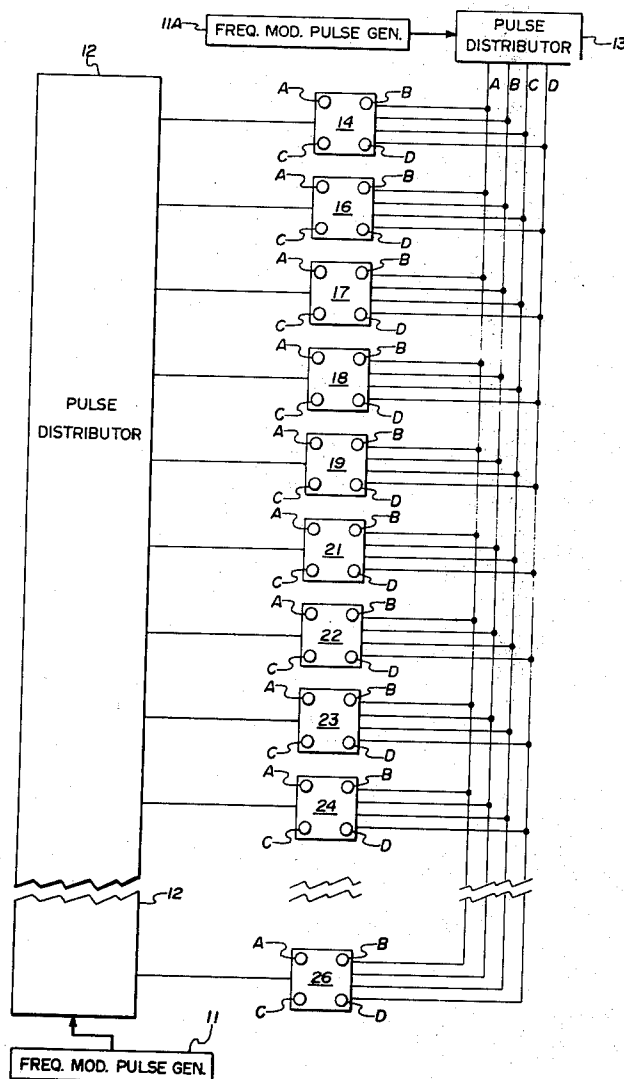
Attorney, Agent, or Firm—Richard K. Macneill

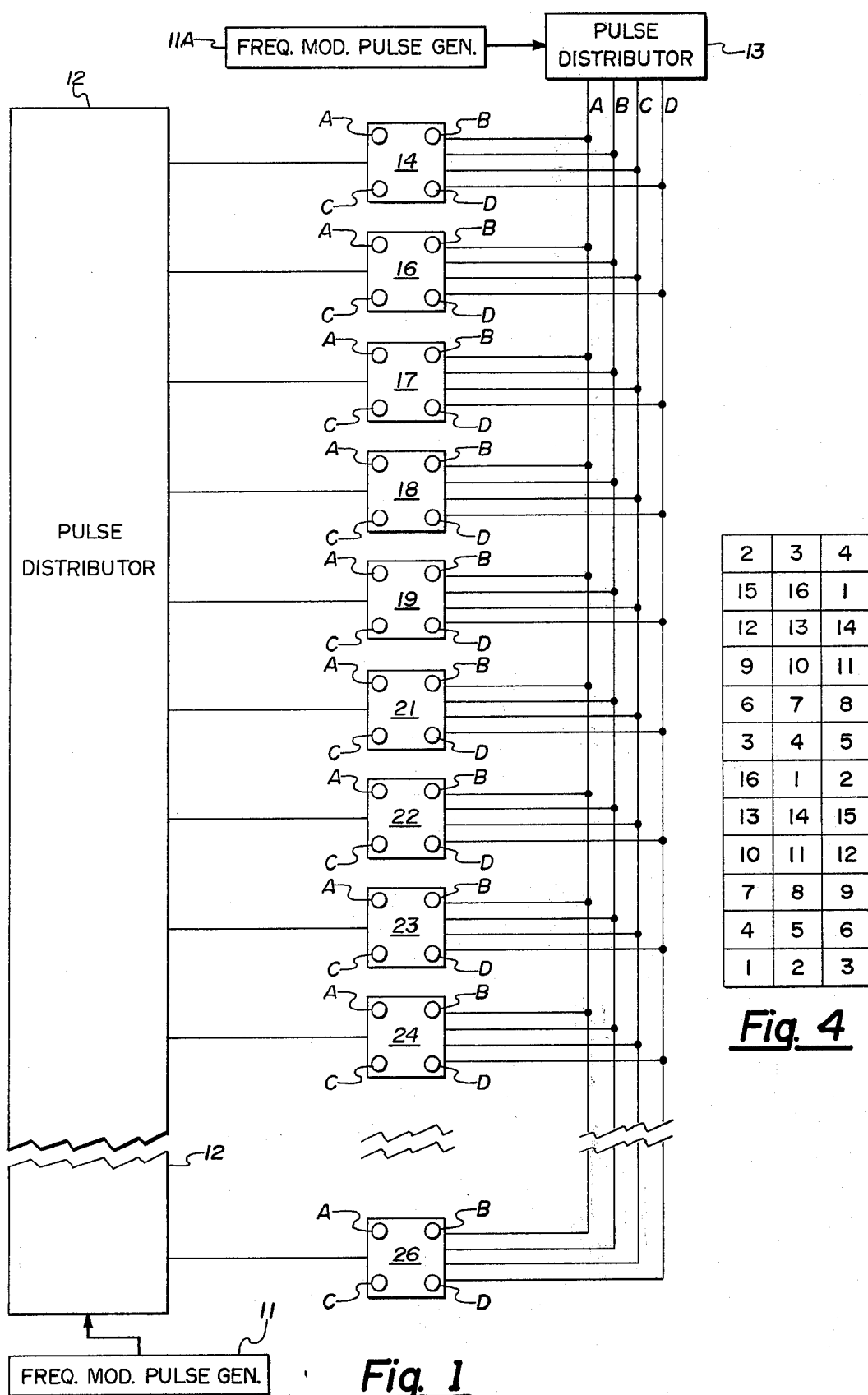
[57]

ABSTRACT

A pulse distribution system for distributing first and second chains of pulses which are being swept in frequency are passed through first and second pulse distribution logic systems, each of the outputs of the first distributor being coupled to a different cluster of multi-colored lamps to serve as an enabling pulse to all of the lamps in that cluster and the outputs of the second distributor each being coupled to a lamp of the same color in each of the clusters; the groups being placed in a series of columns and rows so that various groups are energized at different fundamental frequencies at any one of the variety of predetermined randomly selected patterns or sequences such as diagonal, horizontal, forward, backwards, left, right, and combinations of these sequences, providing a multitude of patterns.

4 Claims, 4 Drawing Figures





2	3	4
15	16	1
12	13	14
9	10	11
6	7	8
3	4	5
16	1	2
13	14	15
10	11	12
7	8	9
4	5	6
1	2	3

Fig. 4

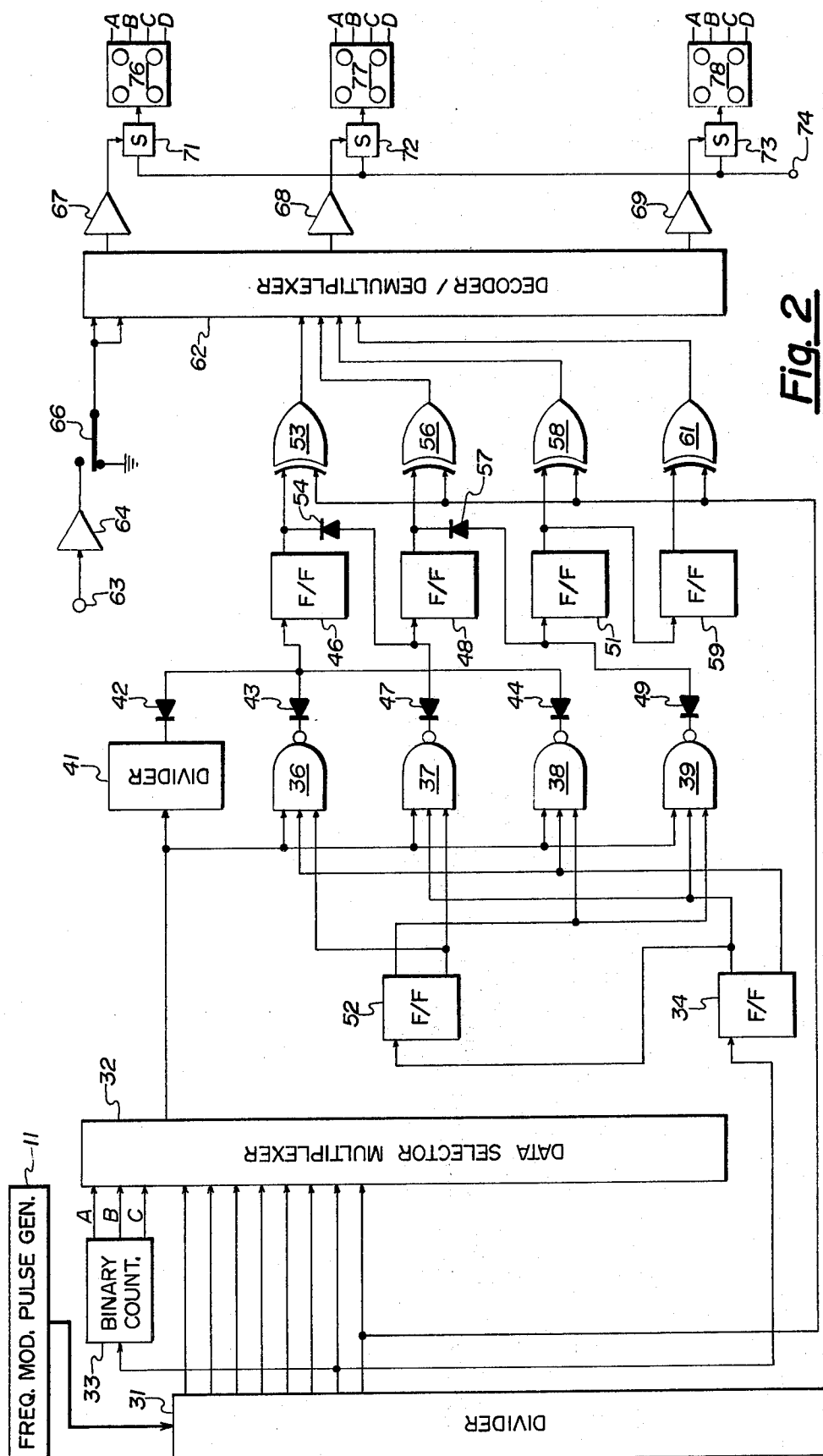


Fig. 2

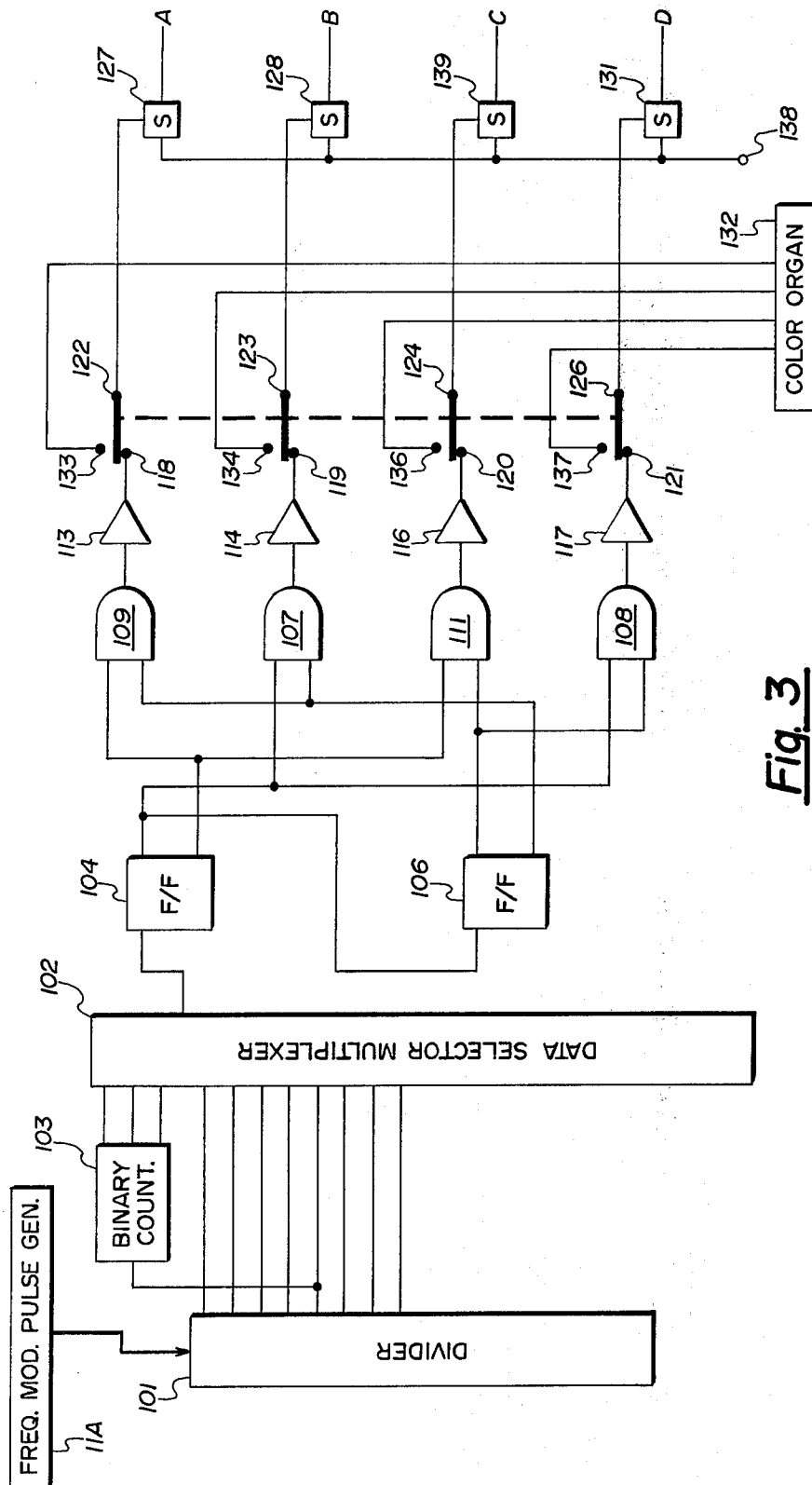


Fig. 3

PULSE DISTRIBUTION SYSTEM

PRIOR ART

The following U.S. Pat. Nos. were discovered in a preliminary patentability search:

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3,648,102 Hubertus Bettin
3,648,274 D. T. Roth et al.
3,651,319 R. H. Norris et al.
3,653,026 Frederick A. Hurley
3,717,867 W. Rosenzweig

The prior art devices of this type utilizing randomly activated light amusement devices are often found in the form of randomly flashing light bulbs. Such bulbs, when placed in a grouping, provide various patterns due to the coincidental flashing of one or more lamps occasionally giving the appearance of continuity of apparent movement. These devices are subject to the disadvantage of the limited degree of frequency of logical continuity as well as variance of pattern. Other prior art devices include light patterns changing in accordance with musical variations of recorded music. Although these patterns provide a degree of variety, their diversity is limited, and after a brief period repetition becomes obvious. Other prior art devices producing effects more dramatic than this have proven to be extremely costly and complicated.

BRIEF DESCRIPTION OF THE INVENTION

The present invention relates to a pulse distribution system and more particularly to a pulse distribution system providing a multi-colored light display.

According to the invention, a pulse distribution system for energizing a light display is provided in which literally thousands of different patterns and combinations are achieved with a surprisingly small number of components. Generally, pulse generators which are preferably swept in frequency are applied to the inputs of two pulse distributors. The first distributor has a plurality of outputs, each applied to a common lead of one cluster or group of lamps. Thus, in effect, when an output appears at any one output line of the pulse distributor, one group or cluster of lamps is enabled. Each group or cluster of lamps will have a plurality of colored lamps, each color preferably disposed in the same relative location in each group. The second pulse distributor has a plurality of outputs equal to the number of colors of lamps, and each output is connected to each lamp of one color. Hence, when any one cluster or group of lamps is enabled, whichever output line of the second pulse distributor has an output, the lamp of that corresponding color will be energized in the group that is enabled. A further feature lies in enabling the outputs of one of the distributors with music in place of a patterned common pulse input which gives the effect of synchronizing the display with music.

An object of the present invention is the provision of an improved pulse distribution system.

Another object of the invention is the provision of a pulse distribution system in combination with a lighting display device.

A further object of the invention is the provision of a lighting display device synchronized with external stimuli.

A still further object of the invention is the provision of unique lighting pattern display.

Yet another object of the invention is the provision of a lighting display device which is inexpensive to manufacture and extremely versatile in operation.

Other objects and many of the attendant advantages of the present invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings in which like reference numerals designate like parts throughout the Figures thereof and wherein:

FIG. 1 is a system block diagram of the preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram of one pulse distributor of the embodiment of FIG. 1;

FIG. 3 is a detailed block diagram of another pulse distributor of the embodiment of FIG. 1; and

FIG. 4 is a schematic representation of a typical display layout of the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Referring to FIG. 1, a frequency modulated pulse generator 11 has an output coupled to pulse distributor 12. Pulse distributor 12 has outputs coupled to load groups 14, 16, 17, 18, 19, 21, 22, 23, 24 and 26. Pulse distributor load group 14 has loads 14A, 14B, 14C and 14D. Load group 16 has loads 16A, 16B, 16C and 16D. Load group 17 has loads 17A, 17B, 17C and 17D. Load group 18 has loads 18A, 18B, 18C and 18D. Load group 19 has loads 19A, 19B, 19C and 19D. Load group 21 consists of loads 21A, 21B, 21C and 21D. Load group 22 consists of loads 22A, 22B, 22C and 22D. Load group 23 consists of loads 23A, 23B, 23C and 23D. Load group 24 consists of loads 24A, 24B, 24C and 24D. Load group 26 consists of loads 26A, 26B, 26C and 26D. Frequency modulated pulse generator 11A has an output coupled to pulse distributor 13 which has outputs A, B, C and D. Output A is coupled to loads 14A, 16A, 17A, 18A, 19A, 21A, 22A, 23A, 24A and 26A. Output B is connected to loads 14B, 16B, 17B, 18B, 19B, 21B, 22B, 23B, 24B and 26B. Output C is connected to loads 14C, 16C, 17C, 18C, 19C, 21C, 22C, 23C, 24C and 26C. Output D is connected to loads 14D, 16D, 17D, 18D, 19D, 21D, 22D, 23D, 24D and 26D.

Referring to FIG. 2, frequency modulated pulse generator 11 is coupled to divider 31 which has a plurality of outputs coupled to data selector/multiplexer 32. Data selector/multiplexer 32 can be a Texas Instruments integrated Circuit No. 74152 which is described in the *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, published by Texas Instruments, Inc., 1973, on page 294.

Divider 31 also has an output coupled to an input of binary counter 33 which has three outputs coupled to address inputs of data selector/multiplexer 32. Binary counter 33 can be Texas Instruments integrated Circuit No. 7493 which is described in *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, on page 224. Divider 31 also has an output coupled to flip-flop 34. Flip-flop 34 (and 52) can be a Texas Instruments integrated Circuit No. 7473 which is described in the *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, published by Texas Instruments, Inc., 1973, on page

76. Data selector/multiplexer 32 has an output coupled to a first input of NAND gates 36, 37, 38 and 39. Data selector/multiplexer 32 also has an output coupled to divider 41. Divider 41, NAND gate 36 and NAND gate 38 each have outputs coupled through diodes 42, 43 and 44, respectively, to the input of flip-flop 46. NAND gate 37 has an output coupled through diode 47 to an input of flip-flop 48. NAND gate 39 has an output coupled through diode 49 to an input of flip-flop 51.

$\bar{Q}$ of flip-flop 34 is connected to a second input of AND gates 36 and 38. The $\bar{Q}$ of flip-flop 34 is connected to the input of flip-flop 52 and to a second input of AND gates 37 and 39. Q of flip-flop 52 is connected to a third input of AND gates 36 and 37 and the Q is connected to the third inputs of AND gates 38 and 39. Flip-flop 46 has an output coupled to one input of exclusive OR gate 53 and through diode 54 to the input of flip-flop 48. Flip-flop 48 has an output connected to one input of exclusive OR gate 56 and through diode 57 to the input of flip-flop 51. Flip-flop 51 has an output coupled to one input of exclusive OR gate 58 and to the input of flip-flop 59. Flip-flop 59 has an output coupled to one input of exclusive OR gate 61. Divider 31 has an output connected to a second input of exclusive OR gates 53, 56, 58 and 61. The outputs of exclusive OR gates 53, 56, 58 and 61 are all coupled to a separate input of the decoder/demultiplexer 62. The decoder/demultiplexer 62 can be a Texas Instruments integrated Circuit No. 74154 which is described in the *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, published by Texas Instruments, Inc., 1973, at page 308. Sound source 63 is coupled through amplifier 64 to an enable input of decoder/demultiplexer 62 through one contact of switch 66. Another contact of switch 66 is grounded. The outputs of decoder/demultiplexer 62 are coupled through amplifiers 67, 68 and 69 to electronic switches 71, 72 and 73, respectively. One side of electronic switches 71, 72 and 73 are connected together and to terminal 74. Another side of switches 71, 72 and 73 are coupled to a common input of light boxes 76, 77 and 78, respectively. Each of light boxes 76, 77 and 78 have four other inputs labeled A, B, C and D.

Referring to FIG. 3, frequency modulated pulse generator 11A is coupled to divider 101. The outputs of divider 101 are coupled to data selector/multiplexer 102, one of which is coupled to the input of binary counter 103. Binary counter 103 can be Texas Instruments integrated Circuit No. 7493 which is described in the *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, at page 224. The three outputs of binary counter 103 are coupled to address inputs of data selector/multiplexer 102. Data selector/multiplexer 102 can also be a Texas Instruments integrated Circuit No. 74152 described in the *TTL DATA BOOK FOR DESIGN ENGINEERS*, First Edition, published by Texas, Instruments, Inc., 1973, at page 294. The output of data selector/multiplexer 102 is coupled to flip-flop 104. Flip-flop 104 has one output connected to flip-flop 106 and to the first input of AND gates 107 and 108. Flip-flop 104 has a second output connected to a first input of flip-flops 109 and 111. Flip-flop 106 has one output connected to a second input of AND gates 111 and 108. Flip-flop 106 has a second output connected to a second input of AND gates 109 and 107.

AND gates 109, 107, 111 and 108 have outputs connected to inputs of amplifiers 113, 114, 116 and 117, respectively. Amplifiers 113, 114, 116 and 117 have

outputs coupled to contacts 118, 119, 120 and 121, respectively, of switches 122, 123, 124 and 126, respectively. Switches 122, 123, 124 and 126 are coupled to a control input of electronic switches 127, 128, 129 and 131, respectively. Music organ 132 has first, second, third and fourth outputs connected to contacts 133, 134, 136 and 137, respectively, of switches 122, 123, 124 and 126, respectively. Switches 122, 123, 124 and 126 are ganged together. One side of electronic switches 127, 128, 129 and 131 are connected together and to terminal 138. Another side of electronic switches 127, 128, 129 and 131 are connected to terminals A, B, C and D, respectively.

OPERATION

Referring back to FIG. 1, frequency modulated pulse generators 11 and 11A provide the clocking sources for the entire system. Each load group is enabled by a separate output from pulse distributor 12, e.g., should an output appear at load group 22, loads 22A, 22B, 22C and 22D are energized on one side simultaneously. When an output appears on any one or more of the outputs A, B, C and D of pulse distributor 13, the corresponding load of load group 22 will then be energized due to the enabling pulse from pulse distributor 12. The sequence of energization will depend upon internal logic of pulse distributors 12 and 13 and the frequency of energization will depend upon this logic as well as the frequency of the outputs of pulse generators 11 and 11A. Hence, a double pulse distribution is effected to a plurality of loads grouped in a plurality of groups. It can be appreciated that if each load group represents four different colored light bulbs and the light bulbs of each color are identically disposed spatially in each group, then a very unique sequential lighting pattern can be effected through this varying frequency double pulse distribution system.

Referring back to FIG. 2, pulse distributor 12 (FIG. 1) will be described. It is pointed out that the only common elements are the loads which are indicated as light boxes 76, 77 and 78. All of the remaining components of FIG. 2, except pulse generator 11, can be considered to be within pulse distributor 12 of FIG. 1. The output of frequency modulated pulse generator 11 is coupled to the input of divider network 31 which can consist of a series of JK flip-flops, for example, dividing the input frequency by two any number of desired times. For the purposes of illustration, we have eight output lines from divider 31 entering data selector/multiplexer 32, with the seventh output coupled to the input of binary counter 33. Of the eight inputs connected to data selector/multiplexer 32, only one is permitted to be gated through to its output. The particular frequency selected is determined by the binary combination of binary counter 33 which is addressed to the input of data selector/multiplexer 32. Hence, the output of data selector/multiplexer 32 yields a continually changing frequency which is accomplished by virtue of the fact that data selector/multiplexer 32 sequentially selects one of eight frequencies supplied to it by divider 31 and also the result of continuous frequency modulation of pulse generator 11.

The output of data selector/multiplexer 32 is applied to the first input of four three-input NAND gates 36, 37, 38 and 39. Flip-flops 34 and 52 comprise a discrete binary counter and have four outputs connected to the remaining two inputs of the three input NAND gates 36, 37, 38 and 39, in such a way as to provide decoding

or a one of four mutually exclusive output. For example, assuming at some point in time a logical 1 appears at the lower output of flip-flops 34 and 52. Under this condition, the particular clock frequency which was selected by data selector 32 appears at the output of AND gate 36, while a static logic 1 appears at the outputs of AND gates 37, 38, and 39. (A logic of 1 in this context is defined as an off state). This condition remains until a negative going pulse arrives at the input of flip-flop 34 from divider 31, which causes a logic of 1 to appear at two of the inputs of NAND gate 37, enabling NAND gate 37, and disabling AND gate 36. Therefore, whatever frequency appears at the output of data selector 32 is gated through to the output of NAND gate 37. This sequence is continued until NAND gates 38 and 39 are sequentially enabled, whereby NAND gate 36 is again enabled and the sequence repeats.

Therefore, whatever clock frequency is selected by data selector 32 its wave form will appear at one output of NAND gates 36, 37, 38 and 39. This, in turn, determines whether the wave form appears at the input of flip-flop 46, 48 or 51. The directional feedback from the output of flip-flop 46 through diode 54 to the input of flip-flop 48 and the output of flip-flop 48 through diode 57 to the input of flip-flop 51 and the output of flip-flop 51 to the input of flip-flop 59 form a discrete binary counter. Therefore, clocking different inputs will result in changing the binary code by different increments. For example, a negatively going pulse at the input of flip-flop 46 will increase the binary count by 1. A pulse at the input of flip-flop 48 will increase the binary count by 2. Such a pulse at the input of flip-flop 51 will increase the count by four, again the diodes 54 and 57 insure that pulses can be coupled through in only one direction. As a result, a train of pulses reaching the input of flip-flop 48, for example, from NAND gate 37, through diode 47, cannot pass through diode 54. Yet when flip-flop 46 instead of flip-flop 48 is enabled, pulses from the output of flip-flop 46 can still reach the input of flip-flop 48.

The binary coded output from flip-flops 46, 48, 51 and 59 is coupled through a series of exclusive OR gates 53, 56, 58 and 61, respectively, to the input of decoder/demultiplexer 62. The outputs of decoder/demultiplexer 62 are sequential and are amplified, inverted, and passed into the control connection of electronic switches 71, 72 and 73, which in turn enable light boxes 76, 77 and 78, respectively. The other sides of these switches are coupled to an input terminal 74 which can be one side of a power line, for example. Thus, each electronic switch (which can be a silicon controlled rectifier, for example) and its respective light box, is sequentially enabled. The rate of sequence is determined by the particular frequency selection of data selector 32 and the sequence itself, i.e., the order in which the various light boxes are enabled, is determined by which NAND gate 36, 37, 38 or 39 is enabled.

The direction of lighting sequence (that is, with reference to FIG. 4, whether the count proceeds upward as 1, 2, 3, 4, 5, 6, 7, . . . , or downward as 16, 15, 14, 13, 12, 11 . . .) is determined by whether the common inputs to exclusive OR gates 53, 56, 58 and 61, from divider 31, are at a logical of 1 or 0. The sequence of count is determined by which NAND gate 36, 37, 38 or 39 is enabled. For example, if NAND gate 37 is enabled, the count sequence would proceed as (assuming 1 is enabled first) 1, 3, 5, 7, 9, 11, 13, 15, etc. If NAND

gate 39 is enabled, the count would proceed as (again assuming that 1 is enabled first) 1, 5, 9, 13, 1, 5, 9, 13, 1, 5, 9, 13, etc.) It can be observed that in both of these cases the count has a tendency to repeat. However, by the addition of divider 41, which is typically a divide by eight counter, one additional bit of information is fed into the binary counter consisting of flip-flops 46, 48, 51 and 59, for each eight pulses arriving at the input of divider 41. This has the effect of changing the count so as to reduce repetitions of count. For example, again assuming NAND gate 39 is enabled, the count would proceed as

1	5	9	13	1	5	9	13	
2	6	10	14	2	6	10	14	
3	7	11	15	3	7	11	15	etc.

The additional spontaneity of light movement by the differences in binary count can be observed by applying the above number sequence to FIG. 4. Note that an upward diagonal movement is achieved, which continually shifts upward position.

If NAND gate 37 is enabled, the count sequence would continue as

1	3	5	7	9	11	13	15	
2	4	6	8	10	12	14	16	etc.

This would result in a left upward diagonal movement, continually shifting in upward position. If flip-flop 46 is enabled, the movement is horizontal and to the right. All of these movements can appear as a forward or backward count depending on the logical state of the inputs to exclusive OR gates 53, 56, 58 and 61, from divider 31.

Sound source 63 is contemplated as a live microphone in a live music environment. When switch 66 is closed, the output from sound source 63 is amplified in amplifier 64 and applied as an enabling signal to decoder/demultiplexer 62. Hence, in this mode, the entire system will function only during an input from sound source 63, and will give a synchronizing effect with music, for example.

Referring to FIG. 3, the pulse distributor 13 of FIG. 1 will be described. Frequency modulated pulse generator 11A is coupled through a divider 101 to a data selector/multiplexer 102 and to a binary counter 103 which also has its outputs coupled to address data selector/multiplexer 102. These function in an identical manner to the divider 31, binary counter 33, and data selector 32 of FIG. 2. In this instance the output of data selector/multiplexer 102 is coupled to a discrete binary counter consisting of flip-flops 104 and 106. A binary address at the outputs of flip-flops 104 and 106 are applied to the two inputs AND gates 109, 107, 111 and 108. They are connected in a manner to provide a decoding or a one of four mutually exclusive output for AND gates 109, 107, 111 and 108. For example, the first pulse appearing at the input of flip-flop 104 is transferred to the output of AND gate 109, while AND gates 107, 111 and 108 are disabled. The second pulse appearing at the input of flip-flop 104 is transferred to the output of AND gate 107, while AND gates 109, 111 and 108 are disabled. The third pulse is transferred to the output of AND gate 111 and the fourth to the output of AND gate 108. The fifth pulse repeats to the output of AND gate 109.

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The outputs of AND gates 109, 107, 111 and 108 are amplified in amplifiers 113, 114, 116 and 117, respectively, and coupled through switches 122, 123, 124 and 126, respectively, to the inputs of electronic switches 127, 128, 129 and 131, respectively. These switches are preferably silicon controlled rectifiers. One side of electronic switches 127, 128, 129 and 131 are coupled together and to terminal 138 which can be the other side of the power supply terminal 74 in FIG. 2. The other side of electronic switches 127, 128, 129 and 131 are connected to buses A, B, C and D which are coupled to inputs A, B, C and D of light boxes 76, 77 and 78 of FIG. 2, i.e., they correspond with outputs A, B, C and D of pulse distributor 13 of FIG. 1. It can be seen, then, that through the double pulse distribution, a sequential lighting is effected with an almost infinite variety of distribution patterns and varying frequencies.

It should be understood, of course, that the foregoing invention relates to only a preferred embodiment of the disclosure, and that it is intended to cover all changes and modifications of the example of the invention herein chosen, for the purposes of the disclosure, which do not constitute departures from the spirit and scope of the invention.

The invention claimed is:

1. A pulse distributor system comprising:

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first and second pulse distributors;

first and second pulse generators coupled to an input of said first and second pulse distributors, respectively,

a plurality of lamp groups, each of said plurality of lamp groups having a plurality of individual lamps; said first pulse distributor having a plurality of outputs, each of said first pulse distributor outputs coupled to one side of each of the plurality of lamps in a separate lamp group;

said second pulse distributor having a plurality of outputs, each of said second pulse distributor plurality of outputs coupled to a single separate lamp within each of said plurality of lamp groups; and at least one of said first and second pulse generators being frequency modulated.

2. The pulse distributor system of claim 1 wherein: the lamps within each group have a plurality of colors.

3. The pulse distributor system of claim 2 wherein: each group contains lamps of the same colors as the other groups.

4. The pulse distributor system of claim 3 wherein: the groups of lamps are arranged in a series of columns for sequential lighting.

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