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[21] Appl. No. **830,464**
[22] Filed **June 4, 1969**
[45] Patented **July 27, 1971**
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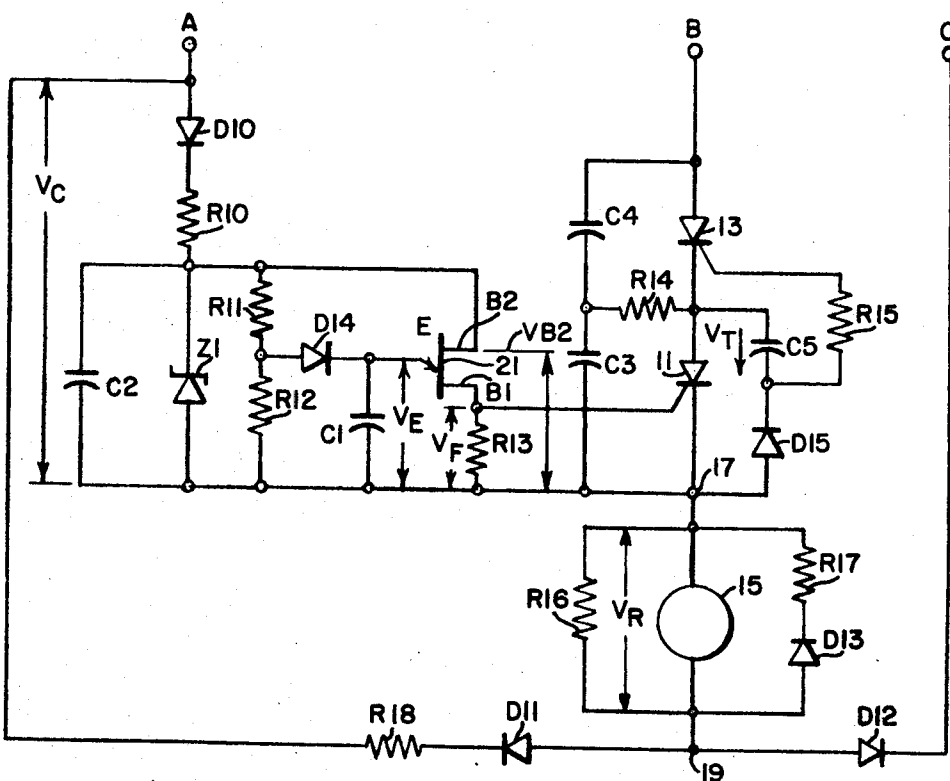
[54] **POLYPHASE CONTROL DEVICE**
4 Claims, 15 Drawing Figs.

[52] U.S. Cl. **317/47,
307/127, 317/48, 324/86, 324/87, 340/223**
[51] Int. Cl. **H02h 3/26**
[50] Field of Search **307/127;
317/48, 47; 324/86, 87; 340/253, 223**

[56] **References Cited**

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ABSTRACT: A reverse phase and single phase detecting device utilizes a silicon controlled rectifier connected with its main current path between at least two of the phases of the polyphase source to be monitored. The control electrode of the SCR receives its energization from a firing circuit connected to a third phase of the polyphase source. Under normal operating conditions the firing signal is delivered early enough in the interval when the SCR is forward biased that sufficient current is passed through the current path to operate a translating device. Under reverse phase or single phase conditions the SCR does not fire until late in the interval when the SCR is forward biased or it does not fire at all so that the detector is not activated. Preferably the firing circuit comprises a pulse generator adjusted to deliver a triggering pulse through the control electrode of the SCR at an instant which provides a greater separation in the response of the device between normal conditions and reverse or single phase conditions. A second SCR can be placed in series with the first with its control electrode receiving its firing signal from a sample and hold circuit connected across the primary SCR so that the translating device will not be operated should the primary SCR fail as a short circuit.



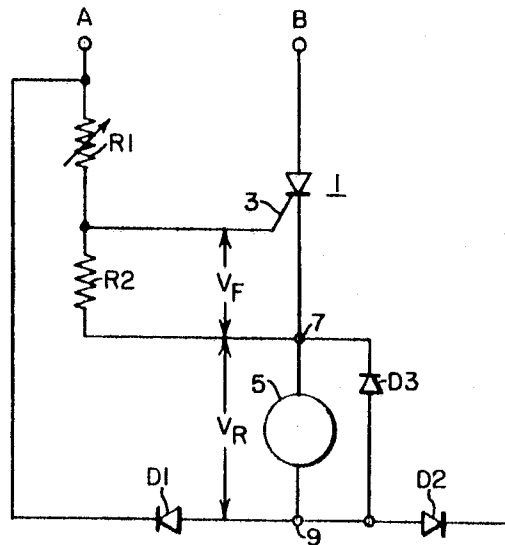


FIG. 1

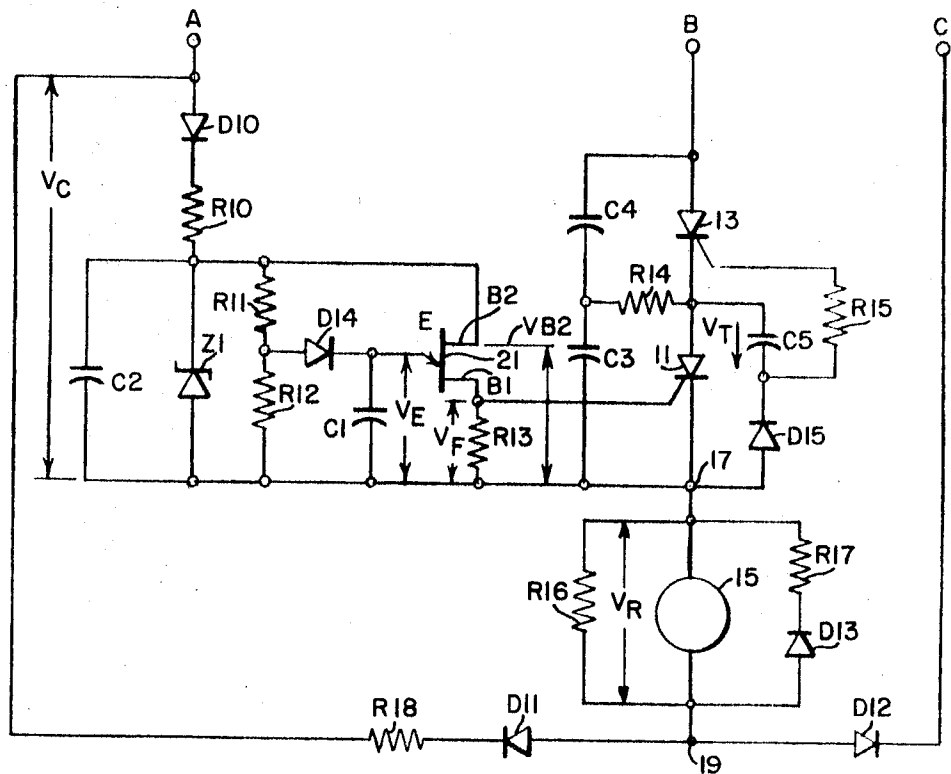


FIG. 6

FIG. 3

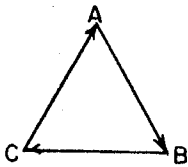
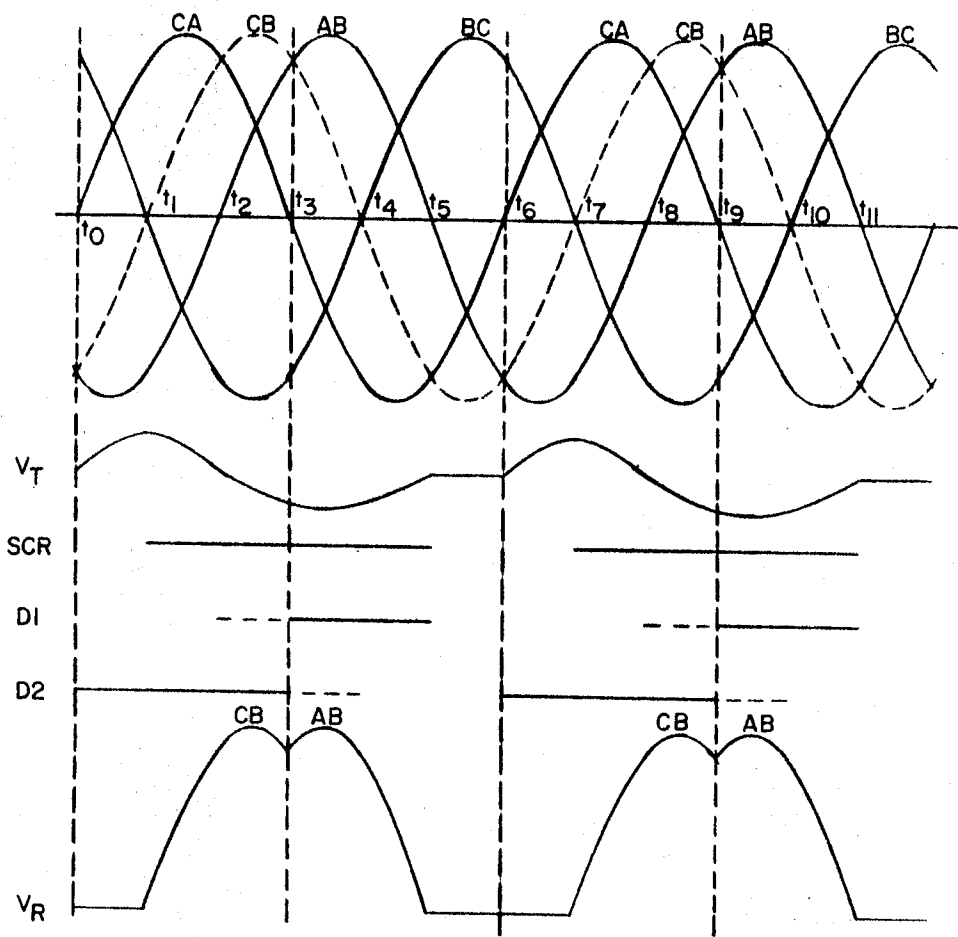


FIG. 2

FIG. 5

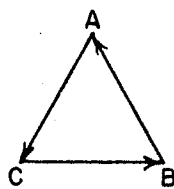
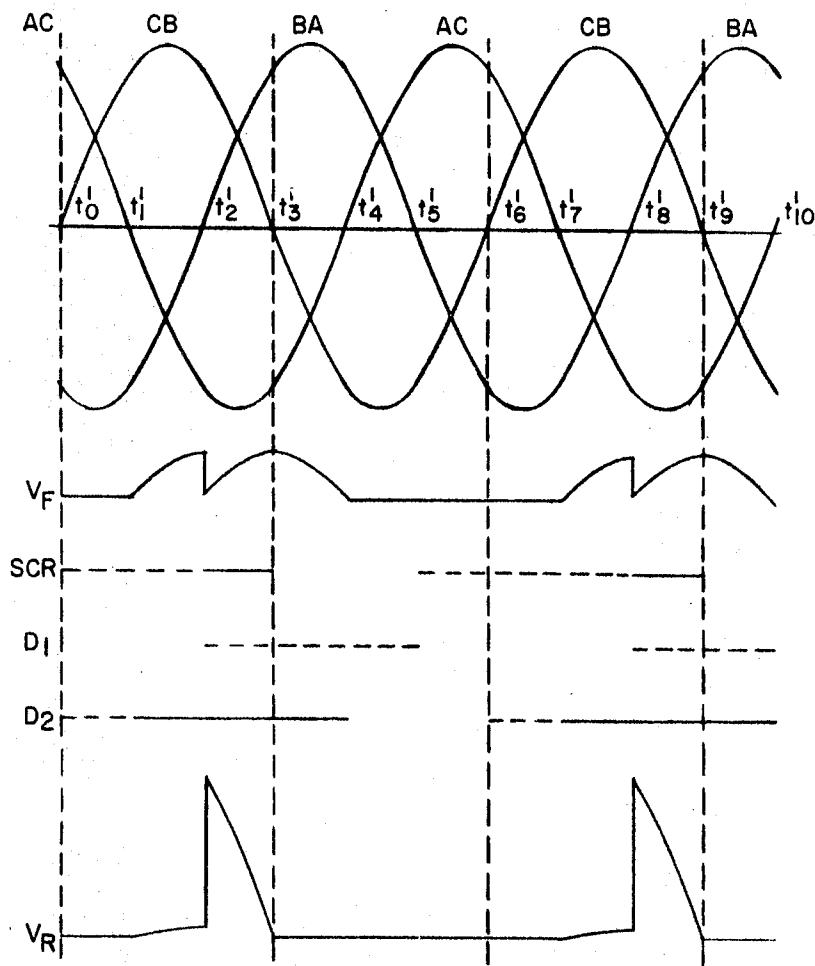


FIG. 4

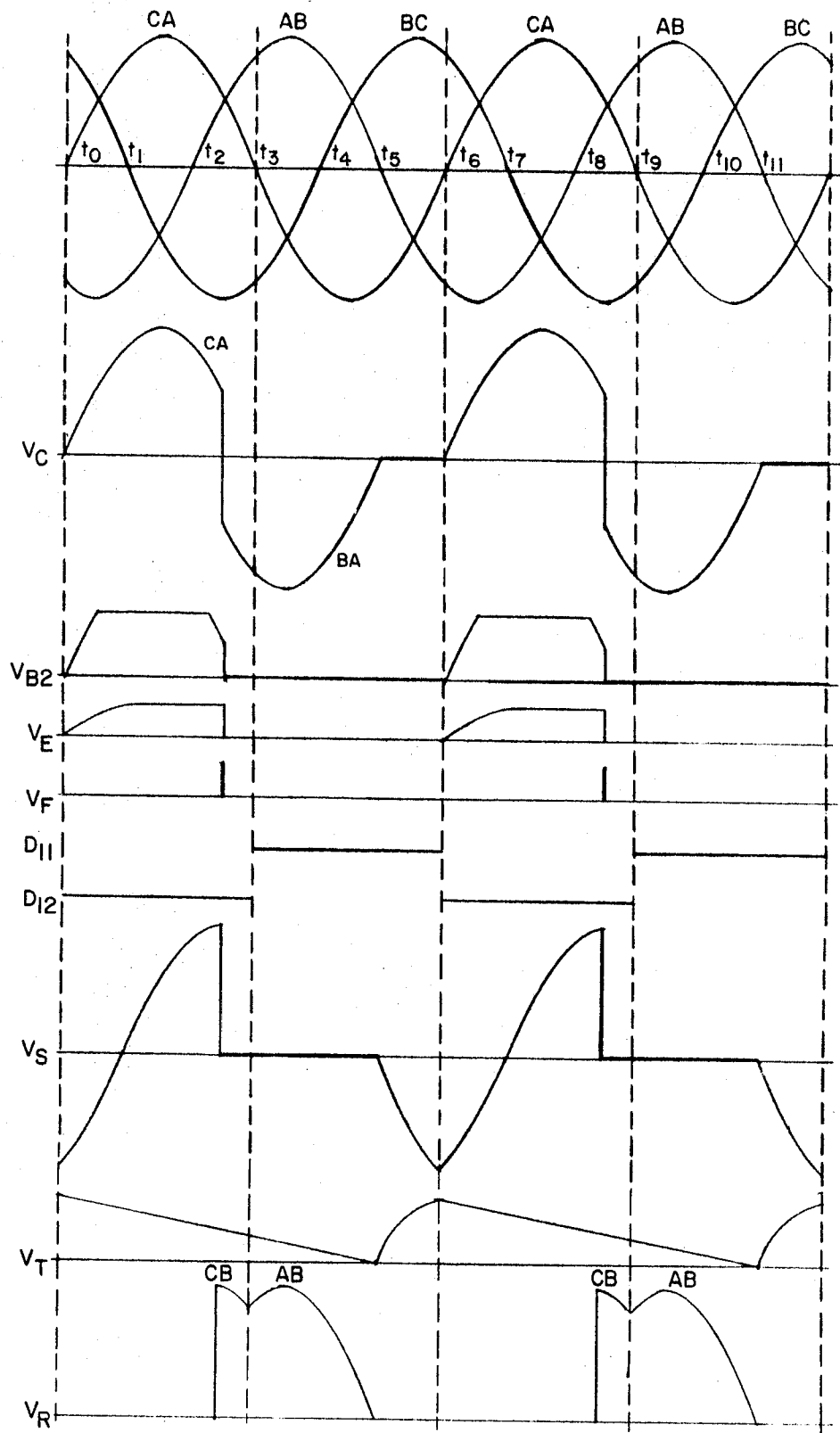


FIG. 7

FIG. 8

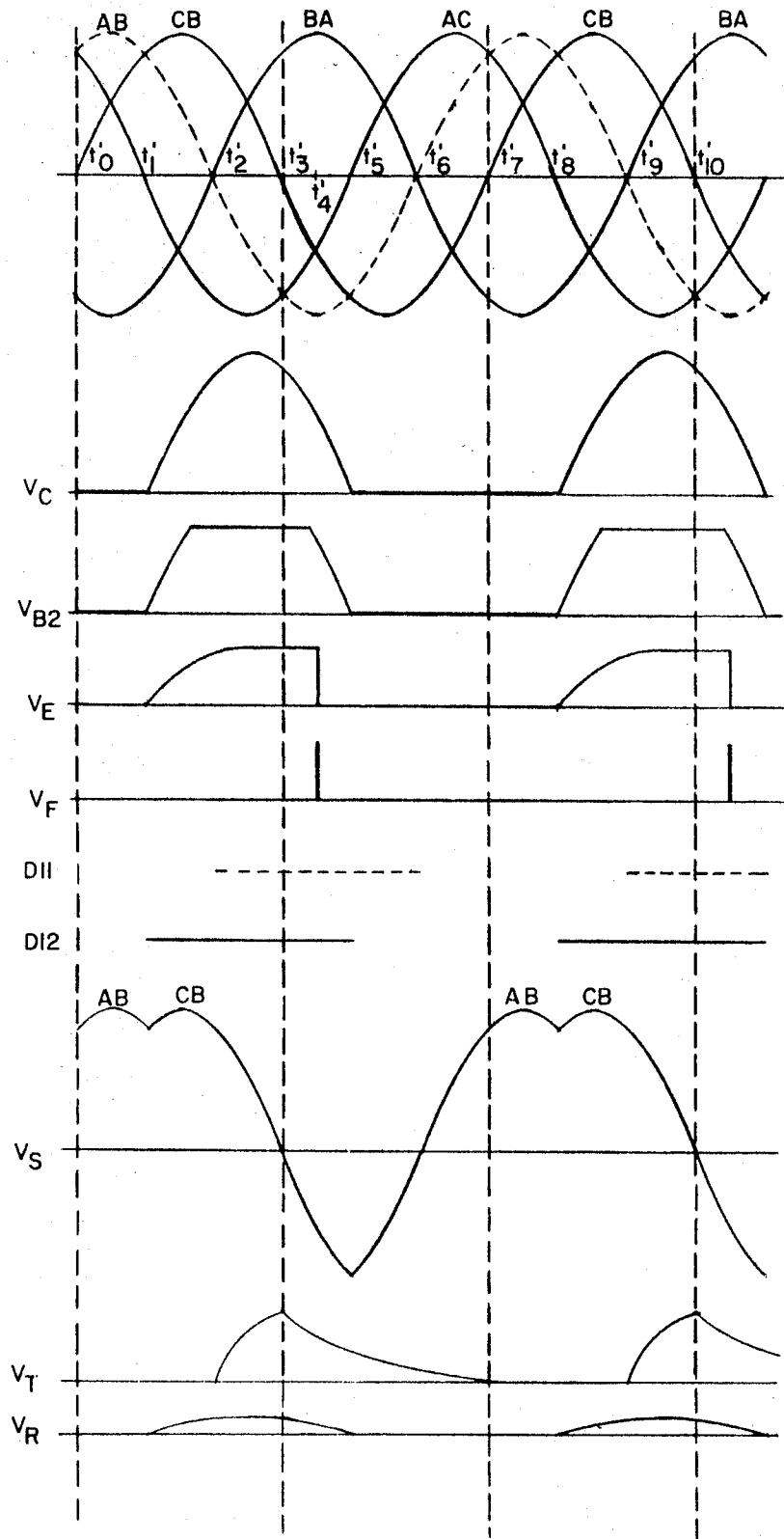


FIG. 9

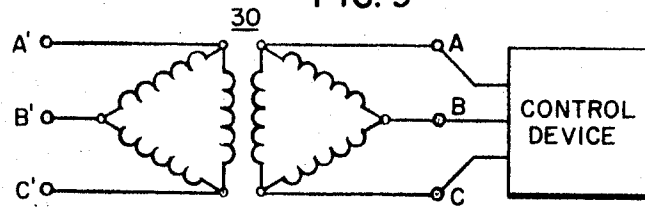


FIG. II

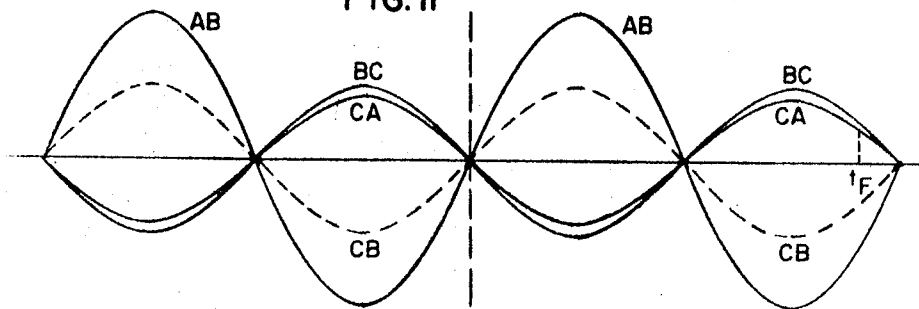


FIG. 10

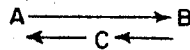


FIG. 12

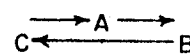


FIG. 13

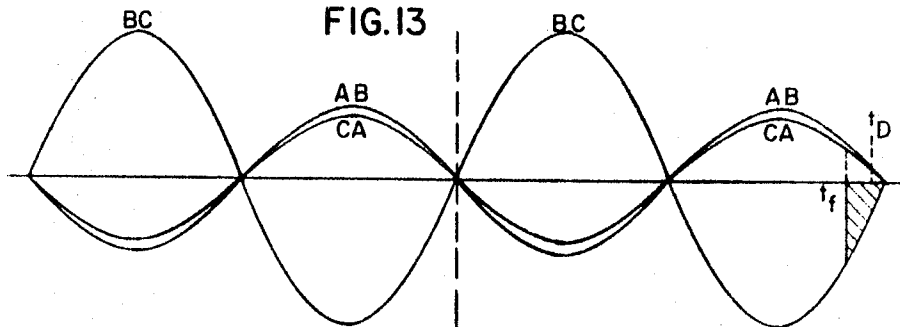


FIG. 14

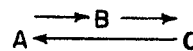
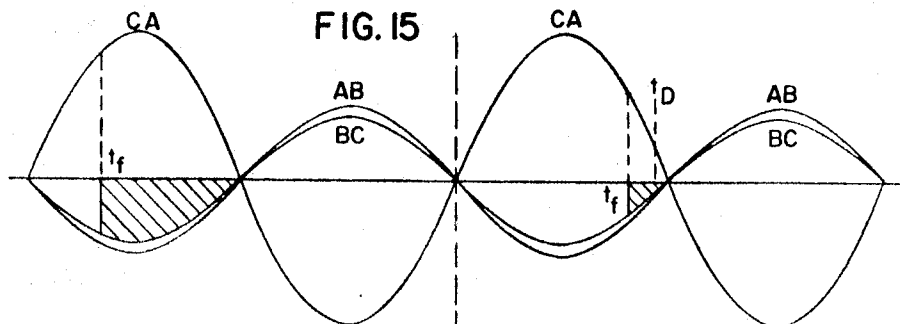


FIG. 15



POLYPHASE CONTROL DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a control device for use with a polyphase electrical system. More specifically, it relates to an improved device responsive to reverse phase and single phase conditions in such systems.

2. Prior Art

In many polyphase electrical systems the direction of phase rotation is important to the operation of the system. For instance, the direction of rotation of a polyphase induction motor is dependent upon the phase rotation of the polyphase source. If the connections to the motor are reversed the rotor will turn in the wrong direction. This can be of serious consequence where the motor is being utilized in a control system. It is of such concern in elevator systems that the elevator codes require that polyphase drive motors be protected by phase responsive devices. It is common practice today in the elevator art to utilize a small torque motor which rotates in a given direction against a spring to close contactors in the supply line when the phase rotation is correct. Such torque motor devices have been reasonably reliable but are relatively expensive and cumbersome.

Another type of reverse phase detector utilizes either an inductive or capacitive reactance to shift a signal derived from one phase of the polyphase source. This signal is vectorially added to a signal proportional to at least one other phase. The effect of cancellation or reenforcement is then utilized to operate a translating device which can include a relay connected to a reversing switch which will ensure proper phase rotation for the load device. Examples of these types of devices can be found in U.S. Pat. Nos. 3,218,485 and 3,334,273. The latter patent utilizes thermal switches connected across two phases of a three phase system which are selectively operated by the increase in current through one of the switches caused by an inductor connected across the third phase.

Also of interest in polyphase electrical systems is the detection of single phase or loss of a phase. If the open circuit occurs directly in the line being monitored it is easily detected; however, when the fault occurs on the primary side of a transformer, especially a delta wound transformer, voltages will still be detected on each phase on the secondary side of the transformer and detection is consequently more difficult. Many single phase detectors such as that disclosed in U.S. Pat. No. 3,243,796 utilize full wave rectifiers and detectors responsive to the magnitude of the ripple in the rectified voltage.

SUMMARY OF THE INVENTION

It is a primary object of the invention to provide an improved reverse phase responsive device.

It is also a primary object of the invention to provide such a device which also detects single phasing.

It is another object of the invention to provide an improved device as described in the preceding objects which when connected to the secondary side of a transformer is responsive to a loss of a phase on the primary side.

It is yet another object of the invention to provide an improved reverse phase responsive device which operates on a positive switching operation rather than relying strictly on the vectorial sum of phase shifted signals.

It is an additional object of the invention to preferably provide a device as described in the preceding objects which provides a positive switching operation only if the phase rotation is correct, maintaining an open circuit when the phase rotation is incorrect.

It is an important object of the invention to provide a device as described to varying degrees in the previous objects which is reliable, inexpensive, fast acting and compact.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the basic circuit incorporating the invention;

FIG. 2 is a vector diagram illustrating the relationship of the phase-to-phase voltages of a polyphase electrical system during normal phase rotation;

FIG. 3 is a diagram illustrating the time relationship of various signals which appear in the circuit FIG. 1 when energized by the polyphase electrical signal shown in FIG. 2;

FIG. 4 is a vector diagram illustrating the relationship of the phase-to-phase voltages during reverse phase rotation;

FIG. 5 is a diagram illustrating the time relationship of various signals appearing in the circuit of FIG. 1 when energized by the polyphase electrical signal shown in FIG. 4;

FIG. 6 is a schematic circuit diagram of the preferred embodiment of the invention;

FIG. 7 is a diagram illustrating the relationship with respect to time of various signals appearing in the circuit of FIG. 6 when energized by the electrical signal shown in FIG. 2;

FIG. 8 is a diagram illustrating the relationship with respect to time of various signals appearing in the circuit of FIG. 6 when energized by the electrical signal shown in FIG. 4;

FIG. 9 is a schematic circuit diagram of a device according to the invention connected to the secondary of a delta wound transformer whose primary is connected to a polyphase electrical source;

FIGS. 10, 12 and 14 are vector diagrams of the polyphase electrical signals appearing at the terminals A, B and C in the circuit of FIG. 9 for the loss of each phase on the primary side of the transformer; and

FIGS. 11, 13 and 15 are diagrams illustrating the relationship with respect to time of the signals applied to the control device in the circuit of FIG. 9 for the loss of phase conditions illustrated in FIGS. 10, 12 and 14 and include in the left half of the figure the response of the control device of FIG. 1 to such input voltages and in the right half the response of the circuit of FIG. 6 to such inputs.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The basic operation of the invention can best be understood by reference to the basic circuit diagram illustrated in FIG. 1. In this circuit the anode of a silicon-controlled rectifier 1 is connected to a terminal B which in turn is connected to the B phase of a three phase electrical source. The control electrode of the SCR is connected through a resistor R2 and terminal 7 to the cathode. The control electrode is also connected through a variable resistor R1 to terminal A which is connected to the A phase of the three phase electrical source. The cathode of the SCR is connected in series with the coil 5 of an electromagnetic relay which in turn is connected to the anodes of diodes D1 and D2 through a terminal 9. The cathode of diode D1 is connected to the terminal A while the cathode of diode D2 is connected to a terminal C which in turn is connected to the C phase of the three phase electrical source. The relay 5 is shunted by a diode D3 which passes current around the relay 5 in the direction opposite to that directed by the SCR and diodes D1 and D2. Since as will be seen shortly the relay 5 is energized by pulsating DC current, the diode D3 permits the reactive energy of the coil to hold the relay in when the SCR is not conducting.

To illustrate the operation of the circuit of FIG. 1, consider that three phase electrical source with a phase relationship as illustrated in the vector diagram of FIG. 2 is applied to the terminals ABC of the circuit. The relationship with respect to time between the voltages illustrated vectorially in FIG. 2 appears at the top of FIG. 3. It will be understood that for instance when the representation of the CA phase-to-phase voltage is above the reference line that the terminal A is positive with respect to the terminal C. Since it will be of more interest in considering the operation of the circuit of FIG. 1 to know when the terminal B is positive with respect to the terminal C

rather than vice versa, the dashed curve CB, which is the reverse of the BC curve, is also shown in FIG. 3.

It will be seen from FIG. 3, that at time t_0 when the CA voltage begins to go positive, a voltage V_F will be developed across the resistor R2 through the following circuit:

A, R1, R2, S, D2, C

The build up of this voltage, which serves as the triggering voltage for the silicon controlled rectifier 1, is shown diagrammatically in FIG. 3. The relative magnitudes of the signals illustrated in FIG. 3 should only be considered as representative. In reality voltage V_F remains relatively small since R2 is made small compared with the resistor R1 in order to preclude destroying the SCR by passing excessive current through the gate circuit. Representative values of R1 and R2 would be 1K and 270 ohms respectively. The current passing through the relay R during this interval is far below the pull-in current of the relay since the variable resistor R1 is very large. The solid line D2 in FIG. 3 indicates that the diode D2 is conducting during this interval.

When the voltage V_F reaches a predetermined value the SCR 1 will fire providing that its anode is positive with respect to its cathode. It can be seen from FIG. 3 however, that between the time t_0 and t_1 the anode of the SCR will be negative with respect to its cathode since both the voltage AB and CB are negative meaning that the potential at the terminal B is below that of both terminals A and C. At the time t_1 when the terminal B begins to go positive with respect to the terminal C, or in other words when the voltage CB goes positive, the SCR becomes forward biased. With the voltage V_F now above the previously mentioned predetermined value, the SCR 1 will fire thereby providing a current path for energizing the relay R. Current will begin to flow from terminal B, through SCR 1, through the relay 5 and diode D2 to terminal C. No current will flow through diode D1 at this time since with the terminal 9 essentially at the potential of the terminal C while D2 is conducting and with the terminal A above the potential of the terminal C, diode D1 is reverse biased. Since the forward drop of the SCR when conducting is essentially zero, the full potential between terminals C and B appears across the relay 5. Graphical representation of the voltage V_R developed across the relay 5 is illustrated at the bottom of FIG. 3. Since the terminal 7 is now essentially at the same potential as terminal B, the voltage V_F is derived as a function of the potential between terminals A and B as illustrated in FIG. 3.

At the time t_2 when the terminal B goes positive with respect to terminal A, the voltage V_F begins to go negative. As previously mentioned, this voltage is very small since the resistance of potentiometer R1 is very large. The diode D1 remains reverse biased however, since the potential of terminal A is still above the potential of the terminal 9 which is at the potential of terminal C. The voltage V_R therefore continues to follow the value of the voltage CB. As the voltage CB begins to decrease and the voltage AB begins to increase, at a time t_3 the potential of the terminal A goes below the potential of terminal C and diode D2 becomes cut off while diode D1 begins to conduct as shown by the solid line D1 in FIG. 3. Since the SCR remains forward biased it continues to conduct even though the potential of the control electrode is now negative. The voltage V_R now follows the value of the voltage AB. At a time t_4 the potential of terminal B goes negative with respect to the potential of terminal C, but the SCR continues to conduct since the potential of this terminal remains above that of terminal A. At time t_5 the terminal B goes negative with respect to terminal A. Since at this instant the terminal B is also negative with respect to terminal C, the SCR is reverse biased and will cease conducting.

At time t_6 when a new cycle begins, a positive triggering voltage V_F is developed across the resistor R2 as the voltage CA goes positive. However, again at this point the SCR is reverse biased and therefore the current path remains in the cutoff condition. At time t_7 when CB again goes positive the SCR will fire and current will be supplied to the relay 5. Again at time t_9 when the terminal B becomes more positive with

respect to the terminal A than with respect to the terminal C the voltage V_R begins to follow the potential AB until it too does negative at t_{11} .

The voltage V_R shown in FIG. 3 is the potential applied across terminals 9 to 7 by the alternating current source only. As the potential AB begins to fall, and during the interval between t_5 and t_7 when no external potential is being applied across the terminals 9 to 7 the collapse of the magnetic field associated with the coil of relay 5 generates a current which is shunted around the coil by the diode D3. It is this reactive energy stored in the coil which keeps the relay energized during the interval when no external potential is being applied across the terminals 9 to 7.

BASIC CIRCUIT—REVERSE PHASE

If the phase rotation of the three phase electrical signal applied to the terminals ABC is reversed, the relationship of the phase-to-phase voltage would be as shown in the vector diagram of FIG. 4. The relationship of these voltages with respect to time is displayed at the top of FIG. 5. From the previous discussion it should be clear that when the potential AC is negative the A terminal is at a higher potential than the C terminal. Likewise when the BA voltage is negative the B terminal is at a higher potential than the A terminal.

It can be seen from FIG. 5 that at t_0' that the voltage AC is positive so that the C terminal is at a higher potential than the A terminal. Under these conditions V_F will be zero since the diode D2 prevents flow of current through resistor R2. Therefore, even though at this time the SCR becomes forward biased by the voltage CB, the SCR remains in the current-blocking condition since no firing signal is being applied to its control electrode. The dashed line during this interval on the line labeled SCR in FIG. 5 indicates that the SCR is forward biased but is not conducting. At the time t_1' the A terminal begins to go positive with respect to the C terminal and the voltage V_F begins to build up across the resistor R2. The SCR, however, remains nonconducting until the time t_1' when the voltage V_F reaches the magnitude at which sufficient current flows in the gate circuit of the SCR to cause the SCR to fire. While the voltage V_F was building up it could be seen that the diode D2 was conducting. This current produced a voltage V_R as shown at the bottom of FIG. 5 across the relay 5, however, it was much less than that needed to energize the relay 5. When the SCR fires the voltage V_R across the relay 5 assumes the potential CB. At the time t_3' when the voltage CB begins to go negative, the SCR becomes reverse biased and stops conducting since the potential of terminal B is also below that of terminal A.

With the SCR conducting, the potential of the terminal 7 becomes essentially the potential of the terminal B and therefore for the interval between t_2' and t_3' the voltage V_F is determined by the voltage BA as shown in FIG. 5. At the time t_3' when the SCR stops conducting the voltage V_F is again determined by the potential between terminals A and C. At the time t_4' when the potential at the terminal C is positive with respect to that of terminal A, the voltage V_F becomes zero and remains zero until the potential of terminal A again becomes positive with respect to the terminal C at time t_7' .

At the time t_5' the SCR becomes forward biased by the potential BA. However, since voltage V_F is zero the SCR cannot be rendered conductive. Even though the potential of terminal B is above that of both terminals A and C at the time t_7' when terminal A becomes positive with respect to terminal C, the SCR cannot be fired until the time t_8' when the potential V_F reaches the firing voltage of the SCR. Again when the SCR fires the potential across the relay 5 assumes the voltage CB until the time t_9' when the SCR becomes cut off. As can be seen by comparing the waveform V_R in FIG. 5 with that of V_R in FIG. 3, even though voltage is applied to the relay 5 during part of the time while the phase rotation is reversed, the average power applied to the relay is considerably less than that applied during normal phase rotation. Although the diode

D3 will still circulate the reactive energy in the coil 5 during those intervals when the SCR is cut off, the average power applied to the relay during reverse phase conditions is insufficient to energize this relay.

The relay 5 is but one type of electroresponsive translating device which can be used as the output of the divide. The relay could be used to operate an indicator such as a light or a buzzer or it could be used to disconnect the three phase power from the load or even to reverse the leads so that the phase rotation of the three phase power supplied to the load is correct. Preferably, make contacts of the relay are used to connect the three phase source to the load. Therefore, the relay must remain picked up in order for the load to be energized.

PREFERRED EMBODIMENT: NORMAL PHASE

The basic circuit illustrated in FIG. 1 will effectively act as a reverse phase detector however, its operation is dependent upon the difference in the average power delivered to the relay during normal phase and reverse phase. The value of the potentiometer R1 is critical. It must not be too low so that too much power is supplied to the relay during reverse phase and yet it cannot be so high that the SCR cannot be fired during normal phase.

The circuit shown in FIG. 6 operates in essentially the same manner as the circuit of FIG. 1 however, its response is sharper and it is more reliable since its operation is not dependent on the critical value of the components. The current path includes two SCR's 11 and 13 connected in series with their anode towards the B terminal and their cathodes towards a junction 17. The translating means again comprises an electromagnetic relay 15 connected between the junction 17 and a junction 19. A diode D12 with its anode connected to the junction 19 connects the relay 15 with the C terminal. Similarly, a diode D11 with its anode connected to junction 19 connects the relay 15 to the terminal A through current limiting resistor R18. This resistor prevents short circuiting between terminals A and C should either the diode D11 or D12 fail. This resistor could as easily be placed between a junction 19 and the terminal C.

In the circuit of FIG. 6, the control circuit which supplies the triggering signal to the control electrode of the SCR 11 is in the form of a pulse generator. The B2 base of a unijunction transistor 21 is connected to terminal A through resistor R10 and diode D10. The base B1 of the unijunction transistor is connected to the control electrode of the SCR 11, and through resistor R13 to the junction 17. A capacitor C1 is connected between the emitter E of the unijunction transistor and the junction 17. The capacitor C1 is charged through a diode D14 by a voltage divider consisting of resistor R11 connected to the base B2 and resistor R12 connected to the junction 17. The unijunction transistor is protected by a zener diode Z1 connected between the base B2 and the junction 17. The pulse generator is also shunted by a capacitor C2 the function of which will be discussed below.

The control electrode of the SCR 13 is connected through a resistor R15 to a capacitor C5 which is also connected to the cathode of the SCR. The capacitor C5 is charged by the voltage across the SCR 11 through diode D15. The charging current is limited by the resistor R14. Capacitors C3 and C4 shunting SCR's 11 and 13 protect these SCR's from transient spikes and distributes the blocking voltage available across SCR 11 and SCR 13.

The relay 15 is shunted by a diode D13, with its anode connected to the junction 19, in series with a resistor R17. Like the diode D3 in the circuit of FIG. 1 the diode D13 permits reactive energy to hold the relay 15 in during periods when the SCR's are not conducting. The resistor R17 is provided to limit the current should the diode D13 fail.

The relay 15 is also shunted by the latch-in resistor R16. The presence of this resistor is made necessary by the fact that the current through an SCR must reach a certain minimum value in order for the SCR to remain in a conductive state

once the firing voltage is removed from the control electrode. In the circuit of FIG. 6 the inductance of the relay 15 prevents the flow of latch-in current for SCR 11 during the short interval when the firing pulse is applied to the control electrode. With the resistor R16 shunting the relay sufficient current can be passed through the SCR 11 to cause latch-in.

FIG. 7 illustrates some of the waveforms appearing at various points in the circuit of FIG. 6 when a three phase signal with normal phase rotation, as illustrated in the vector diagram of FIG. 2, is applied to the A, B and C terminals. At the top of the figure appears a diagram showing the time relationship of the potential applied to the terminals ABC. The waveform V_C is the potential appearing across the control circuit between junction 17 and terminal A. The potential V_{B2} is a potential appearing between junction 17 and the base B2 of the unijunction transistor 21 while the voltage V_E is that appearing between the junction 17 and the emitter of the unijunction transistor. The voltage V_F is the firing signal appearing across the resistor R13. The solid horizontal lines labeled D11 and D12 indicate the time intervals when the diodes D11 and D12 respectively are conducting. The waveform V_S is the voltage between junction 17 and terminal B appearing across the SCR's while the voltage V_T is the triggering voltage for the SCR 13 appearing across the capacitor C5. Again the voltage V_R is the voltage applied between the terminals 19 and 17 appearing across the relay 15.

At time t_0 when the terminal A goes positive with respect to the terminal C, diodes D10 and D12 are forward biased and the voltage V_C begins to rise as the voltage CA increases. At this time the voltage V_S across the SCR's is made negative by the fact that the terminal B is below the potential of terminal C. The potential V_{B2} rises in conformity with the voltage V_C until the breakdown voltage of the zener diode Z1. Thereafter while the voltage V_C continues to rise in conformity with the potential between the terminals A and C, the potential V_{B2} maintains a constant value as determined by the zener diode. Also beginning at t_0 , the voltage V_E across the capacitor C1 begins to build up at a rate which keeps the ratio of the potential on the emitter E of the unijunction transistor to that on the base B2 below the intrinsic standoff ratio. Under these conditions the voltage V_F across the resistor R13 remains at zero. At this time a positive charge on the capacitor C5 begins to bleed off.

At the time t_1 the potential of the terminal B begins to go positive with respect to the potential of the terminal C, however, since the triggering voltage for the SCR 11, V_F , is equal to zero, the current path through the SCR's remains in the current-blocking condition. Shortly after the time t_2 , when the potential of terminal B goes positive with respect to the potential of terminal A, the voltage CA has decreased sufficiently so that the voltage V_{B2} begins to drop below the bypass voltage of the zener diode Z1 and the potential of the base B2 of the unijunction transistor begins to decrease. In the meantime, its voltage V_E across the capacitor C1 remains essentially at its maximum value due to the blocking effect of the diode D14 and the high cutoff resistance between the emitter and the base B1 of the unijunction transistor.

When the potential of the base B2 drops sufficiently so that the ratio of the potential of the emitter E to the base B2 reaches the intrinsic standoff ratio, the unijunction transistor fires. In so doing, the effective resistance between the emitter and the base B1 of the transistor drops to a very low value so that the capacitor C1 is discharged through the relatively low value resistor R13. The discharge of the capacitor C1 is rapid so that a pulse, V_F , is applied to the control electrode of the SCR 11. Since the triggering voltage V_{T0} is still being applied by the capacitor C5 to the SCR 13 and since the terminal B is positive with respect to the terminal C both of the SCR's 11 and 13 will fire simultaneously. Although the inductance of the coil of the relay 15 will impede the immediate flow of current through the current path, sufficient latch-in current for the SCR 11 can be bypassed through the resistor R16. Therefore, even though the firing voltage V_F is a pulse of short duration the SCR 11 remains latched in.

Since the forward drop across the SCR's when they are conducting is negligible, the voltage V_S drops to essentially zero. With the junction 17 therefore at the same potential as the terminal B, the voltage V_C assumes the value of the voltage AB being applied across the AB terminals. Since the diode D10 prevents flow of current from junction 17 to terminal A the voltages V_{B2} and V_E and V_F remain equal to zero at this time.

At the time t_3 when the terminal A becomes more negative with respect to the terminal B than terminal C, diode D12 ceases to conduct and the voltage V_R assumes the value of the voltage AB as shown in FIG. 7. The SCR's will continue to conduct until time t_5 when both of the terminals A and C will be above the potential of the terminal B and the SCR's will be rendered nonconducting. At time t_5 when terminal A begins to go positive with respect to terminal B current begins to flow from the terminal A through the control circuit through diode D15, capacitor C_5 , resistor R14 and capacitor C4 to terminal B thereby charging the capacitor C5. Since capacitor C5 is relatively small, on the order of 0.01 microfarads, negligible current passes through the circuit and hence no voltage rise in V_C , V_{B2} or V_E are shown in FIG. 7. At time t_6 the sequence starts all over again.

It can be seen from the circuit of FIG. 6 that should the SCR 11 fail as a short circuit, the capacitor C5 is shorted in the interval between t_5 and t_6 so that no triggering voltage V_T can be built up across the capacitor C5. Therefore even though the SCR's become forward biased and a firing voltage is applied to SCR 11 the SCR 13 will not fire and the current path will not be transferred to its conducting condition. Should the SCR 13 fail as a short circuit firing would still be normal. If either of the SCR's should fail as an open circuit the current path could not be established and the relay would remain deenergized.

The unijunction transistor triggering circuit utilized in the circuit of FIG. 6 is a commonly used very reliable triggering circuit. It remains relatively stable despite substantial variations in the components or in line voltage. Again it should be noted that the voltage V_R illustrated in FIG. 7 is the applied voltage appearing across the terminals 19 to 17 and does not reflect the effect of the diode D13 which applies the reactive energy stored in the coil to maintain the relay in the energized condition.

The capacitor C2 across the pulse generator, in addition to assisting the zener diode in protecting the pulse generator from transient signals, also delays the response of the pulse generator to the control voltage V_C . It will be observed from the diagrams of FIG. 7 which do not incorporate the effect of the capacitor C2 for simplicity, that the parameters of the pulse generator are chosen so that the firing signal V_F is developed approximately 150° after the A terminal goes positive with respect to the C terminal. The value of the capacitor C2 can be chosen so that the response of the pulse generator is delayed until the voltage CA is closer to the 180° point. The purpose and effect of this will be discussed below in relation to the response of the system to single phasing.

PREFERRED EMBODIMENT: REVERSE PHASE

When a three phase source with phase rotation as shown in FIG. 4 is applied to the circuit of FIG. 6, the voltages across the terminals A, B and C with respect to time are as illustrated at the top of FIG. 8. The voltage AB which is positive when the terminal B is positive with respect to the terminal A is shown as a dotted line in FIG. 8 for convenience. At the time t_0 shown in FIG. 8, the terminal B is positive with respect to both the terminal A and the terminal C. However, at this time the terminal A is negative with respect to the terminal C so that the voltage V_C is held equal to zero by the diode D10. Consequently, no firing pulse V_F can be generated during this interval. Since at this time the terminal A is more negative than terminal C, the voltage V_S across the SCR's follows the voltage AB.

At the time t_1 the terminal A begins to go positive with respect to the terminal C hence the control voltage V_C begins to rise causing the voltage V_{B2} on the base B2 of the unijunc-

tion transistor and the emitter voltage V_E to both rise. Since due to the RC network connected to the emitter the voltage V_{B2} rises more rapidly than the voltage V_E , the intrinsic standoff ratio cannot be reached at this time and therefore a firing pulse cannot be generated. Also at time t_1 the terminal C becomes more negative with respect to terminal B than terminal A so that the voltage across the SCR begins to follow the voltage CB. As the pulse generator begins to charge the diode D12 conducts. By the time t_3 when CB goes negative the B terminal becomes negative with respect to both the A and C terminals.

At the time t_4 when the base two voltage of the unijunction transistor begins to decrease below the zener voltage, the ratio of the emitter voltage V_E to the base two voltage V_{B2} reaches the intrinsic standoff ratio and the unijunction transistor fires generating a firing pulse V_F across the resistor R13. Even though a firing voltage V_T which was generated across the C_5 beginning at t_2 when the voltage BA went positive is also applied to SCR 13, a current path is not completed through the SCR's since the voltage V_S is still following the voltage CB which went negative at time t_3 to reverse bias the SCR's.

At the time t_5 the terminal C begins to go positive with respect to the terminal A so that the control voltage V_C goes to zero. It cannot go negative because of the diode D10. The effect of the terminal C going positive with respect to the terminal A also causes the voltage V_S across the SCR's to begin to follow the voltage AB. With the voltage V_C equal to zero at this time all the voltages in the pulse generator go to zero. Since the firing pulse is delivered to the SCR 11 only during periods when this SCR is reverse biased, the current path is never transferred to its conducting condition. Therefore, the only current that is supplied to the relay 15 during reverse phase conditions is the very small current which produces the voltage V_R shown in FIG. 8 as the pulse generator is charged during the interval when the A terminal is positive with respect to the C terminal.

It can be seen then from FIGS. 3 and 5 and 7 and 8 that greater separation between the response to normal phase and reverse phase conditions can be obtained by the circuit of FIG. 6. There is a more positive switching operation in the case of the circuit of FIG. 6. The SCR's conduct for normal phase rotation but do not conduct at all for reverse phase conditions. On the other hand, in the circuit of FIG. 1 the SCR's will conduct under both conditions however, they conduct for a shorter length of time under reverse phase conditions.

SINGLE PHASING

The loss of a phase in a three phase system is known as single phasing. The phenomenon is given this name since, as can be seen from the vector diagram of FIG. 2, if the phase C for instance is open circuited the only vector remaining is the AB vector. Consequently the only curve that would remain in the diagram at the top of FIG. 3 would be the AB curve. Both the CA and the BC curves would be absent, hence the term single phasing.

If any one of the phases connected directly to either the terminal A, B or C in the circuit of FIG. 1 or FIG. 6 was open circuited, neither circuit would be able to pass current through its SCR's. For instance, with the A phase missing no firing voltage V_F would ever be generated and with the C phase open, SCR latch-in current would not be established when V_F was generated. On the other hand, with no B phase the SCR's could never be forward biased.

The situation is not so clear cut, however, when the device is connected to the secondary of a three phase transformer and the open circuit occurs in one of the phases on the primary side of the transformer. Although voltages will be induced in all of the secondary phases when the open circuit occurs on the primary side of a wye wound transformer, the worst case occurs when the open circuit occurs on the primary side of a delta wound transformer. Therefore, the latter case will be considered here.

FIG. 9 shows the control device according to this invention with the ABC terminals connected to the output terminals of delta wound transformer 30. A three phase source A', B', C' is connected to the primary of the delta wound transformer. FIG. 10 is a vector diagram of the phase voltages appearing at the terminals A, B and C connected to the secondary of transformer 30 when the phase C' connected to the primary of the transformer fails as an open circuit. It can be seen from FIG. 10 that the phase AB retains its normal value while the output phases B to C and C to A are exactly 180° out of phase with the voltage AB that each have a magnitude equal to one-half of the output voltage AB.

FIG. 11 illustrates the phase voltages with respect to time appearing at the terminals A, B and C of the device when the C' phase has failed as an open circuit. The response of the circuit of FIG. 1 is illustrated by the waveforms to the left of the center dot-dash line and the response of the circuit of FIG. 6 is illustrated by the waveform to the right of the centerline. It can be seen from FIG. 11 that the SCR's will not be fired since when the terminal A is positive with respect to the terminal C so that a firing voltage V_F for the SCR 1 or 11 can be generated, the SCR's are reverse biased by both the voltage AB and CB, which is 180° out of phase with BC, is shown by a dotted line in FIG. 11.

FIG. 12 is a vector diagram of the phase voltages appearing at the terminals A, B and C in FIG. 9 when the phase A' connected to the primary of the transformer 30 fails as an open circuit. Here the vector BC is normal while the voltages CA and AB are 180° out of phase and equal to one-half the magnitude of the voltage BC. The response of the circuit of FIG. 1 to such voltages as a function of time is shown in the left half of FIG. 13 while the response of the circuit of FIG. 6 with respect to time is shown in the right half of the figure. In the case of the circuit of FIG. 1 the potential between the terminals C and A will be positive while the voltage between the terminals C and B is positive to forward bias the SCR however, the voltage CA by design will not reach sufficient magnitude for the voltage V_F to reach the firing voltage of the SCR hence the SCR will remain in a nonconducting condition. In the case of the circuit of FIG. 6, however, since the firing voltage V_F is generated in response to the emitter of the unijunction transistor reaching a potential which approaches the intrinsic standoff ratio with respect to the voltage on base 2 of the transistor, a firing voltage will be developed at time t_F when the B terminal is positive with respect to the C terminal. However, since as seen in FIG. 13, this occurs very late in the cycle, the amount of power delivered to the relay and represented by the cross-hatched section is insufficient to energize the relay. Only the voltage BC, which is 180° out of phase with the voltage CB, is shown by simplicity. Hence the circuits of FIG. 1 and FIG. 6 will respond to the failure of the C' phase connected to the input of the transformer by deenergizing their relays.

FIG. 14 is a vector diagram of the phase voltages appearing at the terminals A, B and C connected to the secondary of transformer 30 when the phase B' connected to the primary fails as an open circuit. The waveforms appearing at the terminals A, B and C under these circumstances are illustrated in FIG. 15. Again the waveforms associated with the circuit of FIG. 1 are shown in the left half of FIG. 15 while those associated with the circuit of FIG. 6 are illustrated in the right half of the figure. In the circuit of FIG. 1 the SCR is forward biased by the CB voltage while the A terminal goes positive with respect to the C terminal. Therefore at the time t_F when the magnitude of the voltage CA is large enough to cause the voltage V_F to reach the firing voltage of the SCR 11, the SCR will begin to conduct. Again the voltage BC, which is 180° out of phase with CB, is shown for simplicity. Since the magnitude of the voltage CB is only one-half of the normal value the amount of power delivered to the relay will be substantially less than that necessary to hold the relay in. Since the voltage CB goes to zero before the B terminal becomes positive with respect to the A terminal conduction by the SCR ceases at the

end of the half cycle. The SCR remains cut off for the other half cycle even though the B terminal is positive with respect to the A terminal because the voltage CA is negative so that no firing voltage is developed for the SCR. In the circuit of FIG. 6 the terminal B is positive with respect to the terminal C during the interval when the voltage CA is positive. However, the firing signal V_F is not produced by the pulse generator until the voltage V_{B2} is reduced in the later part of the half cycle to the point where the ratio of the potential on the emitter of the unijunction transistor to the voltage V_{B2} reaches the intrinsic standoff ratio. This occurs at t_F and the SCR's fire however, due to the fact that conduction begins late in the half cycle and the fact that the voltage BC has only half its normal magnitude, the amount of power delivered to the SCR is very small.

The functioning of the capacitor C2 shunting the pulse generator in the circuit of FIG. 6 can now be appreciated. If the capacitor is selected so that it delays the generation of the firing pulse V_F until 170° after the voltage CA goes positive it can be seen by referring to FIGS. 13 and 15 that if the firing pulse did not occur until the time t_F that negligible power would be delivered to the relay during single phasing. It is clear then that the response of the circuit of FIG. 6 between normal conditions and reverse phase or single phase conditions is very sharp.

SUMMARY

It can be seen therefore that the device of this invention responds sequentially to conditions in the three phase source being monitored. In order for the SCR to be fired two conditions must occur: 1. the SCR must be forward biased and 2. a firing signal of sufficient magnitude and correct polarity must be applied to the control electrode. Since the main current path and the control electrode are connected to different phases of the three phase source the voltages must be produced by the three phase source in the proper sequence in order for the two conditions mentioned above to occur simultaneously. During normal phase rotation, with each phase operating properly, synchronization of the two conditions occurs at a time which permits sufficient current to flow through the SCR to operate the translating means. During reverse phase or single phase conditions the two above-mentioned conditions do not occur simultaneously or occur at an instant which permits the SCR to deliver insufficient current to the translating means to operate it. In a preferred embodiment of the invention a pulse generator is used to generate the firing signal for the SCR and its timing is so adjusted that a clear cut response between normal and abnormal conditions is achieved.

I claim as my invention:

1. In a phase-responsive device, three terminals adapted to be connected to a three-phase electrical source to produce a three-phase source of electrical power for the device, a first unidirectional electrical valve having a main current path and a control electrode for controlling the conductivity of the main current path, a current responsive translating device connected in series with said main current path of said first unidirectional electrical valve between first and second ones of said terminals, means connecting the control electrode to the third terminal to render said main current path of the first unidirectional electrical valve means conductive as long as the voltage across the main current path maintains a first polarity once the voltage at the third terminal simultaneously has a first polarity, and the improvement comprising second and third unidirectional electrical valve means connected back to back between said second and third terminals with said series connected main current path of the first unidirectional electrical valve and said translating device being connected to the second and third terminals through the common point between the second and third unidirectional electrical valves, whereby for a given phase rotation of the three phase electrical source the main current path of the first unidirectional

electrical valve will be rendered conductive to pass current through the translating device from a point in time when both the first and third phase voltages of the electrical source have said first polarity through the interval that said first terminal maintains said first polarity with respect to either the second or third terminals.

2. In a phase-responsive device, three terminals adapted to be connected to a three-phase electrical source to produce a three-phase source of electrical power for the device, a first unidirectional electrical valve having a main current path and a control electrode for controlling the conductivity of the main current path, a current responsive translating device connected in series with said main current path of said first unidirectional electrical valve between first and second ones of said terminals, means connecting a control electrode to the third terminal to render said main current path of the first unidirectional electrical valve conductive as long as the voltage across the main current path maintains a first polarity once the voltage at the third terminal simultaneously has a first polarity, and the improvement, comprising a second unidirectional electrical valve having a main current path and a control electrode for controlling the conductivity of the main current path said second unidirectional electrical valve being connected with its main current path in series with the main current path of said first unidirectional electrical valve, an energy storage device connected in parallel with the main current path of the first unidirectional electrical valve, means for charging said energy storage device by periodically applying reverse bias to the first unidirectional electrical valve and means for applying the voltage across the energy storage device to the control electrode of the second unidirectional electrical valve, whereby under normal conditions both unidirectional electrical valves will be rendered conductive to supply current to the translating device for a predetermined phase rotation, while no current will be delivered to the translating device should the first unidirectional electrical valve fail as a short circuit.

3. The device of claim 2 wherein the main current path of the second unidirectional electrical valve is connected between said first terminal and the main current path of the first unidirectional electrical valve, wherein the energy storage device connected across the main current path of the first unidirectional electrical valve is a capacitor and wherein the means for reverse-biasing the first unidirectional electrical valve comprises means connecting the voltage between the

third and first terminals across the main current path of the first unidirectional electrical valve and includes a capacitor shunting the main current path of the second unidirectional electrical valve.

4. In a phase-responsive device including 3 terminals to be connected to a 3 phase electrical source, a controlled rectifier having a main current path between an anode and a cathode and a control electrode, a current responsive translating device connected in series with said main current path of said controlled rectifier between first and second ones of said terminals, a pulse generator comprising two junctions, a source of half-wave rectified alternating current connected across said junctions, a unijunction transistor, a resistor, the base b_2 of said unijunction transistor being connected to a first one of said junctions and the base b_1 being connected to the second junction through the resistor, and a triggering circuit comprising a capacitor connected between the emitter of said unijunction transistor and said second junction, a voltage divider connected across said first and second junctions, a tap on said voltage divider being connected to the emitter of said unijunction transistor for charging said capacitor, the relative values of said voltage divider and capacitor being such that the charge on said capacitor will reach a predetermined voltage in less than 120° of phase rotation after the supply voltage goes positive but at a rate such that the instantaneous voltage on the capacitor during charging maintains the emitter to base b_2 voltage ratio below the intrinsic stand off ratio of the unijunction transistor, and a diode connected between the tap on the voltage divider and the emitter of the unijunction transistor for maintaining the charge on the capacitor until it is discharged through the resistor when the magnitude of the alternating current voltage drops to a value where the ratio of the predetermined voltage maintained on the capacitor to the instantaneous magnitude of the alternating current supply voltage equals the intrinsic stand off ratio of the unijunction transistor, means connecting said first junction of the pulse generator to said third terminal through a diode to supply positive half cycles of alternating current to the pulse generator, means connecting said second junction of the pulse generator to the cathode of the controlled rectifier and means connecting said control electrode of the controlled rectifier to the base b_1 of the unijunction transistor whereby the pulse generator will supply firing pulses to the controlled rectifier while the controlled rectifier is forward biased for a given phase rotation of the three phase electrical source.

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