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(54) Title: PHOTODEFINABLE ALIGNMENT LAYER FOR CHEMICAL ASSISTED PATTERNING

(57) Abstract: Photodefinable alignment layers for chemical assisted patterning and approaches for forming photodefinable alignment layers for chemical assisted patterning are described. An embodiment of the invention may include disposing a chemically amplified resist (CAR) material over a hardmask that includes a switch component. The CAR material may then be exposed to form exposed resist portions. The exposure may produce acid in the exposed portions of the CAR material that interact with the switch component to form modified regions of the hardmask material below the exposed resist portions.

FIG. 1E
PHOTODEFINABLE ALIGNMENT LAYER FOR CHEMICAL ASSISTED PATTERNING

TECHNICAL FIELD

Embodiments of the invention are in the field of semiconductor structures and processing and, in particular, photodefined alignment layers for chemical assisted patterning.

BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

In a first aspect, integrated circuits commonly include electrically conductive microelectronic structures, which are known in the arts as vias, to electrically connect metal lines or other interconnects above the vias to metal lines or other interconnects below the vias. Vias are typically formed by a lithographic process. Representatively, a photoresist layer may be spin coated over a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to as a via opening. Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

In the past, the sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset components, graphics chips, etc.). One measure of the size of the vias is the critical dimension of the via opening. One measure of the spacing of the vias is the via pitch. Via pitch represents the center-to-center distance between the closest adjacent vias. When patterning extremely small vias with extremely small pitches by such lithographic processes, several challenges present themselves, especially when the pitches are around 70 nanometers (nm) or less and/or when the critical dimensions of the via openings are around 35nm or less.

One such challenge is that the overlay between the vias and the overlying interconnects, and the overlay between the vias and the underlying landing interconnects, generally need to be controlled to high tolerances on the order of a quarter of the via pitch. As via pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than
lithographic equipment is able to keep up. Another such challenge is that the critical dimensions of the via openings generally tend to scale faster than the resolution capabilities of the lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the via openings. However, the shrink amount tends to be limited by the minimum via pitch, as well as by the ability of the shrink process to be sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) and/or critical dimension uniformity (CDU). Yet another such challenge is that the LWR and/or CDU characteristics of photoresists generally need to improve as the critical dimensions of the via openings decrease in order to maintain the same overall fraction of the critical dimension budget. However, currently the LWR and/or CDU characteristics of most photoresists are not improving as rapidly as the critical dimensions of the via openings are decreasing. A further such challenge is that the extremely small via pitches generally tend to be below the resolution capabilities of even extreme ultraviolet (EUV) lithographic scanners. As a result, commonly two, three, or more different lithographic masks may be used, which tend to increase the costs. At some point, if pitches continue to decrease, it may not be possible, even with multiple masks, to print via openings for these extremely small pitches using EUV scanners.

Thus, improvements are needed in the area of via and related interconnect manufacturing technologies.

In a second aspect, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate or other non-planar transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and compatibility with the existing high-yielding bulk silicon substrate infrastructure. Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the semiconductor processes used to fabricate these building blocks have become overwhelming.

Thus, improvements are needed in the area of non-planar transistor manufacturing technologies.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Figures 1A-1F illustrate plan views and corresponding cross-sectional views of various operations in a method involving both EUVL and BCP lithography, in accordance with an embodiment of the present invention, wherein:
Figure 1A is a plan view and corresponding cross-sectional view taken along the a-a’ axis of the plan view illustrating a hardmask layer coated or otherwise disposed on an underlying layer or substrate;

Figure 1B is a plan view and corresponding cross-sectional view taken along the b-b’ axis of the plan view illustrating an EUVL exposed chemically amplified photoresist (CAR) material layer formed on the structure of Figure 1A;

Figure 1C is a plan view and corresponding cross-sectional view taken along the c-c’ axis of the plan view illustrating the structure of Figure 1B following an anneal process;

Figure 1D is a plan view and corresponding cross-sectional view taken along the d-d’ axis of the plan view illustrating the structure of Figure 1C following removal of the annealed CAR layer;

Figure 1E is a plan view and corresponding cross-sectional view taken along the e-e’ axis of the plan view illustrating the structure of Figure 1D following coating and annealing of a block co-polymer (BCP) material; and

Figure 1F is a plan view and corresponding cross-sectional view taken along the f-f axis of the plan view illustrating the structure of Figure 1E following removal of a portion of the BCP material and patterning of the hardmask layer to provide a patterned hardmask layer.

Figures 2A-2E illustrate plan views and corresponding cross-sectional views of various operations in a method involving both EUVL and BCP lithography, in accordance with an embodiment of the present invention, wherein:

Figure 2A is a plan view and corresponding cross-sectional view taken along the a-a’ axis of the plan view illustrating a hardmask layer coated or otherwise disposed on an underlying layer or substrate;

Figure 2B is a plan view and corresponding cross-sectional view taken along the b-b’ axis of the plan view illustrating an EUVL chemically amplified photoresist (CAR) material layer formed on the structure of Figure 2A;

Figure 2C is a plan view and corresponding cross-sectional view taken along the c-c’ axis of the plan view illustrating the structure of Figure 2C following removal of the exposed portions of the CAR layer and a surface treatment of the exposed portions of the hardmask layer;

Figure 2D is a plan view and corresponding cross-sectional view taken along the d-d’ axis of the plan view illustrating the structure of Figure 2C following coating and annealing of a block co-polymer (BCP) material; and

Figure 2E is a plan view and corresponding cross-sectional view taken along the e-e’ axis of the plan view illustrating the structure of Figure 2D following removal of a portion of the BCP material and patterning of the hardmask layer to provide a patterned hardmask layer.
Figures 3, 4 and 5 illustrate various operations in a method involving use of a photoactive film that includes either poly-styrene or PMMA brush with a photoacid generator (PAG), in accordance with an embodiment of the present invention.

Figures 6A-6L illustrate portions of integrated circuit layers representing various operations in a method of self-aligned via and metal patterning, in accordance with an embodiment of the present invention, where:

Figure 6A illustrates a plan view and corresponding cross-sectional views of options for a previous layer metallization structure;

Figure 6B illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6A following formation of interlayer dielectric (ILD) lines above the structure of Figure 6A;

Figure 6C illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6B following selective differentiation of all the potential via locations from all of the plug locations;

Figure 6D1 illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6C following differential polymer addition to the exposed portions of underlying metal and ILD lines of Figure 6C;

Figure 6D2 illustrates a cross-sectional view of the structure of Figure 6B following selective material deposition on the exposed portions of underlying metal and ILD lines, in accordance with another embodiment of the present invention;

Figure 6E illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6D1 following removal of one species of polymer;

Figure 6F illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6E following formation of an ILD material in the locations opened upon removal of the one species of polymer;

Figure 6G illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6F following via patterning;

Figure 6H illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6G following via formation;

Figure 6I illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6H following removal of the second species of polymer and replacement with an ILD material;

Figure 6J illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6I following patterning of a resist or mask in selected plug locations;
Figure 6K illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6J following hardmask removal and ILD layer recessing;

Figure 6L illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6K following metal line formation.

Figure 7A illustrates a cross-sectional view of a non-planar semiconductor device with one or more features patterned using a processing scheme involving a patterned hardmask layer formed through photodefinable alignment, in accordance with an embodiment of the present invention.

Figure 7B illustrates a plan view taken along the a-a’ axis of the semiconductor device of Figure 7A, in accordance with an embodiment of the present invention.

Figure 8 illustrates a computing device in accordance with one implementation of the invention.

Figure 9 illustrates an interposer that may be formed in accordance with one implementation of the invention.

DESCRIPTION OF THE EMBODIMENTS

Photodefinable alignment layers for chemical assisted patterning and approaches for forming photodefinable alignment layers for chemical assisted patterning are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

One or more embodiments described herein are directed to fabrication and application of a photodefinable alignment layer for chemical assisted patterning. Some embodiments are particularly suited to generating 10-50 nanometer pitch patterns, e.g., for critical dimension layers. Photodefinable alignment layers described herein may provide advantages in the field of advanced photoresists. Embodiments described herein may enable continued dimensional scaling at reduced cost compared with the incumbent technology.

To provide context, high resolution extreme ultraviolet lithography (EUV or EUVL) tools have demonstrated an ability to pattern to sub-16 nanometer dimensions. The primary path for patterning at such dimensions is through the continued use of chemically amplified resists
CARs). However, current commercial-grade CARs are limited by both pattern collapse and resolution (e.g., due to aspect ratio, material modulus, dissolution properties and diffusion lengths greater than approximately 8 nanometers). Meanwhile, directed self-assembly (DSA) has shown success, but only on pre-patterns that are challenging and expensive to manufacture (e.g., for applications involving Ebeam writer prepatterns or patterns generated by multiple processing operations).

In accordance with one or more embodiments described herein, the capabilities of EUVL are exploited to form directed, dense pre-patterns. EUVL exposure is further utilized to provide selective top surface modification upon removal of such pre-patterns. When coupled with the natural tendency of block copolymers (BCPs) to micro-phase separate, patterning features are advantageously miniaturized to an extent beyond that possible with either technique independently. Combination of the EUVL approach and an approach involving phase separating BCPs can be implemented to overcome associated disadvantages of either technique applied individually. Namely, EUVL on its own may suffer from pattern collapse/pattern roughness/reduced film thickness which may be due to decreased photon absorbance and thin film effects. On the other hand, BCP alignment is random in the absence of a chemical or topographical pre-pattern.

To provide further context, current state of the art dense logic patterning relies heavily on 193nm immersion technology. Such technology is limited to a single pass minimum resolution of approximately 80 nanometer pitch due to diffraction limitations. Accordingly, it is predicted that dense patterning for future logic technologies may require up to six 193nm individual masking operations in order to realize the most demanding process layers. Due to the challenges associated with implementation of such a multi-pass patterning scheme (e.g., cost and technical), several alternatives are currently being developed. EUVL is one such technology but high volume manufacturing (HVM) readiness has been hampered by low source power and photoresist patterning limitations. For example, there is a tendency for pattern collapse and high line width roughness (LWR). The use of BCPs requires pre-patterning in order to direct the assembly and, thus, cannot be implemented solely.

In accordance with one or more embodiments of the present invention, processing approaches are described which may be implemented to overcome pattern collapse normally associated with EUVL. Pattern collapse may be avoided since the photoresist is not developed but only used to chemically modify an underlying substrate. Additionally, LWR issues are addressed since EUVL implemented herein serves only to modify surface properties prior to removal rather than for final pattern transfer. In an embodiment, very low dose, high LWR EUVL resist pre-patterning is made possible which further strengthens the approaches described
herein by improving wafer throughput and improving quality of the pre-pattern. Since EUVL can be implemented to form chemically distinct pre-patterns, facile directed assembly of the BCP is facilitated. In one embodiment, dense patterns are achieved with as few as two lithography operations (only one of which is an exposure operations) versus a previous 6-fold requirement as described above.

In a first exemplary category of approaches, an acid sensitive hardmask and under layer pairing is patterned using a chemically amplified resist without development of the resist. For example, Figures 1A-1F illustrate plan views and corresponding cross-sectional views of various operations in a method involving both EUVL and BCP lithography, in accordance with an embodiment of the present invention.

Referring to Figure 1A, a plan view and corresponding cross-sectional view taken along the a-a' axis of the plan view illustrates a hardmask layer 100 coated or otherwise disposed on an underlying layer or substrate 102. Suitable hardmask materials are described below, as are options for applicable underlying layers or substrates 102, depending on the specific application of patterning. In an embodiment, the hardmask layer 100 is a polymeric etch-resistant hard mask material formed by spin casting onto the underlying layer or substrate 102. Following spin casting, the hardmask material is annealed to facilitate solvent evaporation and film densification. Also, thermal cross-linking of the hardmask material may also occur. In an embodiment, the hardmask material includes some form of a "switch" akin to that realized in commercial chemically amplified resist. Such a chemical switch is included in order to differentially chemically transform the hardmask material or a portion of the hardmask material, e.g., from a base-insoluble to a base-soluble state (such as RCO-OR to RCO-OH) in subsequent process operations. The switch may be polymer bound or blended. The switch may be dispersed uniformly throughout a matrix of the hardmask material or may be surface self-segregating due to a change in free energy at the surface of the spun cast material. The switch material or component of the hardmask material may additionally be anchored to the hardmask layer via a subsequent coating operation or included in a subsequently formed resist polymer formed on the hardmask material. The chemical switch need not be chemically amplified and can be additive (e.g., protonation or oxidation) or subtractive (e.g., ester hydrolysis).

Referring to Figure 1B, a plan view and corresponding cross-sectional view taken along the b-b' axis of the plan view illustrates a chemically amplified photoresist (CAR) material layer 104 that is formed on the structure of Figure 1A. In an embodiment, the chemically amplified photoresist material layer 104 is spin cast onto the annealed hardmask layer 100. EUVL exposure is then performed to provide exposure lines 106 in the CAR layer 104. However, the CAR layer 104 is not developed. It is to be appreciated that exposure of the CAR layer 104 to
incident actinic photons generates copious amounts of catalytic acid which reacts with the polymer of the CAR 104 to facilitate a deprotection reaction. In one such embodiment, a significantly greater amount of acid is generated in the exposed region compared to the unexposed region.

Referring to Figure 1C, a plan view and corresponding cross-sectional view taken along the c-c’ axis of the plan view illustrates the structure of Figure 1B following an anneal process. In an embodiment, annealing the exposed CAR layer 104 of Figure 1B causes the generated acid in the exposure lines 106 to interact with the top surface of the hardmask layer 100 to locally modify the surface properties of the hardmask layer 100, forming modified regions 108 therein. The modified regions 108 correspond to the exposure image 106. Following the anneal, the image 106 actually may be a slightly broadened latent image 106' as a result of the anneal and corresponding migration of the acid generated in the CAR layer 104 (now designated as layer 104' to represent annealed CAR layer).

Referring to Figure 1D, a plan view and corresponding cross-sectional view taken along the d-d’ axis of the plan view illustrates the structure of Figure 1C following removal of the annealed CAR layer 104’, including the annealed exposure lines 106’. Stripping of the unexposed annelid CAR layer 104’ and the annealed exposure lines 106’ leaves the hardmask layer 100 having modified regions 108 therein which correspond to the original EUVL patterning.

In an embodiment, the imaged and annealed CAR layer 104’ is removed by a solvent process that does not appreciably alter the difference in acidic surface chemistry between the modified 108 and unmodified region of the hardmask layer 100. Maintaining the difference in acidic surface chemistry ensures that a subsequently formed BCP layer is able to adequately segregate. In one such embodiment, the solvent is a polar aprotic solvent such as, but not limited to, acetone, dimethylformamide (DMF), or dimethyl sulfoxide (DMSO). According to another embodiment, two or more solvents may be used to remove the annealed CAR layer 104’. In such embodiments, a first solvent may be a "stripping solution" that might be acidic or basic in character and either aqueous based or solvent based. For example, an aqueous-based stripping solution may be TMAH in water, and a solvent-based stripping solution may be TMAH in a polar aprotic media, such as acetone, DMF, or DMSO.

Referring to Figure 1E, a plan view and corresponding cross-sectional view taken along the e-e’ axis of the plan view illustrates the structure of Figure 1D following coating and annealing of a block co-polymer (BCP) material 110. In an embodiment, the BCP material is spin cast onto the chemically pre-patterned hardmask layer 100 (which includes modified regions 108). Polarity of the pre-pattern 108 directs the BCP according to chemical similarity, providing
first polymer regions 112 and second polymer regions 114 having an alternating pattern
corresponding to the pattern of the modified regions 108. In an exemplary embodiment, for the
case of polystyrene-b-polymethylmethacrylate (PS-b-PMMA), the PMMA portion is driven
towards polar regions while the converse is true for the PS portion. In one embodiment, pattern
multiplication is also possible based on judicious use of the pre-pattern such that PMMA may
align directly with less than a 1:1 relationship with the pre-patterned hard mask yet still maintain
the periodic geometry due to its natural tendency to micro-phase separate according to product of
chi*N. By way of example, the degree of pattern multiplication may be modified by modulating
the length of the polymers in the BCP.

While PS-b-PMMA is described as an exemplary embodiment, it is to be appreciated that
many different materials, such as diblock copolymers, triblock copolymers (e.g., ABA, or ABC),
or self-segregating combinations of homopolymers may be used. By way of example, and not by
way of limitation, other suitable materials that may be used according to an embodiment include
polystyrene-b-polyethylene oxide (PS-b-PEO), polystyrene-b-isoprene (PS-b-PI, Pt), 4-tert-
butylstyrene-block-methyl methacrylate (PtBS-b-PMMA), polystyrene-b-
poly(pentafluorostyrene) (PS-b-PFS), polystyrene-b-poly(acrylic acid) (PS-b-PAA), polystyrene-
b-poly-2-vinylpyridine (PS-b-P2VP), polyethylene-polydimethylsiloxane (PE-PDMS),
polystyrene-b-polylactide (PS-b-PLA)(PDLA), polystyrene-b-polydimethylsiloxane (PS-b-
PDMS), poly(ethylene phthalate)- polylactide (PEP-PLA), polystyrene-b-poly-4-vinylpyridine
(PS-b-P4VP), poly(styrene)-b-poly(hydroxystyrene) (PS-b-PHOST), or the like.

Referring to Figure IF, a plan view and corresponding cross-sectional view taken along
the f-f axis of the plan view illustrates the structure of Figure IE following removal of a portion
of the BCP material and patterning of the hardmask layer 100 to provide a patterned hardmask
layer 116. In an embodiment, since PMMA is much less etching resistant compared to PS, the
patterned BCP layer 110 of Figure IE is exposed to a wet or dry etch chemistry suitable for
selective removal of PMMA. As a result, when coupled with the nature of the underlying guide
pattern (as modified regions 108 in hardmask layer 100), directed and selective pattern transfer is
achieved to expose the modified portions 108 of the hardmask layer 100. The pattern of the
remaining trenches 118 can be transferred into the underlying hardmask layer 100 by etching of
the hardmask layer 100 to provide a patterned hardmask layer 116. The pattern of the patterned
hardmask layer 116 can then be transferred into a subsequent underlying layer or structure,
examples of which are described in greater detail below. The overlying layer 112 remaining on
the patterned hardmask layer 116 can be removed or retained for subsequent processing
operations. In either case, overall, a photodefined alignment process scheme for chemical
assisted patterning is used to fabricate a patterned hardmask, which may itself be used for subsequent patterning operations.

In a second exemplary category of approaches, a base sensitive hardmask and under layer pairing is patterned using a chemically amplified resist with development of the resist. For example, Figures 2A-2F illustrate plan views and corresponding cross-sectional views of various operations in a method involving both EUVL and BCP lithography, in accordance with an embodiment of the present invention.

Referring to Figure 2A, a plan view and corresponding cross-sectional view taken along the a-a’ axis of the plan view illustrates a hardmask layer 200 coated or otherwise disposed on an underlying layer or substrate 202. Suitable hardmask materials are described below, as are options for applicable underlying layers or substrates 202, depending on the specific application of patterning. In an embodiment, the hardmask layer 200 is a polymeric etch-resistant hard mask material formed by spin casting onto the underlying layer or substrate 202. Following spin casting, the hardmask material is annealed to facilitate solvent evaporation and film densification. Also, thermal cross-linking of the hardmask material may also occur. According to an embodiment, the hardmask layer 200 does not require a "switch" similar to the first exemplary approach described above. Instead, of relying on a "switch" within the hardmask layer 200 to produce the pre-patterning necessary, the pre-patterning according to the second exemplary category of approaches is provided during or after the development of the a CAR layer 204 that is formed above the hardmask layer 200.

Referring to Figure 2B, a plan view and corresponding cross-sectional view taken along the b-b’ axis of the plan view illustrates a chemically amplified photoresist (CAR) material layer 204 that is formed on the structure of Figure 2A. In an embodiment, the chemically amplified photoresist material layer 204 is spin cast onto the annealed hardmask layer 200. EUVL exposure is then performed followed by a post exposure bake (PEB) to provide exposure lines 206 in the CAR layer 204. It is to be appreciated that exposure of the CAR layer 204 to incident actinic photons followed by a post exposure bake can generates copious amounts of catalytic acid which reacts with the polymer of the CAR 204 to facilitate a deprotection reaction. In one such embodiment, a significantly greater amount of acid is generated in the exposed region compared to the unexposed region, which renders it developable in a subsequent developing operation.

Referring to Figure 2C, a plan view and corresponding cross-sectional view taken along the c-c’ axis of the plan view illustrates the structure of Figure 2B following removal of the exposure lines 206 with a patterning process to form openings 217 in the CAR layer 204. The patterning process may use a tetramethyl ammonium hydroxide (TMAH) development. In an embodiment, the TMAH may render a change in surface chemistry in exposed regions only to
create modified portions 208 in the hardmask layer 200 during the development process. The modified regions 208 correspond to the exposure lines 206. Since the modified regions 208 are the result of a surface treatment, the modified regions 208 may not extend into the hardmask layer 200 to the extent observed when the first exemplary process is implemented. In an embodiment, the modified regions 208 may not extend into the hardmask layer 200 at all. For example, the modified regions 208 may be formed by ligands or a brush that are present only along a top surface of the hardmask layer 200. In one such embodiment, cleavage of protected silanols leads to a switch from hydrophobic to hydrophilic (e.g., [Si]-0-SiMe$_3$ → [Si]-OH). In one embodiment, typical development of exposed resist with TMAH is performed following exposure but is followed by rinsing with water to remove all TMAH. Accordingly, in certain embodiments, stripping of the exposure leaves the hardmask layer 200 having modified regions 208 therein which correspond to the original EUVL patterning.

According to an additional embodiment, a PS or PMMA polymer brush (not shown) may be grafted to a top surface of the hardmask 200 via a base-sensitive linkage prior to resist coating, exposure and development. In such embodiments, exposure to TMAH during the development of the exposure lines 206 removes the polymer brush in exposed regions only. As such, the removal of the polymer bush results in a change in surface chemistry in exposed regions only, and therefore creates modified portions 208 in the hardmask layer 200 which correspond to the original EUVL patterning.

According to an additional embodiment, instead of relying on the TMAH to alter the hydrophobicity of the hardmask layer 200, chemical changes to exposed regions to form the modified regions 208 are effected by including a surface grafting agent in the TMAH, or by utilizing a second aqueous or alcoholic treatment immediately following the TMAH development (i.e., before drying). By way of example, and not by way of limitation, the functionalization may include functionalization via reaction of the hardmask with an inorganic acid (e.g., a phosphonic acid) or organic acid (e.g., a carboxylic acid). Additional embodiments may include the use of a gas treatment following the TMAH development. For example, the exposed surfaces may be oxidized with an ozone treatment, or an oxygen ashing process. In order to avoid undesirable solubilization of the unexposed portions of the CAR layer 204, the functionalization should be a relatively rapid process. For example, the functionalization process may be five minutes or less. In a specific embodiment, the functionalization process may be less than one minute.

According to another additional embodiment, the CAR layer 204 is a negative tone resist. In such an embodiment, the negative tone development process may be immediately followed by a surface treatment of the exposed hardmask to form modified regions 208, similar to the
embodiment described in the previous paragraph. Alternatively, a negative tone photoresist is used where a surface grafting agent is included in the organic solvent developer. In such an embodiment, the unexposed hardmask layer 200 is functionalized by the developer to form the modified regions 208, and a subsequent surface treatment may be omitted.

In an embodiment, the remaining portions of the CAR layer 204 are removed by a solvent process that does not appreciably alter the difference in the hydrophobicity between the modified regions 208 and the unmodified regions of the hardmask layer 200. Maintaining the difference in surface chemistry ensures that a subsequent formed BCP layer is able to adequately segregate. In one such embodiment, the solvent is a polar protic solvent such as, but not limited to, acetone, DMF, or DMSO. According to another embodiment, two or more solvents may be used to remove the remaining portions of the CAR layer 204.

Referring to Figure 2D, a plan view and corresponding cross-sectional view taken along the d-d' axis of the plan view illustrates the structure of Figure 2C following the removal of the remaining portions of the CAR layer 204 and the coating and annealing of a block co-polymer (BCP) material 210. In an embodiment, the BCP material is spin cast onto the chemically pre-patterned hardmask layer 200 (which includes modified regions 208). The differences in hydrophobicity of the modified regions 208 directs the BCP according to chemical similarity, providing first polymer regions 212 and second polymer regions 214 having an alternating pattern corresponding to the pattern of the modified regions 208. In an exemplary embodiment, for the case of PS-b-PMMA, the PMMA portion is driven towards modified regions while the PS portion is driven to the unmodified regions. In one embodiment, pattern multiplication is also possible based on judicious use of the pre-pattern such that PMMA may align directly with less than 1:1 pre-patterned hard mask but yet still maintain the periodic geometry due to its natural tendency to micro-phase separate according to product of chi*N. By way of example, the degree of pattern multiplication may be modified by modulating the length of the polymers in the BCP.

While PS-b-PMMA is described as an exemplary embodiment, it is to be appreciated that many different materials, such as diblock copolymers, triblock copolymers (e.g., ABA, or ABC), or self-segregating combinations of homopolymers may be used. By way of example, and not by way of limitation, other suitable materials that may be used according to an embodiment include polystyrene-b-polyethylene oxide (PS-b-PEO), polystyrene-b-isoprene (PS-b-PI, Pt), 4-tert-butylstyrene-block-methyl methacrylate (PtBS-b-PMMA), polystyrene-b-poly(pentafluorostyrene) (PS-b-PFS), polystyrene-b-poly(acrylic acid) (PS-b-PAA), polystyrene-b-poly-2-vinylpyridine (PS-b-P2VP), polyethylene-polydimethylsiloxane (PE-PDMS), polystyrene-b-poly(lactide (PS-b-PLA))(PDLA), polystyrene-b-polydimethylsiloxane (PS-b-
PDMS), poly(ethylene phthalate)- polylactide (PEP-PLA), polystyrene-b- poly-4-vinylpyridine (PS-b-P4VP), poly(styrene)-b-poly(hydroxystyrene) (PS-b-PHOST), or the like.

Referring to Figure 2E, a plan view and corresponding cross-sectional view taken along the e-e' axis of the plan view illustrates the structure of Figure 2D following removal of a portion of the BCP material and patterning of the hardmask layer 200 to provide a patterned hardmask layer 216. In an embodiment, since PMMA is much less etching resistant compared to PS, the patterned BCP layer 210 of Figure 2D is exposed to a wet or dry etch chemistry suitable for selective removal of PMMA. As a result, when coupled with the nature of the underlying guide pattern (as modified regions 208 in hardmask layer 200), directed and selective pattern transfer is achieved to expose the modified portions 208 of the hardmask layer 200. The pattern of the remaining trenches 218 can be transferred into the underlying hardmask layer 200 by etching of the hardmask layer 200 to provide a patterned hardmask layer 216. The pattern of the patterned hardmask layer 216 can then be transferred into a subsequent underlying layer or structure, examples of which are described in greater detail below. The overlying layer 212 remaining on the patterned hardmask layer 116 can be removed or retained for subsequent processing operations. In either case, overall, a photodefinable alignment process scheme for chemical assisted patterning is used to fabricate a patterned hardmask, which may itself be used for subsequent patterning operations.

In a third exemplary category of approaches, acid catalyzed attachment of polymeric material to the hardmask is performed. For example, an alternative method to preparing a pre-patterned surface for block copolymer assembly involves use of a photoactive film that includes either a poly-styrene or a PMMA brush with a photoacid generator (PAG). Upon exposure, the PAG produces an acid that catalyzes attachment of the polymer brush to the hardmask surface at lower temperature than required in the absence of an acid. Accordingly, selective exposure of the polymeric material, for example, with EUVL, allows for a pre-pattern to be formed on the hardmask surface.

In an exemplary embodiment of the third exemplary category of approaches, Figures 3, 4 and 5 illustrate various operations in a method involving use of a photoactive film that includes either poly-styrene or PMMA brush with a photoacid generator (PAG). Referring to Figure 3, a surface 300 with hydroxide (OH) ligands has a polymeric brush 302 and associated PAG 304 disposed there above. For example, the polymeric brush 302 and the PAG 304 may be incorporated into a resin (not shown) that is disposed over the surface 300. The structure of Figure 3 is exposed to EUV irradiation 306 to convert the PAG 304 to an acid 404, as is depicted in Figure 4. The structure of Figure 4 is then heated and treated with a solvent rinse 408 to provide the structure of Figure 5.
Referring to Figure 5, in an example, a polystyrene brush 502 is thus attached 504 to the surface 500. Thus, referring to Figures 3-5 collectively, an acid-catalyzed attachment of a brush to a surface may be performed. Attachment is limited to the area of the structure of Figure 3 that is exposed to the EUV irradiation 306. In one embodiment, to enhance selectivity of the attachment, either the brush polymer or surface (or both) can be designed to also be activated by the acid. Thus, acid is needed to generate reactants and catalyze the attachment reactions. Furthermore, the attachment of the brush 502 to the surface 500 may be accomplished at a lower temperature than required in the absence of the acid 404. It is to be appreciated that the strategy contemplated here is not necessarily limited to brush polymers and can be adapted for use of other surface grafting agents such as, but not limited to, phosphonic acids, carboxylic acids, etc.

In a fourth exemplary category of approaches, direct patterning of inorganic films and monolayers is performed. For example, the chemical information necessary to direct BCP assembly may be directly patterned into a surface without the need for a CAR layer. In such scenario, a highly EUV-absorbing film is required to maintain exposure dose at an acceptable limit. In one embodiment, highly absorbing transition metal nanoparticles containing organic ligands, such as hydrophobic thiols, are utilized where exposure releases ligands from metal cores leading to a switch in polarity from hydrophobic to hydrophilic in exposed areas. A similar approach may be taken using self-assembled monolayers on highly absorbing thin metal films.

In an exemplary application of a photodefiable alignment layer, one or more embodiments described herein are directed to self-aligned via and plug patterning. The self-aligned aspect of the processes described herein may be based on a directed self-assembly (DSA) mechanism, as described in greater detail below. However, it is to be understood that selective growth mechanisms may be employed in place of, or in combination with, DSA-based approaches. In an embodiment, processes described herein enable realization of self-aligned metallization processing schemes involving patterned hardmask layers formed through photodefiable alignment for back-end of line feature fabrication.

To provide context, patterning and aligning of features at less than approximately 80 nanometer pitch requires many reticles and critical alignment strategies that are extremely expensive for a semiconductor manufacturing process. Generally, embodiments described herein involve the fabrication of metal and via patterns based on the positions of an underlying layer. That is, in contrast to conventional top-down patterning approaches, a metal interconnect process is effectively reversed and built from the previous layer up. This is in contrast to a conventional approach where an interlayer dielectric (ILD) is first deposited, with a pattern for metal and via layers subsequently patterned therein. In the conventional approach, alignment to a previous layer is performed using a lithography scanner alignment system. The ILD is then etched.
More specifically, one or more embodiments are directed to an approach that employs an underlying metal as a template to build the conductive vias and non-conductive spaces or interruptions between metals (referred to as "plugs"). Vias, by definition, are used to land on a previous layer metal pattern. In this vein, embodiments described herein enable a more robust interconnect fabrication scheme since alignment by lithography equipment is no longer relied on. Such an interconnect fabrication scheme can be used to save numerous alignment/exposures, can be used to improve electrical contact (e.g., by reducing via resistance), and can be used to reduce total process operations and processing time otherwise required for patterning such features using conventional approaches.

As illustrated below, self-aligned via and metal patterning approaches described herein may include one or more of the following aspects or attributes: (a) a bottom up super-self-aligned via/metal patterning process is enabled; (b) a previous layer metal is used to direct positions of vias on the layer formed above; (c) a process that generates every possible via and metal line end position but maintains only required or desired via and metal line end positions; (d) the position and shape of vias and metal line ends are pre-formed from a previous layer pattern; (e) an intersection of metal below and above naturally forms the fully self-aligned via positions; (f) via and plugs position, size and shape are defined by a pre-existing grating lithography from underlying metal layers; (g) via and plug lithography is required only for selecting one or another and does not affect the position, shape or size of the features (e.g., LWR is irrelevant); (h) processes described herein may be characterized as an upside down dual-damascene or via/plug first approach; (i) corresponding lithography photoresist design can be simplified since greater tolerance is achieved in the selection of via and plug locations within a layer (this may be referred to as a "bucket" approach, where a photoresist is merely used to fill a plurality of generated holes, where only certain holes are subsequently selected to be maintained or deleted); (j) LWR is not critical and faster resists can be used; (k) the size of the features can be fabricated as a single shape and size, and may be applicable for electron beam direct write (EBDW) processes; and (k) via design rules are simplified and all possible vias are allowed in any geometric configuration, where the size of the vias is completely defined by the intersection of the metal above and below.

Figures 6A-6L illustrate portions of integrated circuit layers representing various operations in a method of self-aligned via and metal patterning, in accordance with an embodiment of the present invention. In each illustration at each described operation, plan views are shown on the left-hand side, and corresponding cross-sectional views are shown on the right-hand side. These views will be referred to herein as corresponding cross-sectional views and plan views.
Figure 6A illustrates a plan view and corresponding cross-sectional views of options for a previous layer metallization structure, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-section view option (a), a starting structure 600 includes a pattern of metal lines 602 and interlayer dielectric (ILD) lines 604. The starting structure 600 may be patterned in a grating-like pattern with metal lines spaced at a constant pitch and having a constant width (e.g., for a DSA embodiment, but not necessarily needed for a directed selective growth embodiment), as is depicted in Figure 6A. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach. In other embodiments, the pattern is formed using a processing scheme involving fabrication of a patterned hardmask layer formed through photodefinable alignment, as described above. Some of the lines may be associated with underlying vias, such as line 602' shown as an example in the cross-sectional views.

Referring again to Figure 6A, alternative options (b)-(f) address situations where an additional film is formed (e.g., deposited, grown, or left as an artifact remaining from a previous patterning process) on a surface of one of, or both of, the metal lines 602 and interlayer dielectric lines 604. In example (b), an additional film 606 is disposed on the interlayer dielectric lines 604. In example (c), an additional film 608 is disposed on the metal lines 602. In example, (d) an additional film 606 is disposed on the interlayer dielectric lines 604, and an additional film 608 is disposed on the metal lines 602. Furthermore, although the metal lines 602 and the interlayer dielectric lines 604 are depicted as co-planar in (a), in other embodiments, they are not co-planar. For example, in (e), the metal lines 602 protrude above the interlayer dielectric lines 604. In example, (f), the metal lines 602 are recessed below the interlayer dielectric lines 604.

Referring again to examples (b)-(d), an additional layer (e.g., layer 606 or 608) can be used as a hardmask (HM) or protection layer or be used to enable a selective growth and/or self-assembly described below in association with subsequent processing operations. Such additional layers may also be used to protect the ILD lines from further processing. In addition, selectively depositing another material over the metal lines may be beneficial for similar reasons. Referring again to examples (e) and (f), it may also be possible to recess either the ILD lines or the metal lines with any combination of protective/HM materials on either or both surfaces. Overall, there exist numerous options at this stage for preparing ultimately underlying surfaces for a selective or directed self-assembly process.

In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material, such as the material of the interlayer dielectric lines 604, is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO₂)), doped oxides of silicon,
fhiorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, interconnect material, such as the material of metal lines 602, is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect. As will be described further below, top surfaces of the lower interconnect lines may be used for self-aligned via and plug formation.

In an embodiment, as is also used throughout the present description, hardmask materials, such as layers 606 or 608 if included as a hardmask, are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

It is to be understood that the layers and materials described in association with Figure 6A are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may
also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structure depicted in Figure 6A may be fabricated on underlying lower level interconnect layers.

Figure 6B illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6A following formation of interlayer dielectric (ILD) lines 610 above the structure of Figure 6A, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a) and (c) taken along axes a-a’ and c-c’, respectively, the ILD lines 610 are formed in a grating structure perpendicular to the direction of underlying lines 604. In an embodiment, a blanket film of the material of lines 610 is deposited by chemical vapor deposition or like techniques. In an embodiment, the blanket film is then patterned using lithography and etch processing which may involve, e.g., spacer-based-quadruple-patterning (SBQP) or pitch quartering. It is to be understood that the grating pattern of lines 610 can be fabricated by numerous methods, including EUV and/or EBDW lithography, directed self-assembly, etc. In other embodiments, the grating pattern of lines 106 is formed using a processing scheme involving fabrication of a patterned hardmask layer formed through photodefnable alignment, as described above.

As will be described in greater detail below, subsequent metal layer will thus be patterned in the orthogonal direction relative to the previous metal layer since the grating of lines 610 is orthogonal to the direction of the underlying structure. In one embodiment, a single 193nm lithography mask is used with alignment/registration to the previous metal layer 602 (e.g., grating of lines 610 aligns to the previous layer 'plug' pattern in X and to the previous metal grating in Y). Referring to cross-sectional structures (b) and (d), a hardmask 612 may be formed on, or retained following patterning of, dielectric lines 610. The hardmask 612 can be used to protect lines 610 during subsequent patterning operations. As described in greater detail below, the formation of lines 610 in a grating pattern exposes regions of the previous metal lines 602 and previous ILD lines 604 (or corresponding hardmask layers on 602/604). The exposed regions correspond to all possible future via locations where metal is exposed. In one embodiment, the previous layer metal layer (e.g., lines 602) is protected, labeled, brushed, etc. at this point in the process flow.

Figure 6C illustrates a plan view and corresponding cross-sectional views of the structure of Figure B following selective differentiation all of the potential via locations from all of the plug locations, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a)-(d) taken along axes, a-a’, b-b’, c-c’ and d-d’, respectively, following formation of ILD lines 610, a surface modification layer 614 is formed on exposed regions of the underlying ILD lines 604. In an embodiment, surface modification layer
614 is a dielectric layer. In an embodiment, surface modification layer 614 is formed by a selective bottom-up growth approach. In one such embodiment, the bottom-up growth approach involves a directed self-assembly (DSA) brush coat that has one polymer component which assembles preferentially on the underlying ILD lines 604 or, alternatively, on the metal lines 602 (or on a sacrificial layer deposited or grown on the underlying metal or ILD material).

Figure 6D1 illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6C following differential polymer addition to the exposed portions of underlying metal and ILD lines of Figure 6C, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d', respectively, directed self-assembly (DSA) or selective growth on exposed portions of the underlying metal/ILD 602/604 grating is used to form intervening lines 616 with alternating polymers or alternating polymer components in between the ILD lines 610. For example, as shown, polymer 616A (or polymer component 616A) is formed on or above the exposed portions of interlayer dielectric (ILD) lines 604 of Figure 6C, while polymer 616B (or polymer component 616B) is formed on or above the exposed portions of the metal lines 602 of Figure 6C. Although polymer 616A is formed on or above the surface modification layer 614 described in association with Figure 6C (see cross-sectional views (b) and (d) of Figure 6D1), it is to be understood that, in other embodiments, the surface modification layer 614 can be omitted and the alternating polymers or alternating polymer components can instead be formed directly in the structure described in association with Figure 6B.

Referring again to Figure 6D1, in an embodiment, once the surface of the underlying structure (e.g., structure 600 of Figure 6A) has been prepared (e.g., such as the structure of Figure 6B or the structure of Figure 6C) or is used directly, a 50-50 diblock copolymer, such as polystyrene-polymethyl methacrylate (PS-PMMA), is coated on the substrate and annealed to drive self assembly, leading to the polymer 616A/polymer 616B layer 616 of Figure 6D1. In one such embodiment, with appropriate surface energy conditions, the block copolymers segregate based on the underlying material exposed between ILD lines 610. For example, in a specific embodiment, polystyrene aligns selectively to the exposed portions of underlying metal lines 602 (or corresponding metal line cap or hardmask material). Meanwhile, the polymethyl methacrylate aligns selectively to the exposed portions of ILD lines 604 (or corresponding metal line cap or hardmask material).

Thus, in an embodiment, the underlying metal and ILD grid, as exposed between ILD lines 610 is recreated in the block co-polymer (BCP, i.e., polymer 616A/ polymer 616B). This can particularly be so if the BCP pitch is commensurate with the underlying grating pitch. The polymer grid (polymer 616A/ polymer 616B) is, in one embodiment, robust against certain small
deviations from a perfect grid. For example, if small plugs effectively place an oxide or like material where a perfect grid would have metal, a perfect polymer 616A/ polymer 616B grid can still be achieved. However, since the ILD lines grating is, in one embodiment, an idealized grating structure, with no metal disruptions of the ILD backbone, it may be necessary to render the ILD surface neutral since both types of polymer (616A and 616B) will, in such an instance, be exposed to ILD like material while only one type is exposed to metal.

In an embodiment, the thickness of the coated polymer (polymer 616A/ polymer 616B) is approximately the same as, or slightly thicker than, the ultimate thickness of an ILD ultimately formed in its place. In an embodiment, as described in greater detail below, the polymer grid is formed not as an etch resist, but rather as scaffolding for ultimately growing a permanent ILD layer there around. As such, the thickness of the polymer 616 (polymer 616A/ polymer 616B) can be important since it may be used to define the ultimate thickness of a subsequently formed permanent ILD layer. That is, in one embodiment, the polymer grating shown in Figure 6D1 is eventually replaced with an ILD grating of roughly the same thickness.

In an embodiment, as mentioned above, the grid of polymer 616A/polymer 616B of Figure 6D1 is a block copolymer. In one such embodiment, the block copolymer molecule is a polymeric molecule formed of a chain of covalently bonded monomers. In a block copolymer, there are at least two different types of monomers, and these different types of monomers are primarily included within different blocks or contiguous sequences of monomers. The illustrated block copolymer molecule includes a block of polymer 616A and a block of polymer 616B. In an embodiment, the block of polymer 616A includes predominantly a chain of covalently linked monomer A (e.g., A-A-A-A-A- ...), whereas the block of polymer 616B includes predominantly a chain of covalently linked monomer B (e.g., B-B-B-B-B- ...). The monomers A and B may represent any of the different types of monomers used in block copolymers known in the arts. By way of example, the monomer A may represent monomers to form polystyrene, and the monomer B may represent monomers to form poly(methyl methacrylate) (PMMA), although the scope of the invention is not so limited. In other embodiments, there may be more than two blocks. Moreover, in other embodiments, each of the blocks may include different types of monomers (e.g., each block may itself be a copolymer). In one embodiment, the block of polymer 616A and the block of polymer 616B are covalently bonded together. The block of polymer 616A and the block of polymer 616B may be of approximately equal length, or one block may be significantly longer than the other.

Typically, the blocks of block copolymers (e.g., the block of polymer 616A and the block of polymer 616B) may each have different chemical properties. As one example, one of the blocks may be relatively more hydrophobic (e.g., water repelling) and the other may be relatively
more hydrophilic (water attracting). At least conceptually, one of the blocks may be relatively more similar to oil and the other block may be relatively more similar to water. Such differences in chemical properties between the different blocks of polymers, whether a hydrophilic-hydrophobic difference or otherwise, may cause the block copolymer molecules to self-assemble. For example, the self-assembly may be based on microphase separation of the polymer blocks. Conceptually, this may be similar to the phase separation of oil and water which are generally immiscible. Similarly, differences in hydrophilicity between the polymer blocks (e.g., one block is relatively hydrophobic and the other block is relatively hydrophilic), may cause a roughly analogous microphase separation where the different polymer blocks try to "separate" from each other due to chemical dislike for the other.

However, in an embodiment, since the polymer blocks are covalently bonded to one another, they cannot completely separate on a macroscopic scale. Rather, polymer blocks of a given type may tend to segregate or conglomerate with polymer blocks of the same type of other molecules in extremely small (e.g., nano-sized) regions or phases. The particular size and shape of the regions or microphases generally depends at least in part upon the relative lengths of the polymer blocks. In an embodiment, by way of example (as shown in Figure 6D1), in two block copolymers, if the blocks are approximately the same length, a grid-like pattern of alternating polymer 616A lines and polymer 616B lines is generated. In another embodiment (not shown), in two block copolymers, if one of the blocks is longer than the other, but not too much longer than the other, columnar structures may formed. In the columnar structures, the block copolymer molecules may align with their shorter polymer blocks microphase separated into the interior of the columns and their longer polymer blocks extending away from the columns and surrounding the columns. For example, if the block of polymer 616A were longer than the block of polymer 616B, but not too much longer, columnar structures may formed in which many block copolymer molecules align with their shorter blocks of polymer 616B forming columnar structures surrounded by a phase having the longer blocks of polymer 616A. When this occurs in an area of sufficient size, a two-dimensional array of generally hexagonally-packed columnar structures may be formed.

In an embodiment, the polymer 616A/polymer 616B grating is first applied as an unassembled block copolymer layer portion that includes a block copolymer material applied, e.g., by brush or other coating process. The unassembled aspect refers to scenarios where, at the time of deposition, the block copolymer has not yet substantially phase separated and/or self-assembled to form nanostructures. In this unassembled form, the block polymer molecules are relatively highly randomized, with the different polymer blocks relatively highly randomly oriented and located, which is in contrast to the assembled block copolymer layer portion.
discussed in association with the resulting structure of Figure 6D1. The unassembled block copolymer layer portion may be applied in a variety of different ways. By way of example, the block copolymer may be dissolved in a solvent and then spin coated over the surface. Alternatively, the unassembled block copolymer may be spray coated, dip coated, immersion coated, or otherwise coated or applied over the surface. Other ways of applying block copolymers, as well as other ways known in the arts for applying similar organic coatings, may potentially be used. Then, the unassembled layer may form an assembled block copolymer layer portion, e.g., by microphase separation and/or self-assembly of the unassembled block copolymer layer portion. The microphase separation and/or self-assembly occurs through rearrangement and/or repositioning of the block copolymer molecules, and in particular to rearrangement and/or repositioning of the different polymer blocks of the block copolymer molecules.

In one such embodiment, an annealing treatment may be applied to the unassembled block copolymer in order to initiate, accelerate, increase the quality of, or otherwise promote microphase separation and/or self-assembly. In some embodiments, the annealing treatment may include a treatment that is operable to increase a temperature of the block copolymer. One example of such a treatment is baking the layer, heating the layer in an oven or under a thermal lamp, applying infrared radiation to the layer, or otherwise applying heat to or increasing the temperature of the layer. The desired temperature increase will generally be sufficient to significantly accelerate the rate of microphase separation and/or self-assembly of the block polymer without damaging the block copolymer or any other important materials or structures of the integrated circuit substrate. Commonly, the heating may range between about 50°C to about 400°C, or between about 125°C to about 300°C, but not exceeding thermal degradation limits of the block copolymer or integrated circuit substrate. The heating or annealing may help to provide energy to the block copolymer molecules to make them more mobile/ flexible in order to increase the rate of the microphase separation and/or improve the quality of the microphase separation. Such microphase separation or rearrangement/repositioning of the block copolymer molecules may lead to self-assembly to form extremely small (e.g., nano-scale) structures. The self-assembly may occur under the influence of surface energy, molecular affinities, and other surface-related and chemical-related forces.

In any case, in some embodiments, self-assembly of block copolymers, whether based on hydrophobic-hydrophilic differences or otherwise, may be used to form extremely small periodic structures (e.g., precisely spaced nano-scale structures or lines). In some embodiments, they may be used to form nano-scale lines or other nano-scale structures that can ultimately be used to form via and openings. In some embodiments, directed self assembly of block copolymers may be used to form vias that are self aligned with interconnects, as described in greater detail below.
Referring again to Figure 6D1, in an embodiment, for a DSA process, in addition to direction from the underlying ILD/metal 604/602 surfaces the growth process can be affected by the sidewalls of the material of ILD lines 610. As such, in one embodiment, DSA is controlled through graphoepitaxy (from the sidewalls of lines 610) and chemoepitaxy (from the underlying exposed surface characteristics). Constraining the DSA process both physically and chemically can significantly aid the process from a defectivity standpoint. The resulting polymers 616A/616B have fewer degrees of freedom and are fully constrained in all directions through chemical (e.g., underlying ILD or metal lines, or surface modifications made thereto by, for example, a brush approach) and physical (e.g., from the trenches formed between the ILD lines 610).

In an alternative embodiment, a selective growth process is used in place of a DSA approach. Figure 6D2 illustrates a cross-sectional view of the structure of Figure 6B following selective material deposition on the exposed portions of underlying metal and ILD lines, in accordance with another embodiment of the present invention. Referring to Figure 6D2, a first material type 800 is grown above exposed portions of underlying ILD lines 604. A second, different, material type 802 is grown above exposed portions of underlying metal lines 602. In an embodiment, the selective growth is achieved by a dep-etch-dep-etch approach for each of the first and second materials, resulting in a plurality of layers of each of the materials, as depicted in Figure 6D2. Such an approach may be favorable versus conventional selective growth techniques which can form "mushroom-top" shaped films. The mushroom topping film growth tendency can be reduced through an alternating deposition/etch/deposition (dep-etch-dep-etch) approach. In another embodiment, a film is deposited selectively over the metal followed by a different film selectively over the ILD (or vice versa) and repeated numerous times creating a sandwich-like stack. In another embodiment, both materials are grown simultaneously in a reaction chamber (e.g., by a CVD style process) that grows selectively on each exposed region of the underlying substrate.

Figure 6E illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6D1 following removal of one species of polymer, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d', respectively, polymer or polymer portion 616A is removed to re-expose the ILD lines 604 (or hardmask or cap layers formed on the ILD lines 604), while polymer or polymer portion 616B is retained above the metal lines 602. In an embodiment, a deep ultra-violet (DUV) flood expose followed by a wet etch or a selective dry etch is used to selectively remove polymer 616A. It is to be understood that, instead of first removal of the polymer from the ILD lines 604 (as depicted), removal from the metal lines 602
may instead be first performed. Alternatively, a dielectric film is selectively grown over the region, and a mixed scaffolding is not used.

Figure 6F illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6E following formation of an ILD material in the locations opened upon removal of the one species of polymer, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d', respectively, the exposed regions of underlying ILD lines 604 are filled with a permanent interlayer dielectric (ILD) layer 618. As such, the open spaces between all possible via positions are filled with an ILD layer 618 includes a hardmask layer 620 disposed thereon, as depicted in the plan view and in the cross-sectional views (b) and (d) of Figure 6F. It is to be understood that the material of ILD layer 618 need not be the same material as ILD lines 610. In an embodiment, the ILD layer 618 is formed by a deposition and polish process. In the case where ILD layer 618 is formed with an accompanying hardmask layer 620, a special ILD fill material may be used (e.g., polymer encapsulated nanoparticles of ILD that fills holes/trenches).

In such a case, a polish operation may not be necessary.

Referring again to Figure 6F, in an embodiment, the resulting structure includes a uniform ILD structure (ILD lines 610 + ILD layer 618), and the locations of all possible plugs are covered in hardmask 620 and all possible vias are in areas of polymer 616B. In one such embodiment, ILD lines 610 and ILD layer 618 are composed of a same material. In another such embodiment, ILD lines 610 and ILD layer 618 are composed of different ILD materials. In either case, in a specific embodiment, a distinction such as a seam between the materials of ILD lines 610 and ILD layer 618 may be observed in the final structure. Exemplary seams 699 are shown in Figure 6F for illustrative purposes.

Figure 6G illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6F following via patterning, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d', respectively, via locations 622A, 622B and 622C are opened by removal of polymer 616B in select locations. In an embodiment, selective via location formation is accomplished by using a lithographic technique. In one such embodiment, polymer 616B is globally removed with an ash and refilled with photoresist. The photoresist may be highly sensitive and have a large acid diffusion and aggressive deprotection or crosslinking (depending on resist tone) because the latent image is confined in both directions by ILD (e.g., by ILD lines 610 and ILD layer 618). The resist serves as a digital switch to turn "on" or "off" depending whether a via is required in a particular location or not. Ideally, the photoresist can be used to fill the holes only, without spilling over. In an embodiment, the via locations 622A,
622B and 622C are fully confined with the process such that line edge or width roughness
(LWR) and line collapse and/or reflection is mitigated if not eliminated. In an embodiment, low
doses are used with EUV/EBDW and increase runrate significantly. In one embodiment, an
additional advantage with the use of EBDW is that only a single shot type/size that can increase
runrate by significantly reducing the number of apertures required as well as lowering the dose
that needs to be delivered. In a case that 193nm immersion lithography is used, in an
embodiment, the process flow confines the via locations in both directions such the size of the
via that actually is patterned is twice the size of the actual via on the wafer (e.g., assuming 1:1
line/space patterns). Alternatively, the via locations can be selected in the reverse tone where the
vias that need to be retained are protected with photoresist and the remaining sites are removed
and later filled with ILD. Such an approach can allow a single metal fill/polish process at the end
of the patterning flow rather than two separate metal deposition operations.

Figure 6H illustrates a plan view and corresponding cross-sectional views of the structure
of Figure 6G following via formation using a photo-assisted, selective metal deposition process,
in accordance with an embodiment of the present invention. Referring to the plan view and
corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d',
respectively, via locations 622A, 622B and 622C are filled with metal to form vias 624A, 624B
and 624C, respectively.

Figure 6I illustrates a plan view and corresponding cross-sectional views of the structure
of Figure 6H following removal of the second species of polymer and replacement with an ILD
material, in accordance with an embodiment of the present invention. Referring to the plan view
and corresponding cross-sectional views (a)-(d) taken along axes, a-a', b-b', c-c' and d-d',
respectively, remaining polymer or polymer portion 616B (e.g., where vias locations have not
been selected) is removed to re-expose the metal lines 602. Subsequently, an ILD layer 626 is
formed in the locations where the remaining polymer or polymer portion 616B was removed, as
depicted in Figure 6I.

Referring again to Figure 6I, in an embodiment, the resulting structure includes a uniform
ILD structure (ILD lines 610 + ILD layer 618 + ILD layer 626), and the locations of all possible
plugs are covered in hardmask 620. In one such embodiment, ILD lines 610, ILD layer 618 and
ILD layer 626 are composed of a same material. In another such embodiment, two of ILD lines
610, ILD layer 618 and ILD layer 626 are composed of a same material and the third is composed
of a different ILD material. In yet another such embodiment, all of ILD lines 610, ILD layer 618
and ILD layer 626 are composed of a different ILD material with respect to one another. In any
case, in a specific embodiment, a distinction such as a seam between the materials of ILD lines
610 and ILD layer 626 may be observed in the final structure. Exemplary seams 697 are shown
In Figure 6J for illustrative purposes. Likewise, a distinction such as a seam between the materials of ILD layer 618 and ILD layer 626 may be observed in the final structure. Exemplary seams 698 are shown in Figure 6J for illustrative purposes.

Figure 6J illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6J following patterning of a resist or mask in selected plug locations, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a) and (b) taken along axes, a-a' and b-b', respectively, plug positions 628A, 628B and 628C are preserved by forming a mask or resist layer over those locations. Such preservation patterning may be referred to as metal end-to-end lithographic patterning, wherein plug positions are determined where breaks in subsequently formed metal lines are required. It is to be understood that since the plug locations can only be in those locations where ILD layer 618/hardmask 620 are positioned, plugs can occur over the previous layer ILD lines 604. In an embodiment, the patterning is achieved by using a lithography operation (e.g., EUV, EBDW or immersion 193nm). In an embodiment, the process illustrated in Figure 6J, demonstrates use of a positive tone patterning process where the regions where spaces between metal need to occur are preserved. It is to be understood that, in another embodiment, it is also possible to open holes instead and reverse the tone of the process.

Figure 6K illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6J following hardmask removal and ILD layer recessing, in accordance with an embodiment of the present invention. Referring to the plan view and corresponding cross-sectional views (a) and (b) taken along axes, a-a' and b-b', respectively, hardmask 620 is removed and ILD layer 618 and ILD layer 626 are recessed to form recessed ILD layer 618' and recessed ILD layer 626', respectively, by etching of these layers below their original uppermost surfaces. It is to be understood that the recessing of ILD layer 618 and ILD layer 626 is performed without etching or recessing ILD lines 610. The selectivity may be achieved by use of a hardmask layer 612 on the ILD lines (as depicted in cross-sectional views (a) and (b)). Alternatively, in a case that the ILD lines 610 are composed of an ILD material different from the material of ILD layer 618 and ILD layer 626, a selective etch may be used even in the absence of a hardmask 612. The recessing of ILD layer 618 and ILD layer 626 is to provide locations for the second level of metal lines, as isolated by ILD lines 610, as described below. The extent or depth of the recess is, in one embodiment, selected based on the desired ultimate thickness of the metal lines formed thereon. It is to be understood that the ILD layer 618 in the plug locations 628A, 628B and 628C is not recessed.

Figure 6L illustrates a plan view and corresponding cross-sectional views of the structure of Figure 6K following metal line formation, in accordance with an embodiment of the present
invention. Referring to the plan view and corresponding cross-sectional views (a), (b) and (c) taken along axes, a-a', b-b' and c-c', respectively, metal for forming metal interconnect lines is formed conformally above the structure of Figure 6K. The metal is then planarized, e.g., by CMP, to provide metal lines 630, which are confined to locations above recessed ILD layer 618' and recessed ILD layer 626'. The metal lines 630 are coupled with underlying metal lines 602 through the predetermined via locations 624A, 624B and 624C (624B is shown in cross-sectional view (c); note that for illustrative purposes, another via 632 is depicted directly adjacent plug 628B in cross-sectional view (b) even though this is inconsistent with the previous figures). The metal lines 630 are isolated from one another by ILD lines 610 and are disrupted or broken-up by the preserved plugs 628A, 628B and 628C. Any hardmask remaining on the plug locations and/or on the ILD lines 610 may be removed at this portion of the process flow, as depicted in Figure 6L. The metal (e.g., copper and associated barrier and seed layers) deposition and planarization process to form metal lines 630 may be that typically used for standard back end of line (BEOL) single or dual damascene processing. In an embodiment, in subsequent fabrication operations, the ILD lines 610 may be removed to provide air gaps between the resulting metal lines 630.

The structure of Figure 6L may subsequently be used as a foundation for forming subsequent metal line/via and ILD layers. Alternatively, the structure of Figure 6L may represent the final metal interconnect layer in an integrated circuit. It is to be understood that the above process operations may be practiced in alternative sequences, not every operation need be performed and/or additional process operations may be performed. Furthermore, although the above process flow focused on applications of directed self-assembly (DSA), selective growth processes may be used instead in one or more locations of the process flow. In any case, the resulting structures enable fabrication, by selective metal deposition (e.g., photo-assisted ALD/CVD selective deposition), of vias that are directly centered on underlying metal lines. That is, the vias may be wider than, narrower than, or the same thickness as the underlying metal lines, e.g., due to non-perfect selective etch processing. Nonetheless, in an embodiment, the centers of the vias are directly aligned (match up) with the centers of the metal lines. As such, in an embodiment, offset due to conventional lithograph/dual damascene patterning that must otherwise be tolerated, is not a factor for the resulting structures described herein.

In another aspect, one or more embodiments described herein are directed to fabricating semiconductor devices, such as for PMOS and NMOS device fabrication. For example, one or more features of a semiconductor device is formed using a processing scheme involving fabrication of a patterned hardmask layer formed through photodefinable alignment, as described above. As an example of a completed device, Figures 7A and 7B illustrate a cross-sectional view
and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device, in accordance with an embodiment of the present invention.

Referring to Figure 7A, a semiconductor structure or device 700 includes a non-planar active region (e.g., a fin structure including protruding fin portion 704 and sub-fin region 705) formed from substrate 702, and within isolation region 706. A gate line 708 is disposed over the protruding portions 704 of the non-planar active region as well as over a portion of the isolation region 706. As shown, gate line 708 includes a gate electrode 750 and a gate dielectric layer 752. In one embodiment, gate line 708 may also include a dielectric cap layer 754. A gate contact 714, and overlying gate contact via 716 are also seen from this perspective, along with an overlying metal interconnect 760, all of which are disposed in inter-layer dielectric stacks or layers 770. Also seen from the perspective of Figure 7A, the gate contact 714 is, in one embodiment, disposed over isolation region 706, but not over the non-planar active regions. In an embodiment, the pattern of fins is a grating pattern formed by using a processing scheme involving fabrication of a patterned hardmask layer formed through photodefinable alignment, as described above.

Referring to Figure 7B, the gate line 708 is shown as disposed over the protruding fin portions 704. Source and drain regions 704A and 704B of the protruding fin portions 704 can be seen from this perspective. In one embodiment, the source and drain regions 704A and 704B are doped portions of original material of the protruding fin portions 704. In another embodiment, the material of the protruding fin portions 704 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 704A and 704B may extend below the height of dielectric layer 706, i.e., into the sub-fin region 705.

In an embodiment, the semiconductor structure or device 700 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines 708 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

Substrate 702 may be composed of a semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an embodiment, substrate 702 is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof, to form active region 704. In one embodiment, the concentration of silicon atoms in bulk substrate 702 is greater than 97%. In another embodiment, bulk substrate 702 is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer.
grown atop a boron-doped bulk silicon mono-crystalline substrate. Bulk substrate 702 may alternatively be composed of a group III-V material. In an embodiment, bulk substrate 702 is composed of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. In one embodiment, bulk substrate 702 is composed of a III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

Isolation region 706 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, the isolation region 706 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

Gate line 708 may be composed of a gate electrode stack which includes a gate dielectric layer 752 and a gate electrode layer 750. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-K material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of the substrate 702. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride. In an embodiment, the metal layer is a pure metal layer or metal alloy, and may include one or more workfunction and/or fill conductive layers.

Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

Gate contact 714 and overlying gate contact via 716 may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species.
The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material). In accordance with another embodiment of the present invention, at least a portion of a gate contact or gate contact via is formed by photo-assisted ALD/CVD.

In an embodiment (although not shown), providing structure 700 involves formation of a contact pattern which is essentially perfectly aligned to an existing gate pattern while eliminating the use of a lithographic operation with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

Furthermore, the gate stack structure 708 may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF$_6$. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH$_4$OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure 700. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.
Referring again to Figure 7A, the arrangement of semiconductor structure or device 700 places the gate contact over isolation regions. Such an arrangement may be viewed as inefficient use of layout space. In another embodiment, however, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region. In general, prior to (e.g., in addition to) forming a gate contact structure (such as a via) over an active portion of a gate and in a same layer as a trench contact via, one or more embodiments of the present invention include first using a gate aligned trench contact process. Such a process may be implemented to form trench contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a trench contact pattern is formed as aligned to an existing gate pattern. By contrast, conventional approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in combination with selective contact etches. For example, a conventional process may include patterning of a poly (gate) grid with separate patterning of contact features.

It is to be appreciated that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present invention. For example, in one embodiment, dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks. The gate stacks described above may actually be permanent gate stacks as initially formed. Also, the processes described herein may be used to fabricate one or a plurality of semiconductor devices. The semiconductor devices may be transistors or like devices. For example, in an embodiment, the semiconductor devices are a metal-oxide semiconductor (MOS) transistors for logic or memory, or are bipolar transistors. Also, in an embodiment, the semiconductor devices have a three-dimensional architecture, such as a frigate device, an independently accessed double gate device, or a FIN-FET. One or more embodiments may be particularly useful for fabricating semiconductor devices at a 10 nanometer (10 nm) or smaller technology node.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.
Figure 8 illustrates a computing device 800 in accordance with one implementation of the invention. The computing device 800 houses a board 802. The board 802 may include a number of components, including but not limited to a processor 804 and at least one communication chip 806. The processor 804 is physically and electrically coupled to the board 802. In some implementations the at least one communication chip 806 is also physically and electrically coupled to the board 802. In further implementations, the communication chip 806 is part of the processor 804.

Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to the board 802. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 806 enables wireless communications for the transfer of data to and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 806 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communication chips 806. For instance, a first communication chip 806 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 806 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 804 of the computing device 800 includes an integrated circuit die packaged within the processor 804. In some implementations of the invention, the integrated circuit die of the processor includes one or more structures having a pattern formed using a processing scheme involving photodefinable alignment for chemical assisted patterning, built in accordance with implementations of the invention. The term "processor" may refer to any device
or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 806 also includes an integrated circuit die packaged within the communication chip 806. In accordance with an embodiment of the present invention, the integrated circuit die of the communication chip includes one or more structures having a pattern formed using a processing scheme involving photodefinable alignment for chemical assisted patterning, built in accordance with implementations of the invention.

In further implementations, another component housed within the computing device 800 may contain an integrated circuit die that includes one or more structures having a pattern formed using a processing scheme involving photodefinable alignment for chemical assisted patterning, built in accordance with implementations of the invention.

In various implementations, the computing device 800 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic device that processes data.

Figure 9 illustrates an interposer 900 that includes one or more embodiments of the invention. The interposer 900 is an intervening substrate used to bridge a first substrate 902 to a second substrate 904. The first substrate 902 may be, for instance, an integrated circuit die. The second substrate 904 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 900 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 900 may couple an integrated circuit die to a ball grid array (BGA) 906 that can subsequently be coupled to the second substrate 904. In some embodiments, the first and second substrates 902/904 are attached to opposing sides of the interposer 900. In other embodiments, the first and second substrates 902/904 are attached to the same side of the interposer 900. And in further embodiments, three or more substrates are interconnected by way of the interposer 900.

The interposer 900 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 908 and vias 910, including but not limited to through-silicon vias (TSVs) 912. The interposer 900 may further include embedded
devices 914, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 900.

In accordance with embodiments of the invention, apparatuses or processes disclosed herein regarding photodefinable alignment layers for chemical assisted patterning and approaches for forming photodefinable alignment layers for chemical assisted patterning may be used in the fabrication of interposer 900 or in the devices 914.

Thus, embodiments of the present invention include photodefinable alignment layers for chemical assisted patterning and approaches for forming photodefinable alignment layers for chemical assisted patterning.

Embodiments of the invention include a method for forming a photodefinaelble alignment layer, comprising: disposing a chemically amplified resist (CAR) material over a hardmask that includes a switch component; and exposing portions of the CAR material to form exposed resist portions, wherein the exposure produces acid in the exposed resist portions that interact with the switch component to form modified regions of the hardmask below the exposed resist portions. Additional embodiments include a method for forming a photodefinaelble alignment layer, further comprising; removing the CAR material from the top surface of the hardmask subsequent to exposure; disposing a block copolymer over the top surface of the hardmask, wherein the block copolymer segregates into first polymer regions over the unmodified regions of the hardmask and second polymer regions over the modified regions of the hardmask; removing the second polymer regions to expose the modified regions of the hardmask; and etching through the modified regions of the hardmask, wherein the first polymer regions function as a mask to prevent the removal of the unmodified regions of the hardmask. Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein the block copolymer is polystyrene-b-polymethylmethacrylate (PS-b-PMMA). Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein the first polymer region is PS and the second polymer region is PMMA. Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein the CAR material is removed with a polar aprotic solvent. Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein the solvent is acetone, dimethylformamide (DMF), or dimethyl sulfoxide (DMSO). Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein two or more different solvents are used to remove the CAR material. Additional embodiments include a method for forming a photodefinaelble alignment layer, wherein the
modified regions of the hardmask are base soluble and the remainder of the hardmask is base insoluble. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the modified regions of the hardmask include an RCO-OH component and the remainder of the hardmask includes an RCO-OR component. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the switch component is polymer bound within the hardmask. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the switch component is blended within the material. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the switch component is segregated to a top surface of the hardmask.

Embodiments of the invention include a method for forming a photodefinable alignment layer, comprising: disposing a chemically amplified resist (CAR) material over a hardmask; exposing portions of the CAR material to form exposed resist portions; developing the CAR material to expose portions of the hardmask below the exposed resist portions; applying a surface treatment to the exposed portions of the hardmask to form modified regions of the hardmask.

Additional embodiments include a method for forming a photodefinable alignment layer, wherein a developer used to develop the exposed resist portions is also used to apply the surface treatment to the exposed portions of the hardmask. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the developer is tetramethyl ammonium hydroxide (TMAH). Additional embodiments include a method for forming a photodefinable alignment layer, wherein the developer further comprises a reactive surface grafting agent that forms the modified regions of the hardmask. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the surface treatment is an inorganic acid or an organic acid. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the resist is a negative tone photoresist, wherein the developer is an organic solvent, and wherein the organic solvent includes a reactive surface grafting agent that forms the modified regions of the hardmask. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the CAR material further comprises a polymer brush and a photoacid generator (PAG). Additional embodiments include a method for forming a photodefinable alignment layer, wherein exposing the CAR material produces acid in the exposed resist portions that catalyzes attachment of the polymer brush to a surface of the hardmask below the exposed portions of the resist.

Embodiments of the invention include a material stack, comprising: a substrate layer; a hardmask layer formed over the substrate layer, wherein the hardmask layer includes a plurality of patterned through holes, and wherein the hardmask layer further includes a switch component.

Embodiments of the invention include a material stack, wherein the switch component converts
the hardmask from a base insoluble material to a base soluble when it interacts with an acid. Embodiments of the invention include a material stack, wherein the switch component is segregated to a top surface of the hardmask material.

Embodiments include a method for forming a photodefinable alignment layer, comprising: disposing a chemically amplified resist (CAR) material over a hardmask that includes a switch component; exposing portions of the CAR material to form exposed resist portions; annealing the CAR material, wherein the exposure and annealing produces acid in the exposed resist portions that interact with the switch component to form modified regions of the hardmask below the exposed resist portions; removing the CAR material from the top surface of the hardmask subsequent to exposure; disposing a block copolymer over the top surface of the hardmask, wherein the block copolymer segregates into first polymer regions over the unmodified regions of the hardmask and second polymer regions over the modified regions of the hardmask; removing the second polymer regions to expose the modified regions of the hardmask; and etching through the modified regions of the hardmask, wherein the first polymer regions function as a mask to prevent the removal of the unmodified regions of the hardmask. Additional embodiments include a method for forming a photodefinable alignment layer, wherein the block copolymer is polystyrene-b-polymethylmethacrylate (PS-b-PMMA).
What is claimed is:

1. A method for forming a photodefinable alignment layer, comprising:
   disposing a chemically amplified resist (CAR) material over a hardmask that includes a switch component; and
   exposing portions of the CAR material to form exposed resist portions, wherein the exposure produces acid in the exposed resist portions that interact with the switch component to form modified regions of the hardmask below the exposed resist portions.

2. The method of claim 1, further comprising;
   removing the CAR material from the top surface of the hardmask subsequent to exposure;
   disposing a block copolymer over the top surface of the hardmask, wherein the block copolymer segregates into first polymer regions over the unmodified regions of the hardmask and second polymer regions over the modified regions of the hardmask;
   removing the second polymer regions to expose the modified regions of the hardmask; and
   etching through the modified regions of the hardmask, wherein the first polymer regions function as a mask to prevent the removal of the unmodified regions of the hardmask.

3. The method of claim 2, wherein the block copolymer is polystyrene-b-polymethylmethacrylate (PS-b-PMMA).

4. The method of claim 3, wherein the first polymer region is PS and the second polymer region is PMMA.

5. The method of claim 2, wherein the CAR material is removed with a polar aprotic solvent.

6. The method of claim 5, wherein the solvent is acetone, dimethylformamide (DMF), or dimethyl sulfoxide (DMSO).

7. The method of claim 5, wherein two or more different solvents are used to remove the CAR material.
8. The method of claim 1, wherein the modified regions of the hardmask are base soluble and the remainder of the hardmask is base insoluble.

9. The method of claim 8, wherein the modified regions of the hardmask include an RCO-OH component and the remainder of the hardmask includes an RCO-OR component.

10. The method of claim 1, wherein the switch component is polymer bound within the hardmask.

11. The method of claim 1, wherein the switch component is blended within the material.

12. The method of claim 1, wherein the switch component is segregated to a top surface of the hardmask.

13. A method for forming a photodefinition alignment layer, comprising:
   disposing a chemically amplified resist (CAR) material over a hardmask;
   exposing portions of the CAR material to form exposed resist portions;
   developing the CAR material to expose portions of the hardmask below the exposed resist portions;
   applying a surface treatment to the exposed portions of the hardmask to form modified regions of the hardmask.

14. The method of claim 13, wherein a developer used to develop the exposed resist portions is also used to apply the surface treatment to the exposed portions of the hardmask.

15. The method of claim 14, wherein the developer is tetramethyl ammonium hydroxide (TMAH).

16. The method of claim 14, wherein the developer further comprises a reactive surface grafting agent that forms the modified regions of the hardmask.

17. The method of claim 14, wherein the surface treatment is an inorganic acid or an organic acid.
18. The method of claim 14, wherein the resist is a negative tone photoresist, wherein the developer is an organic solvent, and wherein the organic solvent includes a reactive surface grafting agent that forms the modified regions of the hardmask.

19. The method of claim 13, wherein the CAR material further comprises a polymer brush and a photoacid generator (PAG).

20. The method of claim 19, wherein exposing the CAR material produces acid in the exposed resist portions that catalyzes attachment of the polymer brush to a surface of the hardmask below the exposed portions of the resist.

21. A material stack, comprising:
   a substrate layer;
   a hardmask layer formed over the substrate layer, wherein the hardmask layer includes a plurality of patterned through holes, and wherein the hardmask layer further includes a switch component.

22. The material stack of claim 21, wherein the switch component converts the hardmask from a base insoluble material to a base soluble when it interacts with an acid.

23. The method of claim 21, wherein the switch component is segregated to a top surface of the hardmask material.

24. A method for forming a photodefiable alignment layer, comprising:
   disposing a chemically amplified resist (CAR) material over a hardmask that includes a switch component;
   exposing portions of the CAR material to form exposed resist portions;
   annealing the CAR material, wherein the exposure and annealing produces acid in the exposed resist portions that interact with the switch component to form modified regions of the hardmask below the exposed resist portions;
   removing the CAR material from the top surface of the hardmask subsequent to exposure;
   disposing a block copolymer over the top surface of the hardmask, wherein the block copolymer segregates into first polymer regions over the unmodified regions of the hardmask and second polymer regions over the modified regions of the hardmask;
   removing the second polymer regions to expose the modified regions of the hardmask;
etchant through the modified regions of the hardmask, wherein the first polymer regions function as a mask to prevent the removal of the unmodified regions of the hardmask.

25. The method of claim 24, wherein the block copolymer is polystyrene-b-polymethylmethacrylate (PS-b-PMMA).
FIG. 5
FIG. 6D2
INTERNATIONAL SEARCH REPORT

International application No. PCT/US2014/072384

A. CLASSIFICATION OF SUBJECT MATTER
H01L 21/308/2006.01/i, H01L 21/311/2006.01/i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/308; B29C 33/42; G03F 7/004; G03F 7/039; G03F 7/20; H01L 21/3 11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: chemically amplified resist, photodefinable alignment, epitaxial self-assembly, block copolymer, acid

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Relevant to claim No.</th>
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Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search 30 September 2015 (30.09.2015)
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