

[54] COMPENSATED ELECTRONIC VOLTAGE
SOURCE
[75] Inventor: Robert R. Marley, Phoenix, Ariz.
[73] Assignee: Motorola, Inc., Chicago, Ill.
[22] Filed: Dec. 20, 1973
[21] Appl. No.: 426,968

[52] U.S. Cl. 323/19; 323/22 T; 323/23
[51] Int. Cl. G05f 5/00
[58] Field of Search 307/296, 297; 323/1, 4,
323/8, 16, 19, 22 T, 23

[56] References Cited

UNITED STATES PATENTS			
3,649,926	3/1972	Hill	323/1 UX
3,781,648	12/1973	Owens	323/4
3,787,734	1/1974	Dorler et al.	323/22 T
3,794,861	2/1974	Bernacchi	307/297

OTHER PUBLICATIONS
Widlar, New Developments in IC Voltage Regulators,
IEEE Journal of Solid-State Circuits, Vol. SCHy 6,
No. 1, Feb. 1971, pgs. 2-7.

Primary Examiner—A. D. Pellinen
Attorney, Agent, or Firm—Vincent J. Rauner; Maurice
J. Jones, Jr.

[57] ABSTRACT
A voltage and temperature stable integrated voltage
regulator circuit offsets the negative temperature coef-
ficient of the base-to-emitter voltage of one transistor
with a positive temperature coefficient derived from
the base-to-emitter voltage differential ΔV_{BE} between
a pair of additional transistors. Other transistors are
used to produce a pair of regulated stable output volt-
ages, each having a predetermined voltage with re-
spect to a different one of the two input voltage termi-
nals across which the regulator circuit is connected.
Circuit components are provided to cause the two out-
put voltages to be voltage and temperature stable or to
have a predetermined controllable temperature coeffi-
cient.

24 Claims, 4 Drawing Figures

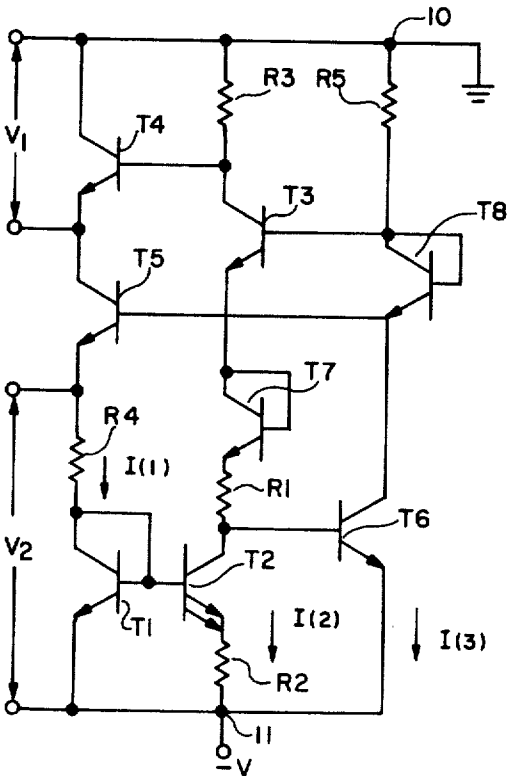


Fig. 1

PRIOR ART

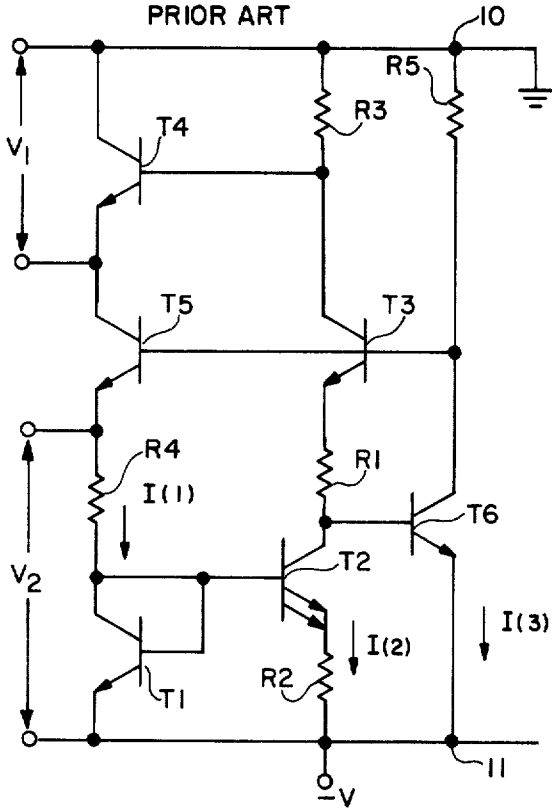


Fig. 2

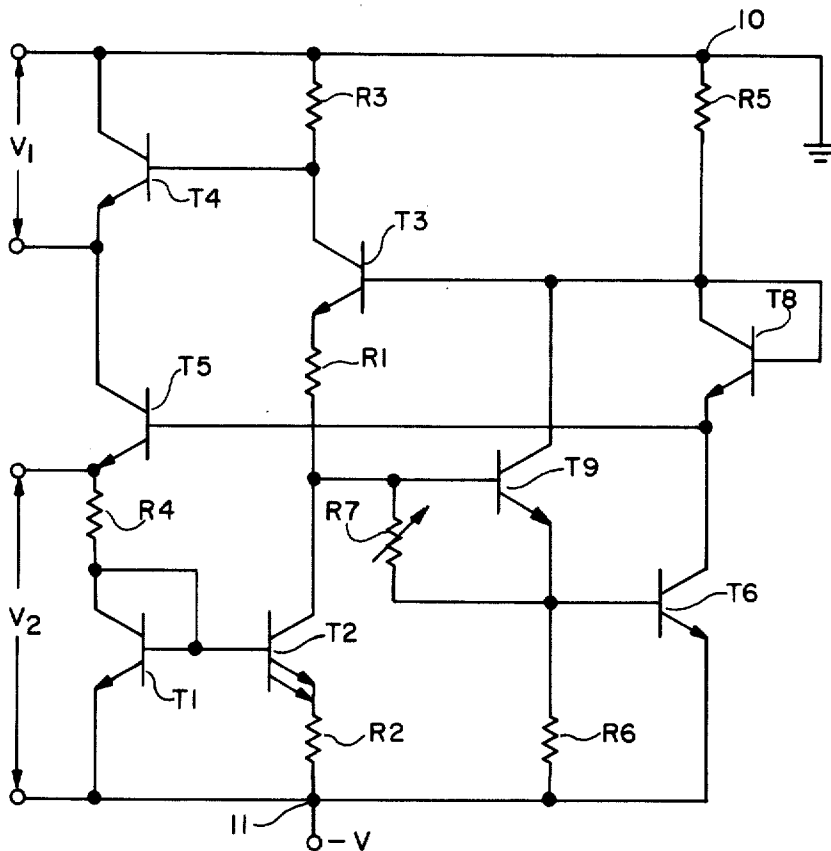
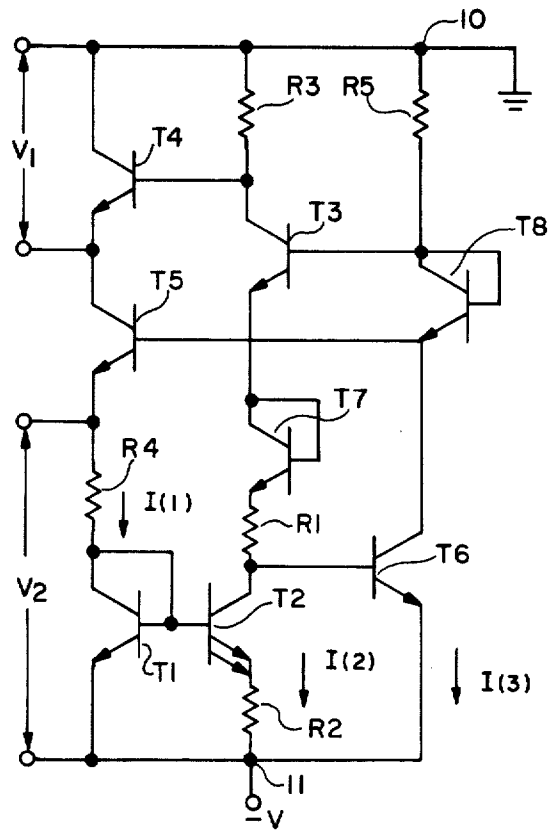


Fig. 3

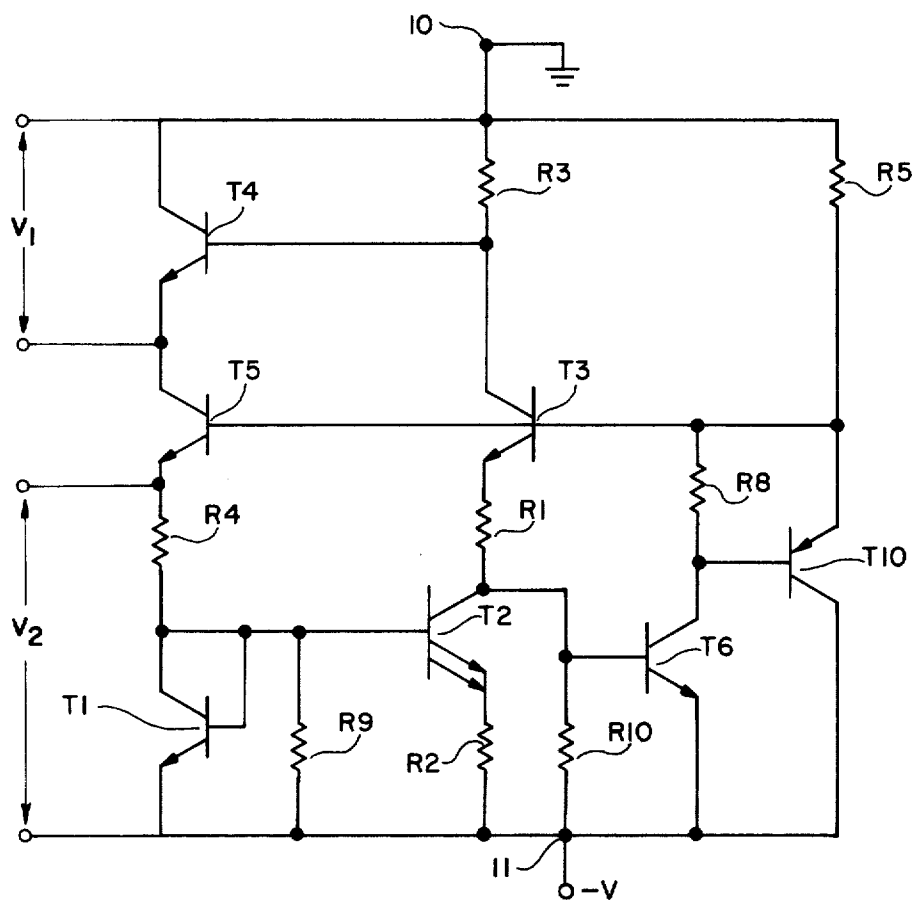


Fig. 4

COMPENSATED ELECTRONIC VOLTAGE SOURCE

BACKGROUND OF THE INVENTION

A monolithic integrated circuit voltage regulator using only transistors and capable of providing a zero temperature coefficient regulated output voltage has been developed. Such a regulator is a three terminal device and can be packaged in a standard three terminal transistor power package.

A modification of this circuit has been made to produce two output voltages of the type which are commonly required for emitter coupled logic (ECL) transistor logic circuits. The two output voltages required for such ECL circuits are used, respectively, to supply a bias voltage (V_{BH}) to the gates and to supply a bias voltage (V_{CS}) for the current source of the circuits. One of these voltages, the current source bias voltage, generally is established with reference to the negative supply voltage used with such circuits. It has been found that when such a modified regulator circuit is used to supply these bias voltages, the current source bias voltage is subject to substantial variation with variations in the unregulated negative supply voltage. This is undesirable for ECL systems requiring a high degree of regulation.

In addition, the known regulators used with ECL circuits do not provide output voltages which track with temperature the characteristics of the ECL circuits itself. Since the ECL circuit exhibits a predetermined variation in characteristics with temperature it is desirable for some applications that the circuit providing the bias voltages also exhibits a matching or tracking temperature characteristic to ensure that the operating characteristics of the ECL circuits remain the same over a wide ambient temperature range.

SUMMARY OF THE INVENTION

It is an object of this invention to provide an improved voltage regulator circuit.

It is another object of this invention to provide a voltage regulator which produces an output voltage which is substantially independent of supply voltage variations over a wide range of temperature.

It is an additional object of this invention to generate two regulated voltages with a voltage regulator circuit capable of integrated circuit fabrication.

It is a further object of this invention to provide a voltage regulator providing at least one output voltage which is substantially independent of the variations of the supply voltage applied to the regulator and which has a predetermined temperature coefficient.

In accordance with a preferred embodiment of this invention, a voltage regulator circuit has first and second voltage input terminals which are adapted to be connected across an unregulated direct current voltage source. A first transistorized circuit is coupled with the first and second input terminals and has an output terminal providing a voltage with a positive temperature coefficient. A shunt regulator transistor has its base connected to the output terminal of the first transistorized circuit. The emitter of the shunt regulator transistor is coupled with the second of the input terminal and its collector is connected through compensating circuit to the first input terminal. The compensating circuit offsets variations in the voltage across the base-emitter junction of the shunt regulator transistor with varia-

tions in the voltage appearing on the second input terminal. An emitter-follower circuit includes an output transistor with its base coupled to the collector of the shunt regulator transistor, its collector coupled with the first input terminal and its emitter coupled with the second input terminal by way of the first transistorized circuit. The interconnections of the shunt regulator transistor and the compensating circuit, in cooperation with the base-emitter junction of the emitter-follower output transistor, operate in conjunction with the first transistorized circuit to produce an output voltage which is substantially independent of variations in the supply voltage applied across the first and second input terminals and which has a predetermined temperature coefficient.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a prior art circuit; and FIGS. 2, 3 and 4 are circuit diagrams of preferred embodiments of this invention illustrating different techniques for compensation of voltage regulators.

DETAILED DESCRIPTION

Referring now to the drawings, in which the same or similar components are identified by the same reference numerals throughout the several figures, there is shown in FIG. 1 a prior art voltage regulator circuit used as a bias driver for an ECL digital logic system. For such systems, it is desirable to produce two regulated output voltages which are identified in FIG. 1 as V_1 and V_2 . The voltage V_1 is established with respect to ground or reference potential and the voltage V_2 is established with respect to a negative direct current supply potential $-V$ illustrated in FIG. 1. The reference potential and negative supply potential $-V$ are applied respectively to a pair of input terminals 10 and 11 which constitute the voltage input terminals for the circuit.

The lower portion of the circuit includes first and second NPN transistors T1 and T2 interconnected to operate at different current densities, so that a positive temperature coefficient of the base-to-emitter voltage differential ΔV_{BE} is produced between them. This is done by interconnecting the collector and base of the transistor T1 to cause it to operate as a diode, with its emitter connected directly to the $-V$ input voltage supply terminal 11. The different current densities are achieved by connecting a resistor R2 between the emitter of the transistor T2 and the terminal 11, while the base of the transistor T2 is connected directly to the collector of the transistor T1.

If the emitter areas of the transistors T1 and T2 were equal, currents $I(1)$ and $I(2)$ flowing through these transistors respectively would be such that the current $I(2)$ would be less than the current $I(1)$. For reasons which will be more fully understood subsequently, it is desirable for these two currents to be equal, while still maintaining the positive temperature coefficient base-to-emitter voltage differential ΔV_{BE} between the transistors T1 and T2. To accomplish this, the total emitter area of the transistor T2 is made larger than that of the transistor diode T1. This is represented in FIG. 1 by showing the transistor T2 as having a double or dual emitter. The exact ratio of the emitter areas of the transistors T1 and T2 must be determined in conjunction with the value of resistance of the resistor R2 to arrive

at the ratio which results in the relationship of $I(1)=I(2)$.

Since the transistors T1 and T2 are operated at different current densities, the voltage drop across the resistor R2 is proportional to the base-emitter voltage differential ΔV_{BE} . The current gains of the transistors are chosen to be high; so that the voltage drop across the collector resistor R1 of the transistor T2 also is proportional to ΔV_{BE} .

The current $I(2)$ is supplied to the resistor R1 through the collector-emitter path of a third NPN transistor T3 and a load resistor R3, coupled to the input terminal 10. Similarly the current $I(1)$ for the transistor diode T1 is supplied through the collector-emitter paths of a pair of NPN transistors T4 and T5 and a resistor R4.

The collector of the transistor T2 is connected to the base of an NPN shunt regulator transistor T6, which has its emitter connected to the input terminal 11 and its collector connected through a load resistor R5 to the terminal 10. The positive temperature coefficient of the voltage applied from the collector of the transistor T2 to the base of the transistor T6 is adjusted by the adjustment of the differential current densities of the transistors T1 and T2 to produce a voltage drop across the resistor R1, which, when it is added to the voltage drop across the base-emitter junction of the transistor T6, results in a voltage on the collector of the transistor T6 which is proportional to the energy band gap of the semiconductor material of the transistors. This voltage has a zero temperature coefficient and is coupled to the bases of the two emitter-follower transistors T3 and T5.

The emitters of the transistors T3 and T5 are coupled respectively to the resistors R1 and R4 in the current paths supplying the currents $I(2)$ and $I(1)$ to the transistors T2 and T1. The collector of the transistor T3 also is connected to the base of the transistor T4, which results in the reference voltage V1 being expressed as:

$$V_1 = \phi_4 + R_3 I_{(1)} \quad (1)$$

where ϕ_4 is the base-to-emitter voltage of the transistor T4 and $R_3 I_{(1)}$ is the voltage across R_3 . The currents $I_{(1)}$ and $I_{(2)}$ are voltage independent due to the nature of the circuit interconnections. Thus, the voltage V_1 also is essentially voltage independent.

The current $I(3)$, however, is produced by the shunt regulator transistor T6 and varies significantly with any variations in the negative voltage ($-V$) applied to the input terminal 11. Because of the relatively large current variations in the current $I(3)$ resulting from the shunt regulator operation of the transistor T6, the emitter-base forward voltage ϕ_6 of the transistor T6 also varies substantially. This term appears in the output voltage V2 supplied by the regulator circuit shown in FIG. 1. The voltage V2 may be derived as follows:

$$V_2 = \phi_6 + R_1 I_{(2)} + \phi_3 - \phi_5 \quad (2)$$

where $R_1 I_{(2)}$ is the voltage drop across the resistor R1, ϕ_3 is the emitter-base voltage of the transistor T3 and ϕ_5 is the base-emitter voltage of the transistor T5.

The operating conditions of the circuit are established to cause the currents $I(1)$ and $I(2)$ to be equal,

so that ϕ_3 equals ϕ_5 if the transistors T3 and T5 are matched. The equation then can be expressed as:

$$V_2 = \phi_6 + R_1 I_{(1)} \quad (3)$$

From the foregoing it can be seen that although the voltage V1 is substantially independent of supply voltage variations, the voltage V2 is not independent and varies significantly to the same extent that the term ϕ_6 , the emitter-base forward voltage of the transistor T6, varies with variations in the negative voltage applied to the terminal 11. If both of the voltages V1 and V2 are made substantially independent of temperature variations and supply voltage variations, greater system noise immunity can be obtained in computer systems which use such a bias driver circuit to supply the operating potentials for the logic circuits, such as ECL logic, of the system.

To overcome the deficiencies in the circuit illustrated in FIG. 1, the circuits of FIG. 2 and FIG. 3 have been developed. The circuit of FIG. 2 will be considered first, and so far as the components of the circuit of FIG. 2 are the same as those of the circuit of FIG. 1, no additional description of those components will be made. The voltage V1 in FIG. 2 is generated in the same manner as it is in the circuit of FIG. 1. The voltage V2, however, in FIG. 2 is developed from a modified circuit which includes a transistor diode T7 connected in series between the emitter of the transistor T3 and the resistor R1. In addition, a second transistor diode T8 is connected in series between the lower terminal of the resistor R5 and the collector of the transistor T6. The base-collector junction of the transistor diode T8 is connected to the base of the transistor T3 to provide voltage drive for that transistor, while the base of the transistor T5 continues to be connected to the collector of the transistor T6. The addition of the two transistor diodes T7 and T8 changes the relationship of the output voltage V2 in accordance with the following expression:

$$V_2 = \phi_6 + R_1 I_{(2)} + \phi_7 + \phi_3 - \phi_8 - \phi_5 \quad (4)$$

where ϕ_7 is the emitter-base voltage of the transistor T7, and ϕ_8 is the base-emitter voltage of the transistor T8.

The transistor diode T7 is matched to the transistor T3 so that both of these transistors have the same emitter-base voltage drop across them. Thus $\phi_3 = \phi_7$. As discussed in conjunction with the development of the equations for the voltage V2 in conjunction with FIG. 1, the currents $I_{(1)}$ and $I_{(2)}$ are selected to be equal so that $\phi_3 = \phi_5$. The transistor diode T8 is matched to the transistor T6; so that $\phi_8 = \phi_6$. In addition, the transistors T4 and T5 are matched so that ϕ_4 equals ϕ_5 . The equation then can be expressed as:

$$V_2 = R_1 I_{(1)} + \phi_4 \quad (5)$$

If in addition, R1 equals R3, then the equation for V2 is the same as that for V1, namely:

$$V_2 = R_3 I_{(1)} + \phi_4 \quad (6)$$

With the addition of the two transistor diodes T7 and T8, the undesirable voltage dependent components have been removed from the output voltage V2 and the two output voltages V1 and V2 are the same but with reference to the two different input terminals 10 and 11 respectively.

One transistor base-emitter voltage term (ϕ_i) remains in each of these output voltages because such a term is desirable in ECL circuits to match the characteristics of the ECL circuits which are supplied with these two bias voltages. The transistor diode T7 is required to produce sufficient voltage drop across R4 and the transistor diode T1 to turn on the transistor T1 when the transistor diode T8 is added to the circuit to cancel the effects of the transistor T6.

Referring now to FIG. 3, there is shown another version of the circuit for producing V2 with a controllable temperature tracking rate or temperature coefficient for both of the output voltages V1 and V2. No additional description will be made of those circuit components which already have been described.

FIG. 3 differs from FIG. 2 in that the transistor diode T7 has been eliminated and is replaced with a transistor T9 having its collector connected to the junction of the base of the transistor T3 and the collector of the transistor diode T8. Its base is connected to the collector of the transistor T2. The shunt regulator transistor T6 no longer has its base connected directly to the collector of the transistor T2, but the base of the transistor T6 is connected to the junction of the emitter of the transistor T9. A large value resistor R6 operates as a power supply insensitive current source for the transistor T9, and a resistor R7 is connected across the base and emitter electrodes of the transistor T9.

The transistor diode T8 of FIG. 3 operates to cancel out the base-emitter voltage effects of the transistor T6 from the output voltage V2 in the same manner as described above in conjunction with FIG. 2. The circuit configuration of FIG. 3, however, operates to enable a choice of a temperature tracking rate which varies from a zero temperature coefficient to a negative temperature coefficient of approximately -2.7 millivolts per degree centigrade for the two output voltages V1 and V2 (at nominal output voltage of 1.3 volts). This provides the greatest flexibility for the circuit in its utilization as a bias voltage driver circuit for logic circuits which in turn may exhibit positive or negative coefficients of temperature in their operation. It is desirable to have the bias or regulator circuit track the circuits with which it is used to minimize temperature effects.

The operation of the circuit of FIG. 3 is such that the transistor combination of the transistors T1 and T2 continues to generate a small voltage across the resistor R2 which has a positive temperature coefficient due to the difference in the device current densities of the transistors T1 and T2.

As stated previously, the gain ratio of the resistors R1 and R3 amplifies this voltage as it is needed for the circuit. Because the resistor R6 and the emitter-base voltage ϕ_6 of transistor T6 set the current of the transistor T9, the V_{BE} voltage of the transistor T9 is essentially just temperature dependent. The resistor R7, which is connected across this V_{BE} voltage thus produces a current which has a negative temperature coefficient in voltage across the resistor R1. By adjusting the relative values of the resistors R1, R2, R7 and R3, the voltage across the resistors R1 and R3 can be varied from a

positive temperature coefficient to a negative temperature coefficient and allows a wide variation of temperature tracking rates for the circuit. This variation can be effected in large part by making the resistor R7 a variable resistor.

If it is desirable to have the output voltages V1 and V2 equal each other, it is necessary that the resistors R1 and R3 are equal. If V1 and V2 do not have to be equal, these resistors can have different values. The development of the equations for the voltages V1 and V2 for the circuit of FIG. 3 is accomplished in the same way as the development which has been given above in conjunction with the description of FIGS. 1 and 2.

In FIG. 4 there is shown another embodiment in which the sensitivity of the shunt regulator transistor T6 to variations in the supply voltage ($-V$) is compensated for without the addition of the separate transistor diode T8 which is illustrated in FIGS. 2 and 3. In the circuit of FIG. 4, the collector of the transistor T2 is connected directly to the base of the shunt regulator transistor T6 in the same manner as in FIG. 1. The collector of the shunt regulator transistor T6, however, is not connected directly to the resistor R5 but instead is connected to the base of a substrate PNP transistor T10 and through a resistor R8 to the junction of the emitter of the transistor T10 with the resistor R5. The collector of the transistor T10 is connected directly to the voltage supply terminal 11.

This configuration causes the PNP transistor T10 to shunt the excess current flowing in the shunt regulator path and forces the current in the transistor T6 to be substantially voltage independent and only temperature dependent. This occurs since the voltage across the resistor R8 is established by the emitter-base voltage of the transistor T10 which is essentially a constant voltage. The other portions of the circuit shown in FIG. 4 operate in the same manner as in the discussion of the circuit shown in FIG. 1.

If it is desired to cause the circuit of FIG. 4 to have something other than a zero temperature coefficient, a pair of resistors R9 and R10 can be connected between the collectors of the transistors T1 and T2, respectively, and the negative supply terminal 11. The ratio of the values of the resistors R9 and R10 can be varied in conjunction with the value of the resistor R1 to adjust the output voltage produced by the circuit of FIG. 4 from one which has a positive temperature coefficient to a negative temperature coefficient over a wide variation of temperature tracking rates for the circuit. Resistors R9 and R10 also can be varied in absolute value to change the voltage levels at the outputs for V1 and V2. If these features are not desired, the resistors R9 and R10 can be eliminated and the circuit will operate substantially as a zero temperature coefficient circuit.

The circuit of FIG. 4 does not require the additional diode junction of the transistors T7 or T9 of FIGS. 2 and 3, so it is capable of operation with a minimum supply voltage which is lower by one V_{BE} voltage drop than the circuits of FIGS. 2 and 3. This is desirable for low voltage applications. The location of the transistor T10 of the circuit of FIG. 4 results in excellent high frequency roll-off, so that the tendency of the circuit to oscillate is minimized. This would not be the case if a PNP transistor current source were connected between the input terminal 10 and the collector of the transistor T6 in place of the resistor R5.

The circuits illustrated in FIGS. 2, 3 and 4 which have been described above, exhibit excellent insensitivity to variations in the supply voltage ($-V$) applied to the input terminal 11 as opposed to the circuit shown in FIG. 1. In addition, the circuits of FIGS. 3 and 4 permit the selection of a wide range of desired temperature tracking rates between negative coefficients of temperature and positive coefficients of temperature, while the circuits of FIGS. 2 and 4 are illustrative of a fully compensated bias drivers or voltage regulator circuits.

The circuits of FIG. 2 and 3 use an offsetting diode to produce the insensitivity of the circuit to variations in the supply voltage ($-V$), while the circuit shown in FIG. 4 achieves this result by the use of a current stabilizing technique. The net result on the operation of the circuits is the same for both of these approaches and it is the elimination of the problem of variations in the supply voltage ($-V$) from affecting the output voltages produced by the circuits.

I claim:

1. A voltage regulator circuit having first and second voltage input terminals for connection across an unregulated direct current voltage source including in combination:

first transistor circuit means coupled with said first and second voltage input terminals and having an output terminal supplying a voltage having a predetermined positive temperature coefficient;

a shunt regulator transistor with emitter, base and collector electrodes, the emitter thereof coupled with said second input terminal and the base thereof coupled with the output terminal of said first transistor circuit means;

first diode means;

first resistance means coupled with said first diode means at a first junction in a series circuit, in the order named, between said first input terminal and the output terminal of said first transistor circuit means;

compensating means coupled between said first junction and the collector of said shunt regulator transistor for offsetting variations of the voltage across the base-emitter junction of said shunt regulator transistor with variations in the voltage appearing on said second input terminal; and

output circuit means including an output transistor having base, collector and emitter electrodes, the base thereof coupled with the collector of said shunt regulator transistor, the collector thereof coupled with said first voltage input terminal and the emitter thereof coupled with said second voltage input terminal.

2. The combination according to claim 1 wherein the emitter of said output transistor is coupled with said second voltage input terminal through at least a portion of said first transistor circuit means, thereby comprising the coupling for said first transistor circuit means with said first input terminal.

3. The combination according to claim 1 further including second resistance means coupled with said first diode means in said series circuit between said first junction and the base of said shunt regulator transistor.

4. The combination according to claim 1 wherein said compensating means comprises second diode means.

5. The combination according to claim 4 further including third diode means coupled in series with said first diode means between said first junction and the base of said shunt regulator transistor, and wherein said first transistor circuit means causes substantially equal current to flow through said first and third diode means and said output transistor in said output circuit means.

6. The combination according to claim 5 wherein said first, second and third diode means and the base-emitter junctions of said shunt regulator transistor and said output transistor all are connected between said first and second input terminals in the forward current conducting direction.

7. The combination according to claim 5 wherein said third diode means comprises the base-emitter junction of a third transistor and wherein a shunt resistance means is connected in parallel with said base-emitter junction.

8. A voltage regulator circuit having first and second input terminals for connection across an unregulated direct current voltage source, including in combination:

first resistance means;

first and second transistor means, each having base, emitter, and collector electrodes, with the collector-emitter path of said first transistor, said first resistance means, and the collector-emitter path of said second transistor coupled in the order named in series circuit between said first and second input terminals, the base of said second transistor coupled with the collector thereof;

second and third resistance means;

third, fourth and fifth transistor means, each having base, collector, and emitter electrodes, with the collector-emitter paths of said third transistor means and said fourth transistor means coupled in series circuit with said third resistance means, the collector-emitter path of said fifth transistor means and said second resistance means, in the order named, between said first and second voltage supply terminals, the base of said fifth transistor means being coupled with the collector of said second transistor means, and the base of said fourth transistor means being coupled with its collector;

sixth and seventh transistor means, each having base, collector, and emitter electrodes, with the collector-emitter paths of said seventh and sixth transistor means connected in series circuit in the order named between said first and second input terminals, the bases of said third and seventh transistor means being coupled with the collector of said seventh transistor means, the collector of said sixth transistor means being coupled with the base of said first transistor means, and the base of said sixth transistor means being coupled with the collector of said fifth transistor means to form a voltage regulator circuit having at least one output terminal at the emitter of said first transistor.

9. The combination according to claim 8 further including a fourth resistance means and an eighth transistor means having base, collector, and emitter electrodes, with the collector thereof coupled with said first input terminal, the emitter thereof coupled with the collector of said first transistor means, and the base thereof coupled with the collector of said third transistor means and through said fourth resistance means to said first input terminal, the resistance of said third and

fourth resistance means being equal and the junction of the emitter of said eighth transistor means and the collector of said first transistor means comprising a second output terminal for said regulator circuit.

10. The combination according to claim 8 wherein all of said transistor means comprise NPN transistors and said second input terminal is adapted to be coupled with a source of negative direct current potential and said first input terminal is adapted to be connected with ground potential.

11. The combination according to claim 10 wherein the emitter of said second transistor is coupled directly to said second input terminal and said fifth transistor has a total emitter area which is greater than the emitter area of said second transistor, such that the total collector-emitter current of said fifth transistor passing through said second resistance means is equal to the collector-emitter current of said second transistor, with said fifth transistor operating at a lower current density than said second transistor.

12. A voltage regulator circuit having first and second input terminals adapted to be connected respectively to a point of reference potential and an unregulated DC voltage source, including in combination:

first resistance means;

first diode means;

a first transistor having base, collector, and emitter electrodes, with the collector and emitter of said first transistor, said first resistance, and said first diode means connected in a first series circuit, in the order named, between said first input terminal and said second input terminal;

second and third resistance means;

second and third transistors, each having base, collector, and emitter electrodes, with the collector and emitter of said second transistor, said third resistance means, the collector and emitter of said third transistor, and said second resistance means connected in a second series circuit, in the order named, between said first and second input terminals, the base of said third transistor being connected to the junction of said first resistance means with said first diode means;

second diode means;

a fourth transistor having base, collector, and emitter electrodes, said second diode means coupled in a third series circuit with the collector and emitter of said fourth transistor, in the order named, between said first and second input terminals, the collector of said fourth transistor coupled with the base of said first transistor, the base of said second transistor coupled with said second diode means;

fourth resistance means coupled between the base of said fourth transistor and said second input terminal; and

third diode means coupled between the collector of said third transistor and the base of said fourth transistor.

13. The combination according to claim 12 further including a fifth resistance means coupled across said third diode means; and a sixth resistance means coupled between said second diode means and said first input terminal.

14. The combination according to claim 13 wherein said first, second and third diode means comprise fifth, sixth and seventh transistors, respectively; with the emitter of said fifth transistor being coupled to said sec-

ond input terminal, and the base and collector thereof being coupled to said first resistance means; with the emitter of said sixth transistor being coupled to the collector of said fourth transistor, and the collector and base of said sixth transistor both being coupled with the base of said second transistor and the collector of said seventh transistor; with the base of said seventh transistor being coupled with the collector of said third transistor, and the emitter of said seventh transistor being coupled with the base of said fourth transistor.

15. The combination according to claim 14 wherein the emitter of said fifth transistor is coupled directly to said second input terminal and said third transistor has a total emitter area which is greater than the emitter area of said fifth transistor, such that the total collector-emitter current of said third transistor passing through said second resistance means is equal to the collector-emitter current of said fifth transistor, with said third transistor operating at a lower current density than said fifth transistor.

16. The combination according to claim 14 wherein said fifth resistance means coupled across the base and emitter electrodes of said seventh transistor comprises a variable resistor.

17. The combination according to claim 14 wherein all of said transistors are of the same conductivity type.

18. The combination according to claim 17 further including a sixth resistance means coupled between said first input terminal and the collector of said sixth transistor; seventh resistance means coupled between the collector of said second transistor and said first input terminal, said third and seventh resistance means having the same value of resistance; and an eighth transistor having collector, base and emitter electrodes, with the base thereof coupled with the collector of said second transistor, the collector thereof coupled with said first input terminal, and the emitter thereof coupled with the collector of said first transistor, a second output terminal being provided at the emitter of said eighth transistor.

19. A voltage regulator circuit having first and second input terminals for connection across an unregulated direct current voltage source including in combination:

first resistance means;

first and second transistor means each having base, emitter and collector electrodes, with the collector-emitter path of said first transistor, said first resistance means and the collector-emitter path of said second transistor coupled, in the order named, in series circuit between said first and second input terminals, the base of said second transistor means coupled with the collector thereof;

second and third resistance means;

third and fourth transistor means each having base, collector and emitter electrodes, with the collector-emitter path of said third transistor means, said third resistance means, the collector emitter path of said fourth transistor means, and said second resistance means coupled in series circuit, in the order named, between said first and second voltage supply terminals, the base of said fourth transistor means being coupled with the collector of said second transistor means;

fourth and fifth resistance means;

fifth transistor means having base, collector and emitter electrodes, with the base thereof coupled

11

12

with the collector of said fourth transistor means, and said fourth and fifth resistance means coupled in series circuit with the collector-emitter path of said fifth transistor means, in the order named, between said first and second input terminals, said first, second, third, fourth and fifth transistor means all being of the same conductivity type; and sixth transistor means of a conductivity type opposite to the conductivity type of said fifth transistor means and having base, collector and emitter electrodes, the emitter of said sixth transistor means coupled with the bases of said first and third transistor means and coupled with a junction between said fourth and fifth resistance means, the base coupled with the collector of said fifth transistor means and the collector of said sixth transistor means coupled with said second input terminal.

20. The combination according to claim 19 wherein said first, second, third, fourth and fifth transistor means are NPN transistors and said sixth transistor means is a PNP transistor.

21. The combination according to claim 20 wherein said voltage regulator circuit is fabricated as a monolithic integrated circuit and said sixth transistor is a sub-

strate PNP transistor.

22. The combination according to claim 20 further including a sixth resistance means coupled between the collector of said second transistor and said second input terminal and a seventh resistance means coupled between the collector of said fourth transistor and said second input terminal.

23. The combination according to claim 20 further including an additional resistance means and a seventh NPN transistor having base, collector and emitter electrodes, with the collector thereof coupled with said first input terminal, the emitter thereof coupled with the collector of said first transistor, and the base thereof coupled with the collector of said third transistor and further coupled through said additional resistance means to said first input terminal.

24. The combination according to claim 23 wherein said third resistance means and said additional resistance means have the same value of resistance, and first and second output terminals for said voltage regulator circuit are obtained at the emitters of said first and seventh transistors, respectively.

* * * * *

25

30

35

40

45

50

55

60

65