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 <i>H02M 3/155</i> (2006.01)</p> | <p>2721, Tumwater, Washington 98512 (US). DIBENE, Joseph T. [US/US]; 4408 87th SE, Olympia, Washington 98501 (US).</p> |
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 PCT/US2013/048766</p> | <p>(74) Agent: NORDSTROM, Erik R.; c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).</p> |
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- (54) Title:** METHOD AND APPARATUS OF CURRENT BALANCING FOR MULTIPLE PHASE POWER CONVERTER

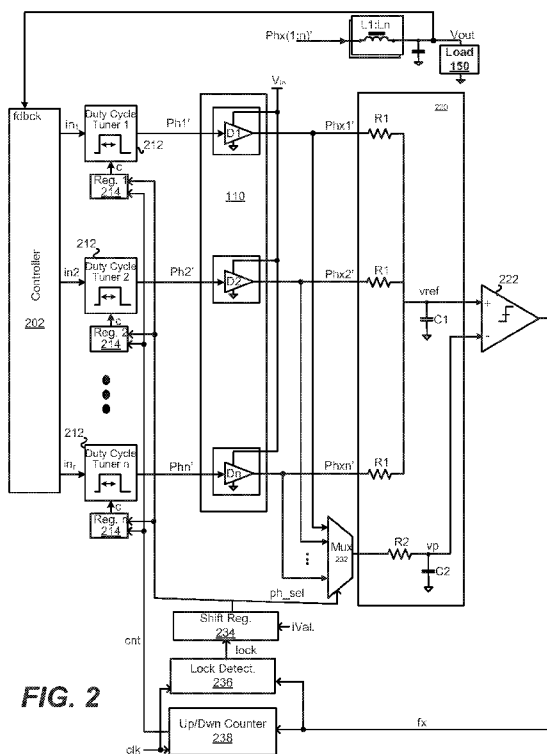


FIG. 2

- (57) Abstract:** In some embodiments described herein, proposed schemes utilize a duty-cycle sensing technique to detect load current imbalance in each individual inductor, and then adjusts the duty cycles for the specific phases through a digital duty cycle tuner.



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EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,

GW, KM, ML, MR, NE, SN, TD, TG).

— *with international search report (Art. 21(3))*

**METHOD AND APPARATUS OF CURRENT BALANCING FOR MULTIPLE
PHASE POWER CONVERTER**

TECHNICAL FIELD

5 The present invention relates generally to power regulators, and in particular, to multi-phase converters with current load balancing.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 shows a conventional multi-phase DC-DC converter.

Figure 2 shows a multi-phase DC-DC converter with load balancing in accordance with some embodiments.

15 **Figure 3** is a timing diagram showing signals from the multi-phase converter of Fig. 2 in accordance with some embodiments.

Figure 4 shows a circuit for a duty cycle tuner in accordance with some embodiments.

Figure 5 shows a multi-phase converter with load balancing and with PFM and PWM phase signal generation in accordance with some embodiments.

20 **Figure 6** shows a chip with multiple VR cells with load balancing in accordance with some embodiment

DETAILED DESCRIPTION

25 Fig. 1 shows a conventional multi-phase switching DC-DC power converter (in this example, a buck converter). The depicted multi-phase converter has a controller 102, bridge 110, and an output section including inductors (L1 to Ln) and a capacitor (C), all coupled together to provide a regulated output voltage (Vout) to a load 150. The bridge 110 includes multiple switch devices (D1 to Dn), each corresponding to a phase of the multi-phase converter and providing current to a corresponding inductor (L1 to Ln) by providing the input voltage (Vin) at the switch device output when the switch is turned on. One or more feedback signals (represented as the “fdbck” signal) are fed back from the output (Vout) to the controller to control the bridge devices (D1 to Dn) to provide more, or less, power to the load in order to regulate Vout at a desired voltage level.

 Multiple-phase switching power converters (such as the depicted voltage regulator of Fig.

1) conduct current through the inductors and capacitor(s) via the switch devices. The duty cycle Pulse train signals with controllable duty cycles are typically applied to the switch devices to control the amounts of current that they provide to their inductors. The time-average current in an inductor is proportional to the duty cycle of the switch device driving the inductor. Accordingly, the amount of current provided to the load, and thus the voltage at the load, can be controlled by controlling the duty cycle of the pulses driving the switch devices.

Typically, multi-phase switching power converters utilize pulse width modulation (PWM) to adjust the duty cycles of the pulse trains accordingly, with each pulse being at a unique phase. One design challenge is to balance the average current driven through the inductor phases, as inductor and other circuit component mismatches can cause unbalanced load currents. In fact, phase current balancing may be particularly important for integrated voltage regulators (multi-phase converters that are part of the same chip as the load to which they supply) since the unbalanced load currents can more readily cause the relatively small inductors to saturate.

In some embodiments described herein, proposed schemes utilize a duty-cycle sensing technique to detect load current imbalance in each individual inductor, and then adjusts the duty cycles for the specific phases through a digital duty cycle tuner.

Figure 2 shows a multi-phase switching converter with load balancing circuits in accordance with some embodiments. A multi-phase switching converter, as illustrated in Fig. 1, is shown, but with additional load balancing circuitry in accordance with some embodiments. The load balancing circuitry generally comprises comparison circuitry and duty cycle tuner circuitry. In the depicted embodiment, the comparison circuitry includes a filter block 220 and a voltage comparator 222. The filter block includes resistors R1 and a capacitor C1, coupled as shown, for providing an average phase leg voltage (v_{ref}) and resistor R2 and capacitor C2 for providing individual phase leg voltages (v_p) from multiplexer 232. A phase leg voltage is a voltage that is proportional to the current in the phase leg, i.e., proportional to the current coming out of the switch device for a given phase.

The voltage (v_{ref}) at C1 is an integration, or average, of all of the switch device output levels ($Phx1'$ to $Phxn'$). The voltage (v_p) at C2 will be the voltage level at a switch device output, as selected by Mux 232. These voltages are essentially DC levels. The resistor and capacitor values for R1, R2, C1, and C2 may be any suitable values to achieve stable, measurable indicative voltages. In some embodiments, the $R1C1$ and $R2C2$ time constants should be sufficiently large, e.g., 100 times the period (T) of the PWM clock, although this is not necessary for practicing the invention. So, for example, if the bridge switches are being driven at a clock frequency of 100 MHz ($T = 10$ nS, then the RC time constants would be greater than 1

μS.) In some embodiments, each phase voltage is compared against the average (v_{ref}) in order to control it, through its duty cycle tuner, to approach (if not equal) the average value, which results in the phase leg currents, in turn, more closely approaching each other and thus, more closely approaching balance with one another. When the selected phx' signal is not equal to v_{ref} , unbalanced load current is sensed (detected). Balancing adjustments are then applied through tuning the duty-cycle of the selected phase signal.

In the depicted embodiment, the duty cycle tuner circuitry comprises: (1) duty cycle tuners 212, with associated control registers 214, for tuning (or offsetting) the duty cycle in each phase, and (2) logic blocks (234, 236, and 238) for setting the duty cycle adjustment in each duty cycle tuner based on the comparisons between the average phase voltage (v_{ref}) and the individual voltages (v_p). It should be appreciated that the logic blocks may be implemented with any suitable digital logic (software, state machines, discrete gates, etc.). The depicted blocks include a shift register 234, a lock detector 236, and an up/down counter 238, coupled together as shown. Counter 238 is an m -bit up-down counter that, for example, may count up when input fx is high and down when input fx is low. Lock detection circuit 236 is designed to sense when v_p is sufficiently close to (if not equal to) v_{ref} .

In operation, the switch devices ($D1$ to D_n) are controlled by multiphase pulse train signals ($Ph1'$ to Phn'), e.g., pulse width modulated rectangular waves. Digital duty cycle tuners 212 are used to alter the duty cycle of a selected phase ($in1$ - inn) signal. A duty-cycle tuner may be any circuit that modifies the duration ratio of switch device "on" (e.g., binary high level) to off (e.g., low level) over a period of an incoming switch device signal. In the depicted embodiment, the duty-cycle ratio is adjusted through an m -bit control (c) input from the control register 214.

Reference is made to both Figs. 2 and 3 for a description of an exemplary duty cycle tuning operation in accordance with some embodiments. Figure 3 is a timing diagram for current sensing for the first 3 phases. $t1$, $t2$ and $t3$ are the time required to balance Phase 1, Phase 2 and Phase 3 load currents, respectively. Other phases would follow similar timing patterns. The duty cycle tuners may be tuned at any time, for example, initially, at start-up or throughout chip operation. The phases are each tuned, one at a time, e.g. beginning with phase 1 and ending with phase n . With this example, initially, register 1 (register 214 for phase 1) and Mux 232 are set to read and select the $phx1$ node. This is done through a default, initial value ($iVal$) signal, which is a preset initial digital value applied to shift register 234. The Mux 232 is used to select one of the incoming Phx inputs. so, with this example, initially it selects $Phx1'$.

Comparator 222 compares v_{ref} (the average phase voltage level) with v_p for the selected phase. The comparator generates a binary signal fx that indicates whether v_p is smaller or greater

than the average voltage (v_{ref}). For example, fx may be '0 if vp is greater than v_{ref} and '1 if vp is less than v_{ref} . If vp is less than v_{ref} , (fx at high state for this example), the counter 238 will count up and in turn, increase the duty-cycle for the selected phase by increasing its control register 214 value. As long as vp is below v_{ref} , the duty-cycle will keep increasing. After one or
5 more cycles, vp will eventually exceed v_{ref} , causing fx to switch, e.g., to a low state. During this low state, the counter counts down and lowers the duty-cycle. This process repeats itself until fx eventually forms a periodic signal (see Fig. 3). It will have a frequency of $clk/2$, where "clk" is a clock signal input to the counter 238 and with a frequency typically less than that of the PWM clock.

10 The lock detector 236 senses this event and then generates a lock signal, as indicated in Fig. 3. For example, as indicated in the timing diagram of Fig. 3, it may "look" for fx toggling between high and low for one or more cycles. When this condition is satisfied, the lock circuit then asserts its output (e.g., to a high state) for a duration of a clock cycle. To make sure fx has entered periodic signal state, lock detect will wait a few cycles before lock signal is asserted.
15 This causes the shift register to advance to the next phase. In turn, this results in the m-bit counter value to be stored in the register 214 for the phase that had just been evaluated. The shift register output (ph_sel) not only enables/disables control registers 214 for a selected phase, but also, it is used to select the input of Mux 232. This overall process is repeated for the remaining phases until the load currents for all phases are suitably balanced with one another.

20 Figure 4 shows a possible circuit for implementing a duty-cycle tuner circuit 212. The circuit comprises an inverter formed from MOS devices $N0$ and $P0$, along with PMOS devices $P1$ through Pn and NMOS devices $N1$ through Nn , all coupled together as shown. It comprises in input (in), output (out), and n-bit control interface ($C1-Cn$). In this embodiment, the P and N devices that are coupled to the control interface are binary weighted such that the least
25 significant bit ($C1$) devices ($P1$, $N1$) are half the strength of the associated $P2$, $N2$ devices, which are half the strength of the associated $P3$, $N3$ devices, and so on. Thus, the higher the digital control value, the stronger the N devices, relative to the P devices, resulting in a decreased duty cycle. This approach is based on current starved topology where the slope of rising and falling edges is proportional to the strengths of the current sources formed from the controllable P and N
30 devices.

Fig. 5 shows a multi-phase converter with load balancing, similar to the circuit of Fig. 2, except that it includes a controller that generates the phase signals with either PWM or PFM (pulsed frequency modulation). PWM typically operates most efficiently for higher load

currents, e.g., 0.5 A and higher. On the other hand, they may be inefficient for smaller current loads. Accordingly, the controller 502 may switch to a PFM mode when the output load current is below a certain threshold (e.g., 0.5 A). In this way, the DC-DC converter of Fig. 5 may operate efficiently over a large current range, e.g., from 1 micro Amp to 2 or 3 Amps.

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Fig. 6 shows a chip or chip package with multiple VR cells 604 with load balancing as discussed herein. The VR cells 604 are integrated into the chip to supply power to a processor block 610 and are managed by a power control module 602. The cells 604 may be ganged together in different combinations to provide one or more different voltage domains with different current sourcing capabilities. In some embodiments, the VR cells 604 are integrated onto the same chip as the processor. The passive output components (inductors, capacitors) may also be integrated into the chip, or chip package (e.g., on the die or in the substrate). Since these inductors may be integrated into the chip, they may have relatively small inductances and thus, be more susceptible to unwanted saturation. Accordingly, current balancing techniques discussed herein may be even more beneficial in such integrated environments.

15

In the preceding description and following claims, the following terms should be construed as follows: The terms “coupled” and “connected,” along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, “connected” is used to indicate that two or more elements are in direct physical or electrical contact with each other. “Coupled” is used to indicate that two or more elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

20

The term “PMOS transistor” refers to a P-type metal oxide semiconductor field effect transistor. Likewise, “NMOS transistor” refers to an N-type metal oxide semiconductor field effect transistor. It should be appreciated that whenever the terms: “MOS transistor”, “NMOS transistor”, or “PMOS transistor” are used, unless otherwise expressly indicated or dictated by the nature of their use, they are being used in an exemplary manner. They encompass the different varieties of MOS devices including devices with different VTs, material types, insulator thicknesses, gate(s) configurations, to mention just a few. Moreover, unless specifically referred to as MOS or the like, the term transistor can include other suitable transistor types, e.g., junction-field-effect transistors, bipolar-junction transistors, metal semiconductor FETs, and various types of three dimensional transistors, MOS or otherwise, known today or not yet developed.

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The invention is not limited to the embodiments described, but can be practiced with

modification and alteration within the spirit and scope of the appended claims. For example, it should be appreciated that the present invention is applicable for use with all types of semiconductor integrated circuit ("IC") chips. Examples of these IC chips include but are not limited to processors, controllers, chip set components, programmable logic arrays (PLA),
5 memory chips, network chips, and the like.

It should also be appreciated that in some of the drawings, signal conductor lines are represented with lines. Some may be thicker, to indicate more constituent signal paths, have a number label, to indicate a number of constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. This, however, should not be construed in a
10 limiting manner. Rather, such added detail may be used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit. Any represented signal lines, whether or not having additional information, may actually comprise one or more signals that may travel in multiple directions and may be implemented with any suitable type of signal scheme, e.g., digital or analog lines implemented with differential pairs, optical fiber lines,
15 and/or single-ended lines.

It should be appreciated that example sizes/models/values/ranges may have been given, although the present invention is not limited to the same. As manufacturing techniques (e.g., photolithography) mature over time, it is expected that devices of smaller size could be manufactured. In addition, well known power/ground connections to IC chips and other
20 components may or may not be shown within the FIGS, for simplicity of illustration and discussion, and so as not to obscure the invention. Further, arrangements may be shown in block diagram form in order to avoid obscuring the invention, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present invention is to be implemented, i.e., such specifics should
25 be well within purview of one skilled in the art. Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the invention, it should be apparent to one skilled in the art that the invention can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. A chip, comprising:

a multi-phase converter having circuitry for balancing phases including

5 comparison circuitry to compare a voltage for a phase to be selected against an average phase voltage; and

a duty cycle tuner for the phase to be selected, the duty cycle tuner to be tuned based on one or more comparisons between a voltage for the phase to be selected and the average phase voltage.

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2. The chip of claim 1, in which the multi-phase converter is coupled to supply power to a processor that is part of the same chip as the multi-phase converter.

3. The chip of claim 2, wherein output inductors for the multi-phase converter are disposed in a
15 die of the chip.

4. The chip of claim 1, in which the comparison circuitry includes a low-pass filter coupled to a switch device for the phase to be selected to provide the voltage for the phase to be selected.

20 5. The chip of claim 4, in which the low-pass filter comprises a resistor and a capacitor.

6. The chip of claim 4, in which the low-pass filter is coupled to a switch device for the phase to be selected through a multiplexer that couples the low-pass filter to other phase switch devices when they are selected.

25

7. The chip of claim 4, in which the comparison circuitry comprises a second low-pass filter having an input coupled to each phase of the multi-phase converter, the second low-pass filter to provide the average phase voltage.

30 8. The chip of claim 1, in which the duty cycle tuner is disposed between a switch device for the phase to be selected and a phase signal output.

9. The chip of claim 8, in which the duty cycle tuner includes a digital current source adjustment to adjust a rise and fall time for a pulse signal from the phase signal output.

10. A multi-phase voltage regulator, comprising:

two or more phase legs each having a duty cycle tuner to be tuned based on a comparison between a voltage for the duty cycle tuner's phase leg and an average voltage for the two or
5 more phase legs.

11. The multi-phase voltage regulator of claim 10, in which the multi-phase regulator is coupled to supply power to a processor that is part of the same chip as the multi-phase regulator.

10 12. The multi-phase voltage regulator of claim 11, wherein output inductors for the multi-phase regulator are disposed in a die of the chip.

13. The multi-phase voltage regulator of claim 10, comprising comparison circuitry to perform the comparison, the circuitry including a low-pass filter coupled to a switch device for the phase
15 leg being tuned to provide a voltage for the comparison.

14. The multi-phase voltage regulator of claim 13, in which the low-pass filter comprises a resistor and a capacitor.

20 15. The multi-phase voltage regulator of claim 13, in which the low-pass filter is coupled to a switch device for the phase leg to be compared through a multiplexer that couples the low-pass filter to other phase switch devices when they are selected.

16. The multi-phase voltage regulator of claim 13, in which the comparison circuitry comprises a
25 second low-pass filter having an input coupled to each phase leg, the second low-pass filter to provide the average phase voltage.

17. The multi-phase voltage regulator of claim 10, in which the duty cycle tuner is disposed between a switch device for the phase leg to be compared and a phase generator output.

30 18. The multi-phase voltage regulator of claim 17, in which the duty cycle tuner includes a digital current source adjustment to adjust a rise and fall time for a pulse signal from the phase signal output.

19. A method comprising:

selecting a phase leg in a multi-phase converter;

comparing a voltage in the phase leg against an average voltage for multiple phase legs of the converter; and

5 adjusting a duty cycle tuner for the phase leg based on the comparing.

20. The method of claim 19, in which there is a separate duty cycle tuner for each phase leg of the converter.

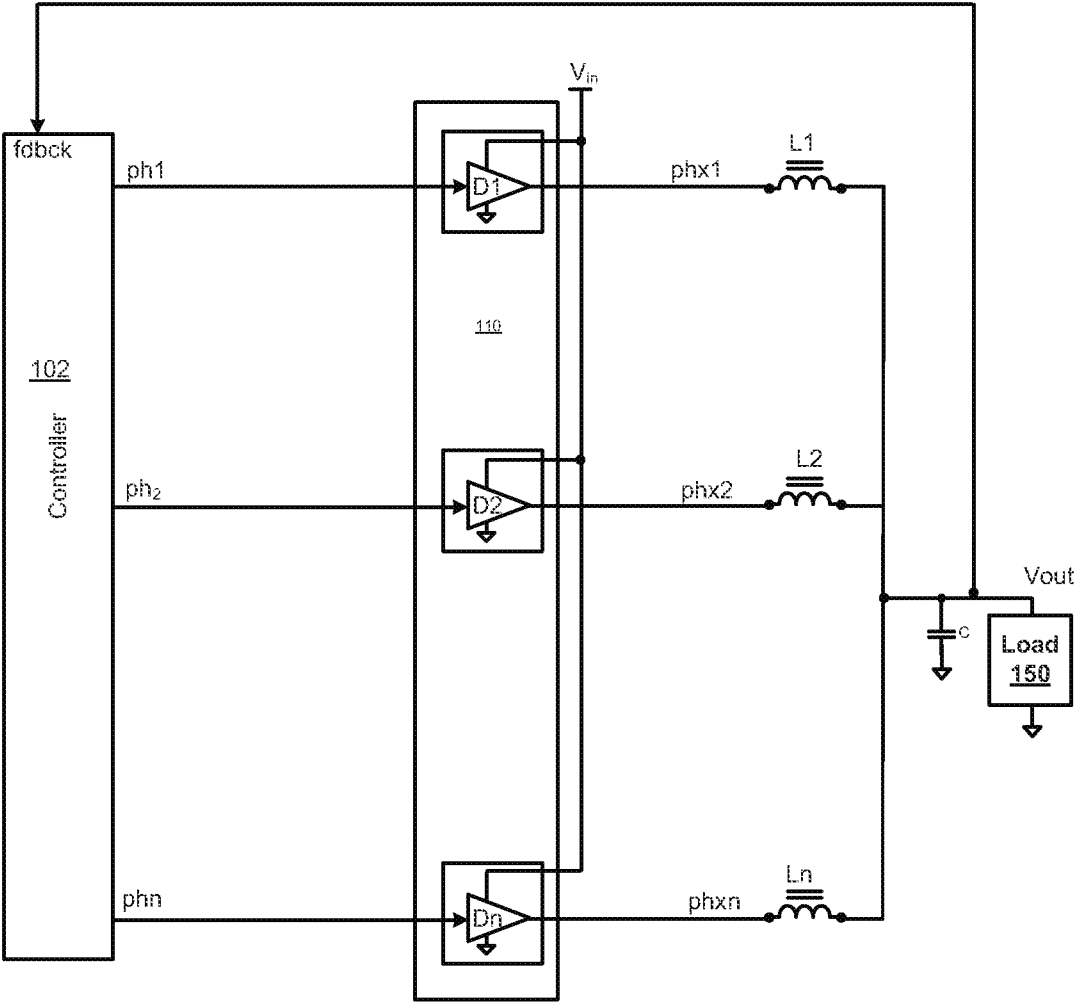
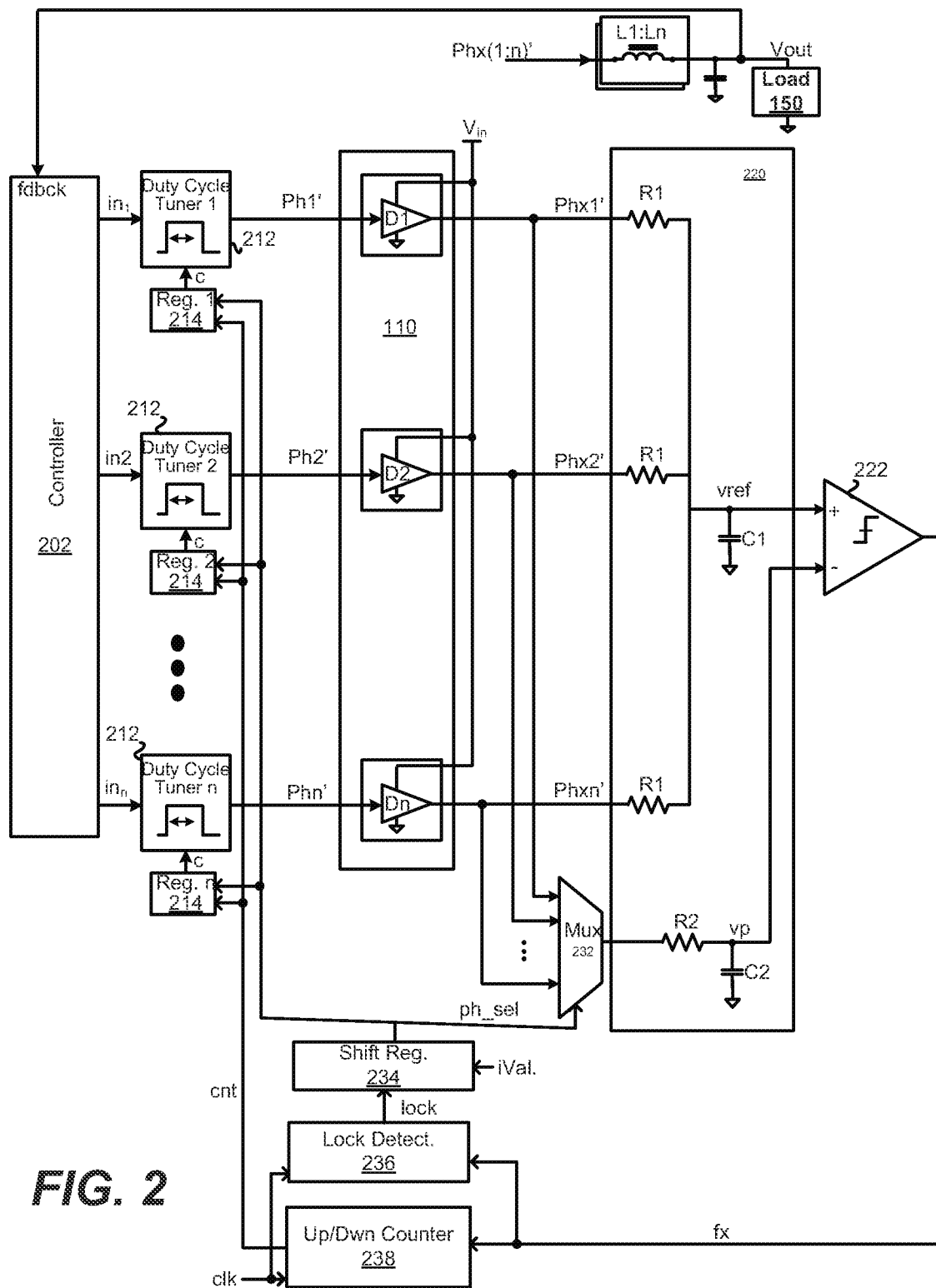


FIG. 1
(PRIOR ART)



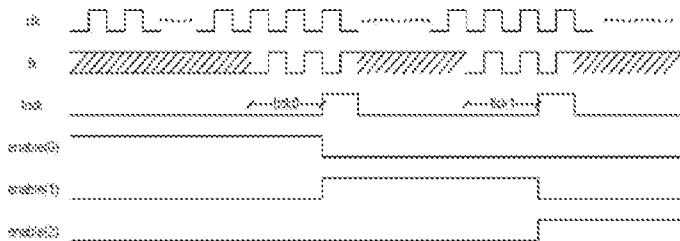


FIG. 3

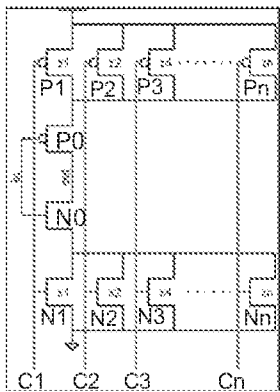


FIG. 4

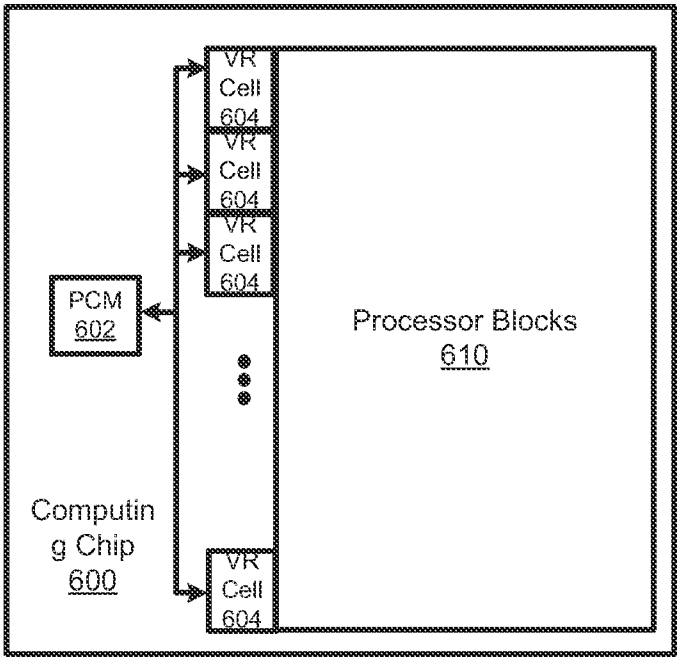


FIG. 6

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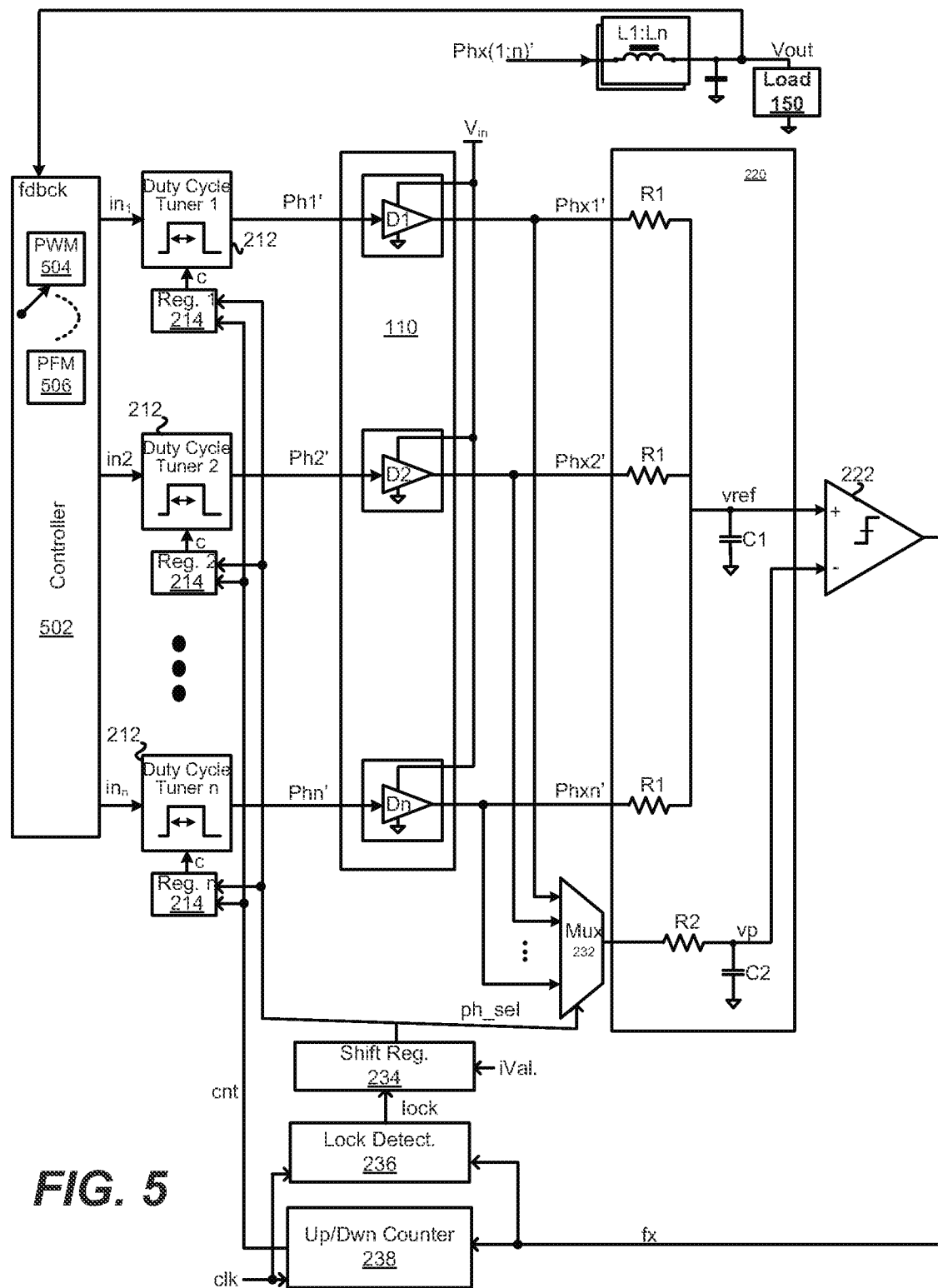


FIG. 5

A. CLASSIFICATION OF SUBJECT MATTER**H02M 3/156(2006.01)i, H02M 3/155(2006.01)i, H02M 1/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 3/156; G05F 1/00; H02M 1/08; H02M 7/519; H02M 1/00; G05F 1/46; H02M 7/527; H03K 5/22; H02M 7/48; H02M 3/155

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: voltage regulator, current balance, PWM, duty, comparing, average, three-phase

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5852554 A (YASUHIRO YAMAMOTO) 22 December 1998	10, 13-14, 17-18
A	See column 6, line 35-column 7, line 65, claims 1, 8 and figures 1, 7.	1-9, 11-12, 15-16, 19-20
Y	US 2011-0267019 A1 (HARISH K. KRISHNAMURTHY et al.) 03 November 2011	10, 13-14, 17-18
A	See paragraphs [0068]-[0070], [0090], claims 1, 18 and figures 7-8.	1-9, 11-12, 15-16, 19-20
A	JP 10-323016 A (FUJI ELECTRIC CO., LTD.) 04 December 1998	1-20
A	See abstract, paragraphs [0019]-[0042] and figures 1-5.	
A	US 2012-0049813 A1 (HUA-CHIANG HUANG et al.) 01 March 2012	1-20
A	See paragraphs [0022]-[0037], claims 1-3 and figures 1-3.	
A	JP 08-331854 A (TOYO ELECTRIC MFG CO., LTD.) 13 December 1996	1-20
A	See abstract, paragraphs [0013]-[0018], claim 1 and figures 1-4.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 September 2013 (26.09.2013)

Date of mailing of the international search report

01 October 2013 (01.10.2013)

Name and mailing address of the ISA/KR

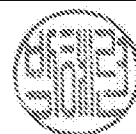
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/048766

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