PATENT SPECIFICATION (11) 1600890

1600890

(21) Application No. 25231/78 (22) Filed 31 May 1978 (19)
(31) Convention Application No. 52/068217 (32) Filed 8 June 1977 in
(33) Japan (JP)
(44) Complete Specification published 21 Oct. 1981
(51) INT. CL.³ H01L 29/78
(52) Index at acceptance
H1K 1CA 1DE 4C11 4C14 4H1A 4H1C 4H3A
9D1 9E 9F 9N2 9R2 DE

(54) SEMICONDUCTOR NON-VOLATILE MEMORY

(71) We, MITSUBISHI DENKI KABUSHIKI KAISHA, of 2—3 Marunouchi 2-chome, Chiyodaku, Tokyo, Japan, a company organized and existing under the laws of Japan,

do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a semiconductor non-volatile memory and more particularly to a floating gate avalanche injection type metal-oxide-semiconductor memory improved in writing characteristic.

Metal-oxide-semiconductor (which is abbreviated to an "MOS") type semiconductor non-volatile memories are sorted into floating gate avalanche injection MOS type memories including the floating gate in each memory cell and the metal-nitride-oxide semiconductor type memories including the gate insulating film having a double layer structure in each memory cell. Those two types of memories are abbreviated to an "FAMOS" and an "MNOS" respectively. In the FAMOS type, the memory cell has an operating mechanism by which a trap for accumulating an electric charge is located in a band of the floating gate, while in the MNOS type the trap is located at a boundary level formed between a pair of electrically insulating films formed of dissimilar materials respectively. The generation of hot carriers for storing information relies upon the avalanche breakdown.

The semiconductor non-volatile memory of the type referred to forms, as a read only memory, (which is abbreviated to an "ROM"), one of those elements composing the microprocessors, microcomputers etc. with the random access memory (which is abbreviated to an "RAM") used for writing and reading and is required to be operative at a higher speed and higher in packing density. In order to attain the high speed operation, it is desirable to increase the conductance of MOS transistors forming the selective gate unit of memories. To this end, it is desirable to decrease both a threshold voltage V_{TH} and a body effect constant K provided that the normalized size effect is considered.

On the other hand, an increase in degree of integration requires both the double layer structure of memory cells and a decrease in spacing formed between the source and drain regions in the MOS structure. If it is attempted to prevent a decrease in punch-through voltage caused by this decrease in source-to-drain spacing then it is required to increase the impurity concentration of semiconductor substrates. However, this increase in impurity concentration gives rise to contradictions since both the body effect K, and the threshold voltage V_{TH} as above described increase to impede the high speed operation.

In order to solve those contradictions, there have been already proposed MOS type semiconductor non-volatile memories including the semiconductor substrate and the semiconductor region for each memory cell identical in conductivity type to and higher in impurity concentration than the semiconductor substrate with a junction formed between that region and a drain region involved. In those MOS semiconductor non-volatile memories, the junction between the high impurity concentration region and the drain region extends outside of an associated gate region and therefore the writing avalanche breakdown current has not much contributed to the storing action as compared with memories not including the high impurity concentration region.

Accordingly, it is an object of the present invention to provide a new and improved semiconductor non-volatile memory capable of attaining both the high speed operation and a high packing density while storing efficiently data with a low writing voltage.

The present invention provides a semicon-

ductor non-volatile semiconductor memory cell comprising a semiconductor layer of one type conductivity, a pair of semiconductor regions of the opposite type conductivity disposed in spaced relationship in the semiconductor layer to form a gate region therebetween, an electrically insulating film disposed on the gate region, and a highly doped, relative to the doping of the semiconductor layer, semiconductor region disposed to form a junction with at least one of the pair of semiconductor regions of the opposite type conductivity, the junction being located only within the gate region, the memory element performing the storing operation by having an electric charge accumulated in the electrically insulating film.

Preferably, a floating gate may be buried in the electrically insulating film and the electric charge is accumulated in the floating gate.

Advantageously, a drain region may be formed of one of the semiconductor regions with the opposite type conductivity forming the junction with the highly doped region, and a source region is formed of the other of the semiconductor regions having the opposite type conductivity.

The present invention will become more readily apparent from the following detailed description taken in conjunction with the accompanying drawing in which:

Figure 1 is a fragmental cross sectional view of a *p* channel FAMOS semiconductor non-volatile memory constructed in accordance with the principles of the prior art;

Figure 2 is a fragmental cross sectional view of a *p* channel FAMOS semiconductor non-volatile memory constructed in accordance with the present invention; and

Figure 3 is a view similar to Figure 2 but illustrating a modification of the present invention.

For a better understanding of the nature of the present invention, a conventional FAMOS semiconductor non-volatile memory will now be described in conjunction with Figure 1 of the drawing. The arrangement illustrated is of a *p* channel MOS transistor structure and comprises an *n* type semiconductor substrate 10, and a pair of p^+ type diffusion regions 12 and 14 disposed in spaced relationship in the surface portion of the substrate 10. In the example illustrated, the diffusion region 12 forms a drain region while the diffusion region 14 forms a source region. The arrangement further comprises an n^+ type avalanche diffusion layer 16 disposed to form a *pn* junction 18 with the p^+ type drain region 12, an electrically insulating film 20 formed, for example, of silicon dioxide and disposed on the surface of the substrate 10, and a polycrystalline silicon gate 22 buried in the electrically insulating film 20 to overlap both diffusion regions 12 and 14.

Then a pair of aluminium wirings 24 are disposed on the electrically insulating film 20 and extend through respective windows disposed in the latter until they are disposed in ohmic contact with the p^+ type diffusion regions 12 and 14.

In this way the basic structure of memory cell has been produced.

The substrate 10 has a low impurity concentration of from 10^{14} to 10^{15} atoms per cubic centimeter for the purpose of decreasing both a threshold voltage V_{TH} and a body effect constant K thereof. This results in a decrease in punch-through voltage but the provision of the n^+ type avalanche diffusion region 18 causes a decrease in writing voltage thereby to operate the arrangement satisfactorily even with a decreased punch-through voltage.

In order to manufacture the arrangement of Figure 1, it is a common practice to form first the n^+ type semiconductor regions 16 in the semiconductor substrate 10 by diffusing selectively an *n* type conductivity impurity, phosphorus into the substrate 10 and then form the source and drain diffusion regions 14 and 12 respectively by diffusing selectively a *p* type conductivity impurity, boron into the substrate 10.

However, in the manufacturing process as above described, the phosphorus in the n^+ type semiconductor region 16 is again diffused into the substrate 10 upon forming the source and drain diffusion regions 14 and 12 respectively and also upon forming the silicaon dioxide films 20 to deepen more the diffusion depth of the n^+ type regions 16 than the source and drain regions 12 and 14 respectively due to the boron as shown in Figure 1. This also attributes to phosphorus having a diffusion coefficient larger than that of boron. As a result, the junction 18 formed between the n^+ type region and the drain region 12 is present not only below the polycrystalline silicon gate 22, that is, in a gate region defined between both regions 12 and 14 but also partly extended under the drain region 12 as shown in Figure 1.

Accordingly, in the arrangement of Figure 1 that portion of the junction 18 located adjacent to the polycrystalline silicon gate 22 to contribute to the storing operation is only one portion of the entire junction. Consequently, a writing avalance breakdown current has not much contributed to the storing operation performed by the memory cell shown in Figure 1.

In view of the abovementioned problem, the present invention has been completed and contemplates to provide a semiconductor non-volatile memory including the junction 18 extending only within the gate region for each memory element to permit for an avalanche breakdown current to contribute

effectively to the storing operation.

Referring now to Figure 2 wherein like reference numerals designate the components identical or corresponding to those shown in Figure 1, there is illustrated one memory cell of a p channel FAMOS semiconductor non-volatile memory constructed in accordance with the principles of the present invention. The arrangement illustrated is different from that shown in Figure 1 only in that in Figure 2 the junction 18 is disposed only within the gate region.

In order to manufacture the memory shown in Figure 2, one main face of an n type silicon layer such as the substrate 10 having an impurity concentration of from 10^{14} to 10^{15} atoms per cubic centimeter is selectively oxidized in a predetermined pattern 4 to expose operative regions thereof to form field oxide films thereon. Then ion implantation technique is used to implant arsenic ions into a predetermined portion of each of operative regions to a depth of 0.2 μm to form the n^+ type region 16 having an impurity concentration of 10^{17} atoms per cubic centimeter.

Following this, a gate oxide film is formed on each of the operative regions in the manner well known in the art and then a polycrystalline silicon gate 22 is formed on that gate oxide film so as to include one portion spreading over the n^+ type region 16.

Thereafter, the silicon gate 22 is used as a mask to diffuse selectively boron into the substrate 10 for form in each of the operative regions a pair of p^+ type source and drain diffusion regions 14 and 12 respectively each having an impurity concentration of from 10^{20} to 10^{22} atoms per cubic centimeter and a diffusion depth of from 1.0 to 1.5 μm.

Subsequently, an oxide film is formed to bury the polycrystalline silicon gate 22 into a unitary structure including the oxide films previously and now formed in the manner well known in the art.

Then aluminum wirings 24 are disposed in pair on the oxide films 20 and also disposed in ohmic contact with the associated source and drain regions 14 and 12 respectively in the manner also well known in art.

It is noted that, upon forming the source and drain regions 14 and 12 respectively and also upon forming the oxide films 20, the n^+ type region 16 is driven but the arsenic located in that region is scarcely diffused into the adjacent portion of the semiconductor layer 10. Thus the depth of the n^+ type region 16 can be shallower than that of the drain region 12. As a result, the junction 18 between both regions 12 and 16 is located only below the polycrystalline silicon gate 22 and in the gate region as shown in Figure 2.

From the foregoing it is seen that in the arrangement of Figure 2 the application of a writing voltage to the drain region 12 causes the avalanche breakdown to be concentrated below the polycrystalline silicon gate 22 with the result that hot electrons generated due to that avalanche breakdown are efficiently accumulated on the polycrystalline silicon gate 22.

In a modification of the present invention shown in Figure 3 wherein like reference numerals designate the components identical or corresponding to those shown in Figure 1 or 2, an n type silicon layer 19 is epitaxially grown on an electrically insulating substrate 34 of sapphire to be about 0.6 μm thick. Then the manufacturing process similar to that above described in conjunction with Figure 2 is repeated with the epitaxially grown semiconductor layer 10 to form an FAMOS semiconductor memory cell as shown in Figure 3.

In the arrangement of Figure 3, the diffusion regions 12, 14 and 16 have a common depth limited by the thickness of the epitaxially grown silicon layer 10. Therefore the junction 18 is formed between the p^+ type drain region 12 and the n^+ type diffusion region 16 below the polycrystalline silicon gate 22 alone even with phosphorus diffused into the semiconductor layer 10 to form the n^+ type region.

From the foregoing it is seen that, in MOS semiconductor non-volatile memories performing the storing operation by accumulating an electric charge in an electrically insulating film portion underlaid with the gate region of each MOS memory cell, the present invention discloses the junction formed between a semiconductor region to which a writing voltage is adapted to be applied and a highly doped region for lowering the writing voltage so as to be only located in a gate region formed between both regions in each memory cell. Therefore the avalanche breakdown current effectively contributes to the storing operation performed by the resulting semiconductor non-volatile memory which is also advantageous in that the writing voltage can be lowered and the efficiency is high.

While the present invention has been illustrated and described in conjunction with a few preferred embodiments thereof it is to be understood that numerous changes and modifications may be resorted to without departing from the scope of the present invention. For example, the present invention is equally applicable to n channel MOS transistor structures and MNOS memories. Also, the semiconductor non-volatile memory of the present invention may be produced by selecting properly a ratio of diffusion concentration between the source and drain diffusion regions and the n^+ type diffusion region to increase the dimension of each of the former regions as compared with the latter region.

WHAT WE CLAIM IS:—

1. A semiconductor non-volatile memory cell comprising a semiconductor layer of one type conductivity, a pair of semiconductor regions of the opposite type conductivity disposed in spaced relationship in said semiconductor layer to form a gate region therebetween, an electrically insulating film disposed on said gate region, and a highly doped, relative to the doping of the semiconductor layer, semiconductor region disposed for form a junction with at least one of said pair of semiconductor regions of the opposite type conductivity, said junction being located only within said gate region, the memory cell performing the storing operation by having an electric charge accumulated in said electrically insulating film.

2. A semiconductor non-volatile memory cell as claim in claim 1 wherein a floating gate is buried in said electrically insulating film and said electric charge is accumulated in said floating gate.

3. A semiconductor non-volatile memory cell as claimed in claim 1 wherein a drain region is formed of one of said semiconductor regions with the opposite type conductivity forming said junction with said highly doped semiconductor region, and a source region is formed of the other of said semiconductor layers having the opposite type conductivity.

4. A semiconductor non-volatile memory cell as claimed in claim 1 wherein said pair of semiconductor regions having the opposite type conductivity are doped with boron and said highly doped semiconductor region includes arsenic.

5. A semiconductor non-volatile memory cell as claimed in claim 1 wherein said semiconductor layer of the one type conductivity is epitaxially grown on a sapphire substrate.

6. A semiconductor non-volatile memory cell substantially as hereinbefore described, with reference to and as illustrated in Figures 2 of 3 the accompanying drawings.

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Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon) Ltd.—1981. Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1600890 COMPLETE SPECIFICATION

1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

FIG. 1 PRIOR ART

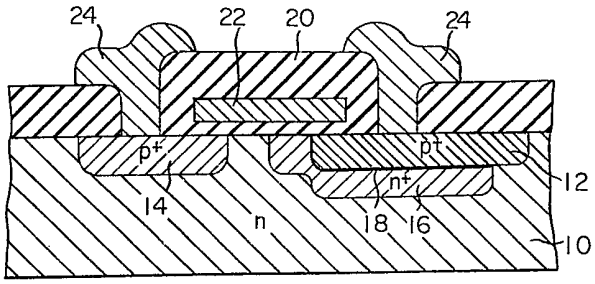

FIG. 2

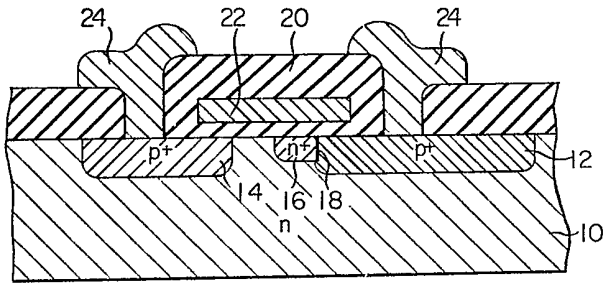

FIG. 3