



US00D409141S

United States Patent [19]
Kashima

[11] **Patent Number: Des. 409,141**
[45] **Date of Patent: ** May 4, 1999**

[54] **ELECTRICAL CIRCUIT SIGNAL EXTRACTOR**

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[75] Inventor: **Isao Kashima**, Tachikawa, Japan

[57] **CLAIM**

[73] Assignee: **Mechano Electronic, Inc.**, Tachikawa, Japan

The ornamental design for electrical circuit signal extractor, as shown and described.

[**] Term: **14 Years**

DESCRIPTION

[21] Appl. No.: **29/079,389**

[22] Filed: **Nov. 13, 1997**

[30] **Foreign Application Priority Data**

Jun. 11, 1997 [JP] Japan 9-57552

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/123; D13/199**

[58] **Field of Search** D13/123, 199;
333/18; 175/40; 348/565

FIG. 1 is a front elevational view of the electrical circuit signal extractor;

FIG. 2 is a rear elevational view thereof;

FIG. 3 is a right hand side elevational view thereof;

FIG. 4 is a left hand side elevational view thereof;

FIG. 5 is a top plan view thereof;

FIG. 6 is a bottom view thereof; and,

FIG. 7 is a perspective view thereof.

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 261,505 10/1981 Miller D13/123

1 Claim, 3 Drawing Sheets

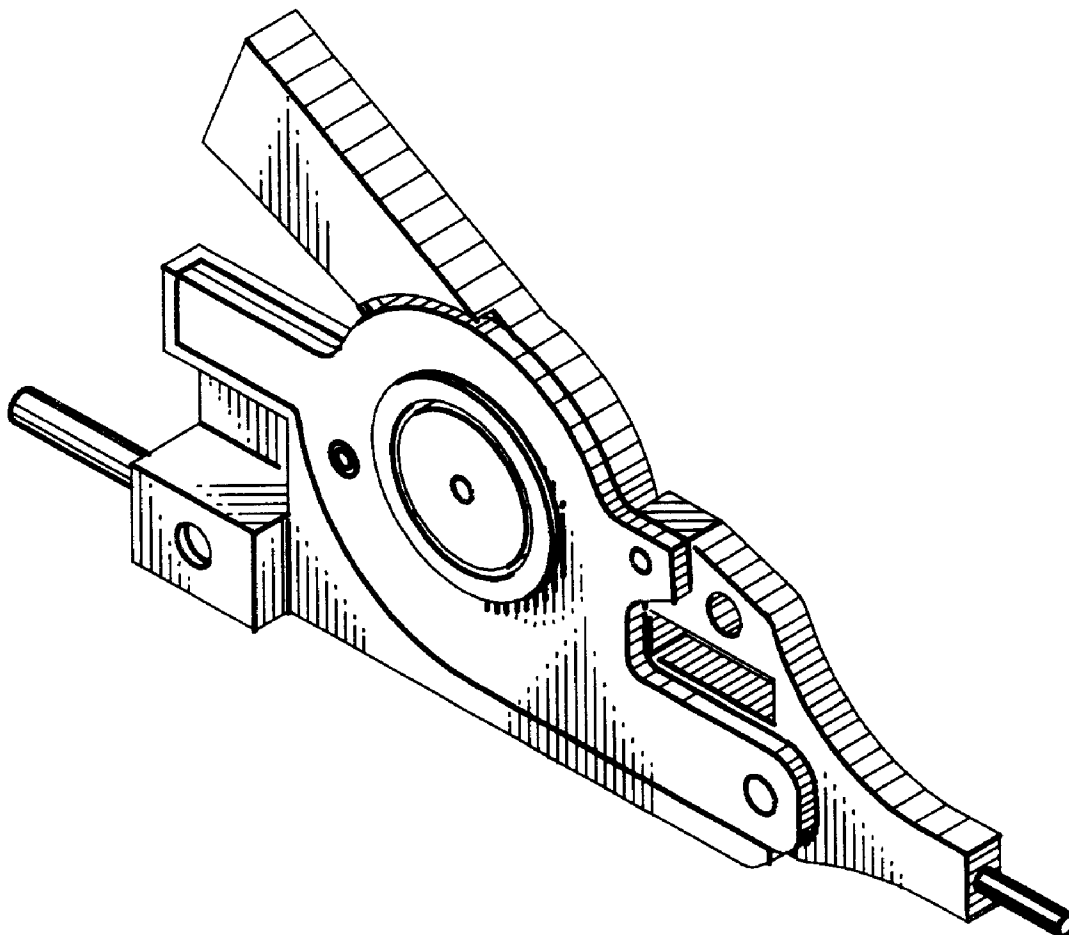


Fig. 1

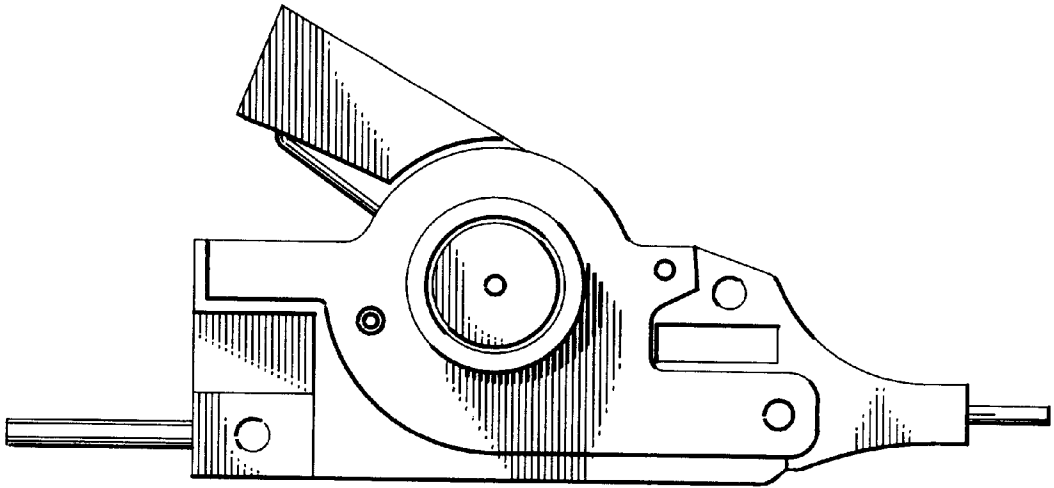


Fig. 2

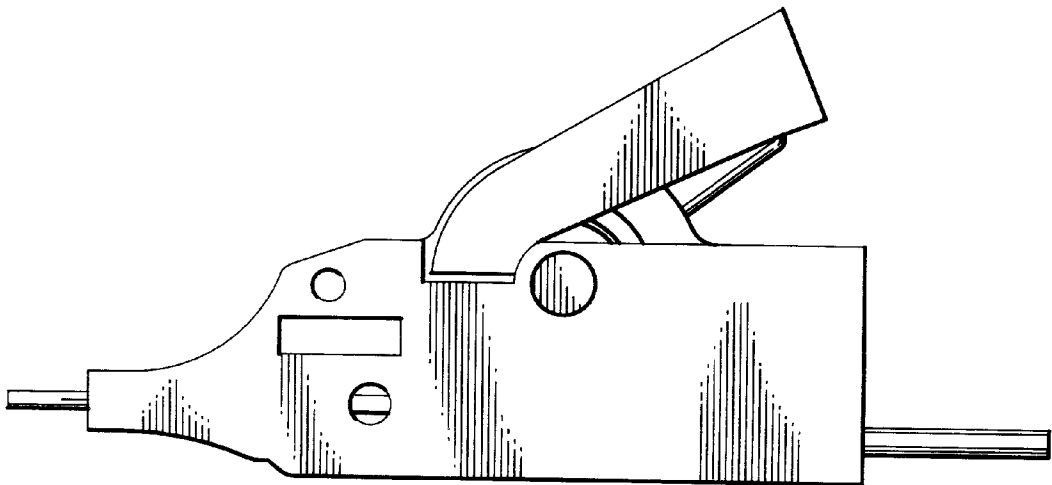


Fig. 4

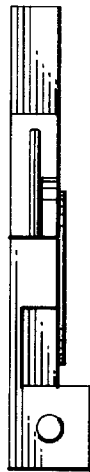


Fig. 3



Fig. 5

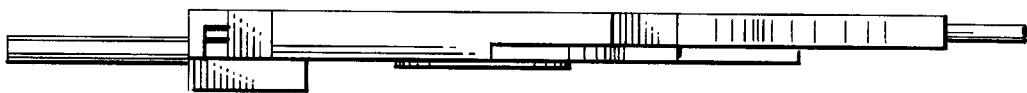


Fig. 6



Fig. 7

