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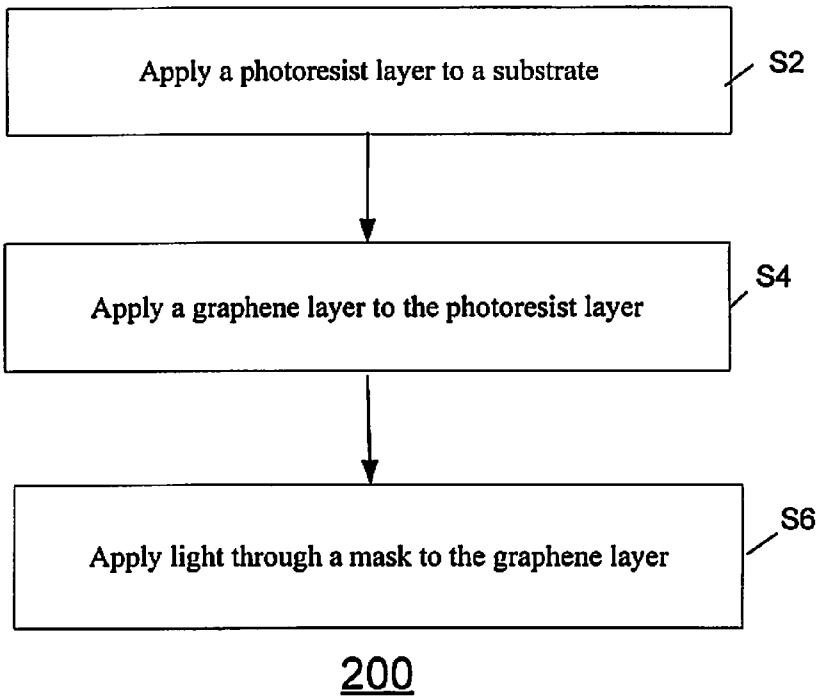
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(54) Title: OPTICAL LITHOGRAPHY USING GRAPHENE CONTRAST ENHANCEMENT LAYER

(57) Abstract: Technologies are generally described for methods, systems, and structures that include patterns formed by optical lithography. In some example methods, a photoresist layer is applied to a substrate, and a graphene layer can be applied to the photoresist layer. Light can be applied through a mask to the graphene layer, where the mask includes a pattern. The light can form the pattern on the graphene layer such that the pattern forms on the photoresist layer.

Fig. 2



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OPTICAL LITHOGRAPHY USING GRAPHENE CONTRAST ENHANCEMENT LAYER

BACKGROUND

[0001] Unless otherwise indicated herein, the materials described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

[0002] In optical lithography, a pattern may be formed on a substrate using a mask. In some examples, a light sensitive photoresist layer may be applied to the substrate. A light source may apply a beam of light to the substrate through the mask. The pattern on the mask may cause the light beam to expose some areas of the photoresist and block other areas of the photoresist from exposure based on the pattern. The photoresist may react to the applied light to form the pattern on the substrate. An optical system may be interposed between the mask and the substrate allowing for changes in a size of the pattern exposed to the photoresist layer.

SUMMARY

[0003] Technologies are generally described for methods, systems and structures that include vias formed by optical lithography.

[0004] In some examples, a method for forming a structure is generally described. Example methods may include applying a photoresist layer on a substrate, and applying a graphene layer on the photoresist layer. In some examples, the method may further include applying light through a mask to the graphene layer, where the mask includes a pattern. The applied light can form the pattern on the graphene layer and such that the pattern forms on the photoresist layer.

[0005] In some examples, a structure is generally described. Example structures may include a substrate with a photoresist layer on the substrate. The structure may further include a graphene layer on the photoresist layer.

[0006] In some examples, a system effective to form a structure is generally described. An example system may include a processor, a light source, a mask, a substrate, a photoresist layer, and a graphene layer. The photoresist layer can be formed on the substrate, with the graphene layer formed on the photoresist layer. The processor can be arranged in communication with the lights source, and configured effective to apply light through the mask to the graphene layer. In some examples, the light is effective to form the pattern on the graphene layer such that the pattern can be formed on the photoresist layer.

[0007] The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE FIGURES

[0008] The foregoing and other features of this disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. Understanding that these drawings depict only several embodiments in accordance with the disclosure and are, therefore, not to be considered limiting of its scope, the disclosure will be described with additional specificity and detail through use of the accompanying drawings, in which:

Fig. 1 illustrates an example system that can be utilized to implement optical lithography using a graphene contrast enhancement layer;

Fig. 2 depicts a flow diagram for an example process for implementing optical lithography using a graphene contrast enhancement layer;

Fig. 3 illustrates a computer program product that can be utilized to implement optical lithography using a graphene contrast enhancement layer; and

Fig. 4 is a block diagram illustrating an example computing device that is arranged to implement optical lithography using a graphene contrast enhancement layer;

all arranged according to at least some embodiments described herein.

DETAILED DESCRIPTION

[0009] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented herein. It will be readily understood that the aspects of the present disclosure, as generally described herein, and illustrated in the Figures, can be arranged, substituted, combined, separated, and designed in a wide variety of different configurations, all of which are explicitly contemplated herein.

[0010] This disclosure is generally drawn, *inter alia*, to systems, methods, materials and apparatus related to optical lithography using a graphene contrast enhancement layer.

[0011] Briefly stated, technologies are generally described for methods, systems, and structures that include patterns formed by optical lithography. In some example methods, a photoresist layer is applied to a substrate, and a graphene layer can be applied to the photoresist layer. Light can be applied through a mask to the graphene layer, where the mask includes a pattern. The light can form the pattern on the graphene layer such that the pattern forms on the photoresist layer.

[0012] It will also be understood that any compound, material or substance which is expressly or implicitly disclosed in the specification and/or recited in a claim as belonging to a group or structurally, compositionally and/or functionally related compounds, materials or substances, includes individual representatives of the group and all combinations thereof.

[0013] Fig. 1 illustrates an example system that can be utilized to implement optical lithography using a graphene contrast enhancement layer, in accordance with at least some embodiments described herein. An example optical lithography system 100 may include a substrate 102, a photoresist layer 104, a graphene layer 106, a light source 110, an optical system 154, and/or a mask 108. At least some of these elements may be arranged in communication with a processor 154 through a

communication link 156. In some examples, processor 154 may be in adapted in communication with a memory 158 that includes instruction 160 stored therein. Processor 154 may be configured (e.g., by instructions 160) to control at least some of the operations described below.

[0014] In some examples, substrate 102 may be a silicon wafer, GaAs, or other semiconductor wafers. As shown at 132 of Fig. 1, photoresist layer 104 may be applied on substrate 102. In various examples, the photoresist layer 104 may be applied by spin coating as shown at 166 or by some other method. As shown at 134, a graphene layer 106 may be applied on photoresist layer 104. The graphene layer 106 may be made of a graphene crystal of a width and length substantially matching photoresist layer 104. The graphene layer 106 may have a height of about one atom. In some examples, two or more graphene layers 106 may be used.

[0015] Graphene layer 106 may be applied on photoresist layer 104 in many ways. In some examples, as shown at 145, graphene layer 106 may be grown on a copper layer 150. Copper layer 150 may be inserted into a quartz tube 156 and heated to about 1000 degrees Celsius with flowing viscosity of 8 s.c.c.m (standard cubic centimeters per minute) H_2 at 90 mtorr. Thereafter, copper layer 150 may be annealed for about 30 minutes at a similar flow rate and pressure. A gas mixture of CH_4 and H_2 may then be flowed at about 460 mtorr with rates of about 24 s.c.c.m. and about 8 s.c.c.m for about 30 minutes, respectively. Copper layer 150 may then be cooled with flowing H_2 at about 10 degrees Celsius per second at a pressure of about 90 mtorr, thereby forming graphene layer 106.

[0016] As shown at 142, copper layer 150 may be attached to a polymer layer 146 such as with rollers 159,161. Copper layer 150 may then be dissolved and the combination of polymer layer 146 and graphene layer 106 may be rolled on to photoresist layer 104 using rollers 158, 160. In some examples, rollers 158, 159, 160, 161 may be in arranged in communication with processor 154. Thereafter, polymer layer 146 may be dissolved leaving graphene layer 106 applied on photoresist layer 104.

[0017] As shown at 136, in some examples, after application of graphene layer 106, the light source 110 may be configured to apply a light beam 112 to mask

108. Based on a pattern 152 on mask 108, at least some photons of light beam 112 may pass through mask 108, through optical system 154 and to graphene layer 106. In some examples, light source 110 may be configured to output light with a power greater than about $3mW/cm^2$. Mask 108 can be configured to block some photons of light beam 112 and allow other photons of light beam 112 to pass through based on pattern 152. In some examples, optical system 154 may be configured to refract light beam 112 to allow for a change in magnification of pattern 152 from mask 108 to graphene layer 106 and photoresist layer 104. Mask 108 and substrate 102 may be placed on respective tables 162, 164. In some examples, tables 162, 164 may be arranged in communication with processor 154 and may be movable with respect to each other.

[0018] As shown at 138, graphene layer 106 can receive photons from light beam 112, based on pattern 152, and allows photons to pass through thereby transmitting photonic energy to exposed graphene layer 116 in the desired pattern from mask 108. In these examples, when photonic energy from light beam 112 passes through graphene layer 106, photons from light beam 112 may expose the photoresist layer 104 resulting in a patterned photoresist layer 114 based on pattern 152. A structure may be formed including substrate 102, patterned photoresist layer 114 and exposed graphene layer 106.

[0019] As shown at 140, exposed graphene layer 116 may be removed from patterned photoresist layer 114. In some examples, the exposed graphene layer 16 may be removed using a dry etching technique such as through the application of an oxygen plasma 168. In some additional examples, photoresist layer 114 may include a silylating agent and may be compatible with such a dry etching technique.

[0020] Graphene layer 106 may be a saturable absorbing material so that, in examples where energy greater than a threshold is applied to graphene layer 106, the applied energy may pass through graphene layer 106. In some examples, graphene layer 106 may have a relatively low bandgap of approximately 0.1 EV so that virtually all photonic energy from light beam 112 passes through the graphene layer 106 to the photoresist layer 104.

[0021] In some examples, graphene layer 106 may be effective to enhance a contrast of images patterned on photoresist 114 by sharpening peaks of light (e.g., photonic energy) passing through the graphene. For example, graphene layer 106 may be effective to provide sharp edge transitions on patterned photoresist layer 114 based on pattern 152 on mask 108 resulting in sharp transparent or opaque areas matching pattern 152.

[0022] Among other benefits, a system arranged in accordance with the present disclosure may be used with light sources with a wide variety of wavelengths. Example light sources may have wavelengths of about 193nm, about 157nm, and about 12nm could be used. A system configured in accordance with the present disclosure may be used to enhance resolution of various features patterned on a substrate allowing for patterning of clear features of various sizes. The graphene layer may have a relatively small height. In some examples, the layer may be one atom in height. Graphene layer 106 may be reversible in that the layer can be used multiple times in multiple applications of light to a photoresist layer.

[0023] As the graphene layer may absorb incident light (i.e., absorb photons), the graphene layer may function as a top antireflective layer. Such an antireflective layer may inhibit light incident on the graphene layer from reflecting back into an optical system. Such a reflection may undesirably result in a double exposure of a photoresist layer.

[0024] Fig. 2 depicts a flow diagram for an example process 200 for implementing optical lithography using graphene as a contrast enhancement layer, arranged in accordance with at least some embodiments described herein. The process in Fig. 2 could be implemented using, for example, system 100 discussed above. An example process may include one or more operations, actions, or functions as illustrated by one or more of blocks S2, S4 and/or S6. Although illustrated as discrete blocks, various blocks may be divided into additional blocks, combined into fewer blocks, or eliminated, depending on the desired implementation. Process 200 may begin at block S2, "apply a photoresist to a substrate."

[0025] At block S2, a photoresist layer may be applied on a substrate. In some examples, the photoresist layer may be applied by pouring the photoresist on the

substrate and spinning the substrate to cause the photoresist to coat the substrate. Processing may continue from block S2 to block S4, "apply a graphene layer to the photoresist layer."

[0026] At block S4, a graphene layer may be applied on the photoresist layer. In some examples, the graphene layer may be applied by rolling the photoresist layer using rollers. Processing may continue from block S4 to block S6, "apply light through a mask to the graphene layer."

[0027] At block S6, light may be applied through a mask to the graphene layer. In some examples, the light may be applied by a laser. The mask may include a pattern. By applying the light to the mask, a pattern of light can be transmitted through the graphene layer to expose the photoresist layer with the desired pattern.

[0028] Fig. 3 illustrates a computer program product that can be utilized to implement optical lithography using a graphene contrast enhancement layer, in accordance with at least some embodiments described herein. Program product 300 may include a signal bearing medium 302. Signal bearing medium 302 may include one or more instructions 304 that, when executed by, for example, a processor, may provide the functionality described above with respect to Figs. 1-2. Thus, for example, referring to system 100, processor 154 may undertake one or more of the blocks shown in Fig. 3 in response to instructions 304 conveyed to the system 100 by medium 302.

[0029] In some implementations, signal bearing medium 302 may encompass a computer-readable medium 306, such as, but not limited to, a hard disk drive, a Compact Disc (CD), a Digital Video Disk (DVD), a digital tape, memory, etc. In some implementations, signal bearing medium 302 may encompass a recordable medium 308, such as, but not limited to, memory, read/write (R/W) CDs, R/W DVDs, etc. In some implementations, signal bearing medium 302 may encompass a communications medium 310, such as, but not limited to, a digital and/or an analog communication medium (e.g., a fiber optic cable, a waveguide, a wired communications link, a wireless communication link, etc.). Thus, for example, program product 300 may be conveyed to one or more modules of the system 100 by an RF signal bearing medium 302, where the signal bearing medium 302 is conveyed

by a wireless communications medium 310 (e.g., a wireless communications medium conforming with the IEEE 802.11 standard).

[0030] Fig. 4 is a block diagram illustrating an example computing device that is arranged to implement optical lithography using a graphene contrast enhancement layer according to at least some embodiments described herein. In a very basic configuration 402, computing device 400 typically includes one or more processors 404 and a system memory 406. A memory bus 408 may be used for communicating between processor 404 and system memory 406.

[0031] Depending on the desired configuration, processor 404 may be of any type including but not limited to a microprocessor (μP), a microcontroller (μC), a digital signal processor (DSP), or any combination thereof. Processor 404 may include one more levels of caching, such as a level one cache 410 and a level two cache 412, a processor core 414, and registers 416. An example processor core 414 may include an arithmetic logic unit (ALU), a floating point unit (FPU), a digital signal processing core (DSP Core), or any combination thereof. An example memory controller 418 may also be used with processor 404, or in some implementations memory controller 418 may be an internal part of processor 404.

[0032] Depending on the desired configuration, system memory 406 may be of any type including but not limited to volatile memory (such as RAM), non-volatile memory (such as ROM, flash memory, etc.) or any combination thereof. System memory 406 may include an operating system 420, one or more applications 422, and program data 424. Application 422 may include an optical lithography using a graphene contrast enhancement layer algorithm 426 that is arranged to perform the functions as described herein including those described with respect to system 100 of Figs 1-3. Program data 424 may include optical lithography using a graphene contrast enhancement layer data 428 that may be useful for implementing optical lithography using a graphene contrast enhancement layer as is described herein. In some embodiments, application 422 may be arranged to operate with program data 424 on operating system 420 such that implementing optical lithography using a graphene contrast enhancement layer may be provided. This described basic

configuration 402 is illustrated in Fig. 4 by those components within the inner dashed line.

[0033] Computing device 400 may have additional features or functionality, and additional interfaces to facilitate communications between basic configuration 402 and any required devices and interfaces. For example, a bus/interface controller 430 may be used to facilitate communications between basic configuration 402 and one or more data storage devices 432 via a storage interface bus 434. Data storage devices 432 may be removable storage devices 436, non-removable storage devices 438, or a combination thereof. Examples of removable storage and non-removable storage devices include magnetic disk devices such as flexible disk drives and hard-disk drives (HDD), optical disk drives such as compact disk (CD) drives or digital versatile disk (DVD) drives, solid state drives (SSD), and tape drives to name a few. Example computer storage media may include volatile and nonvolatile, removable and non-removable media implemented in any method or technology for storage of information, such as computer readable instructions, data structures, program modules, or other data.

[0034] System memory 406, removable storage devices 436 and non-removable storage devices 438 are examples of computer storage media. Computer storage media includes, but is not limited to, RAM, ROM, EEPROM, flash memory or other memory technology, CD-ROM, digital versatile disks (DVD) or other optical storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other medium which may be used to store the desired information and which may be accessed by computing device 400. Any such computer storage media may be part of computing device 400.

[0035] Computing device 400 may also include an interface bus 440 for facilitating communication from various interface devices (e.g., output devices 442, peripheral interfaces 444, and communication devices 446) to basic configuration 402 via bus/interface controller 430. Example output devices 442 include a graphics processing unit 448 and an audio processing unit 450, which may be configured to communicate to various external devices such as a display or speakers via one or more A/V ports 452. Example peripheral interfaces 444 include a serial interface

controller 454 or a parallel interface controller 456, which may be configured to communicate with external devices such as input devices (e.g., keyboard, mouse, pen, voice input device, touch input device, etc.) or other peripheral devices (e.g., printer, scanner, etc.) via one or more I/O ports 458. An example communication device 446 includes a network controller 460, which may be arranged to facilitate communications with one or more other computing devices 462 over a network communication link via one or more communication ports 464.

[0036] The network communication link may be one example of a communication media. Communication media may typically be embodied by computer readable instructions, data structures, program modules, or other data in a modulated data signal, such as a carrier wave or other transport mechanism, and may include any information delivery media. A "modulated data signal" may be a signal that has one or more of its characteristics set or changed in such a manner as to encode information in the signal. By way of example, and not limitation, communication media may include wired media such as a wired network or direct-wired connection, and wireless media such as acoustic, radio frequency (RF), microwave, infrared (IR) and other wireless media. The term computer readable media as used herein may include both storage media and communication media.

[0037] Computing device 400 may be implemented as a portion of a small-form factor portable (or mobile) electronic device such as a cell phone, a personal data assistant (PDA), a personal media player device, a wireless web-watch device, a personal headset device, an application specific device, or a hybrid device that include any of the above functions. Computing device 400 may also be implemented as a personal computer including both laptop computer and non-laptop computer configurations.

[0038] The present disclosure is not to be limited in terms of the particular embodiments described in this application, which are intended as illustrations of various aspects. Many modifications and variations can be made without departing from its spirit and scope, as will be apparent to those skilled in the art. Functionally equivalent methods and apparatuses within the scope of the disclosure, in addition to those enumerated herein, will be apparent to those skilled in the art from the

foregoing descriptions. Such modifications and variations are intended to fall within the scope of the appended claims. The present disclosure is to be limited only by the terms of the appended claims, along with the full scope of equivalents to which such claims are entitled. It is to be understood that this disclosure is not limited to particular methods, reagents, compounds compositions or biological systems, which can, of course, vary. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only, and is not intended to be limiting.

[0039] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[0040] It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (*e.g.*, bodies of the appended claims) are generally intended as "open" terms (*e.g.*, the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to embodiments containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (*e.g.*, "a" and/or "an" should be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is

explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number (*e.g.*, the bare recitation of "two recitations," without other modifiers, means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (*e.g.*, " a system having at least one of A, B, and C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). In those instances where a convention analogous to "at least one of A, B, or C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (*e.g.*, " a system having at least one of A, B, or C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" will be understood to include the possibilities of "A" or "B" or "A and B."

[0041] In addition, where features or aspects of the disclosure are described in terms of Markush groups, those skilled in the art will recognize that the disclosure is also thereby described in terms of any individual member or subgroup of members of the Markush group.

[0042] As will be understood by one skilled in the art, for any and all purposes, such as in terms of providing a written description, all ranges disclosed herein also encompass any and all possible subranges and combinations of subranges thereof. Any listed range can be easily recognized as sufficiently describing and enabling the same range being broken down into at least equal halves, thirds, quarters, fifths, tenths, etc. As a non-limiting example, each range discussed herein can be readily broken down into a lower third, middle third and upper third, etc. As will also be understood by one skilled in the art all language such as "up to," "at least,"

"greater than," "less than," and the like include the number recited and refer to ranges which can be subsequently broken down into subranges as discussed above. Finally, as will be understood by one skilled in the art, a range includes each individual member. Thus, for example, a group having 1-3 cells refers to groups having 1, 2, or 3 cells. Similarly, a group having 1-5 cells refers to groups having 1, 2, 3, 4, or 5 cells, and so forth.

[0043] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

CLAIMS

What is claimed is:

1. A method for forming a structure, the method comprising:

applying a photoresist layer on a substrate;

applying a graphene layer on the photoresist layer;

applying light through a mask to the graphene layer, wherein the mask includes a pattern and wherein applying the light forms the pattern on the photoresist layer through the graphene layer.

2. The method as recited in claim 1, further comprising removing the graphene layer from the photoresist layer after applying light through the mask.

3. The method as recited in claim 2, further comprising removing the graphene layer using a dry etching technique.

4. The method as recited in claim 3, further comprising removing the graphene layer by exposing the graphene layer to an oxygen plasma.

5. The method as recited in claim 1, wherein applying the photoresist layer to the substrate comprises applying the photoresist layer to a silicon substrate.

6. The method as recited in claim 1, further comprising:

applying light through an other mask to the graphene layer, wherein the other mask includes an other pattern and wherein applying the light forms the other pattern on the photoresist layer through the graphene layer.

7. The method as recited in claim 1, wherein applying the graphene layer to the photoresist layer comprises rolling the graphene layer on the photoresist layer.

8. The method as recited in claim 1, wherein applying the photoresist layer to the substrate comprises spin coating the photoresist layer on the substrate.

9. The method as recited in claim 1, wherein applying light through the mask to the graphene layer further comprises applying light having a wavelength of about 157nm through the mask to the graphene layer.

10. A structure comprising:
a substrate;
a photoresist layer on the substrate; and
a graphene layer on the photoresist layer.

11. The structure as recited in claim 10, wherein the substrate includes a silylating agent.

12. The structure as recited in claim 10, wherein:
the graphene layer has a first width and a first length;
the photoresist layer has a second width and a second length;
the first width is substantially equal to the second width; and
the first length is substantially equal to the second length.

13. The structure as recited in claim 12, wherein the graphene layer has a height of about one atom.

14. A system effective to form a structure, the system comprising:
a processor;
a light source arranged in communication with the processor;
a mask, wherein the mask includes a pattern;
a substrate;
a photoresist layer on the substrate; and
a graphene layer on the photoresist layer;

wherein the processor is configured effective to apply light through the mask to the graphene layer, wherein the light is effective to form the pattern on the photoresist layer though the graphene layer.

15. The system as recited in claim 14, further comprising an optical system disposed between the mask and the graphene layer, wherein the optical system is configured effective to refract the light and change a magnification of the pattern between the mask and the substrate.

16. The system as recited in claim 14, further comprising:

a first table, wherein the mask is disposed on the first table;

a second table, wherein the substrate is disposed on the second table; and

wherein the first table is movable with respect to the second table.

17. The system as recited in claim 16, wherein:

the processor is arranged in communication with the first table and the second table; and

the processor is configured effective to control the first table to move with respect to the second table.

18. The system as recited in claim 14, wherein the light source is effective to output light with a wavelength of about 157nm.

19. The system as recited in claim 15, wherein the photoresist includes a silylating agent.

20. The system as recited in claim 15, wherein:

the graphene layer has a first width and a first length;

the photoresist layer has a second width and a second length;

the first width is substantially equal to the second width;

the first length is substantially equal to the second length; and

the graphene layer has a height of about one atom.

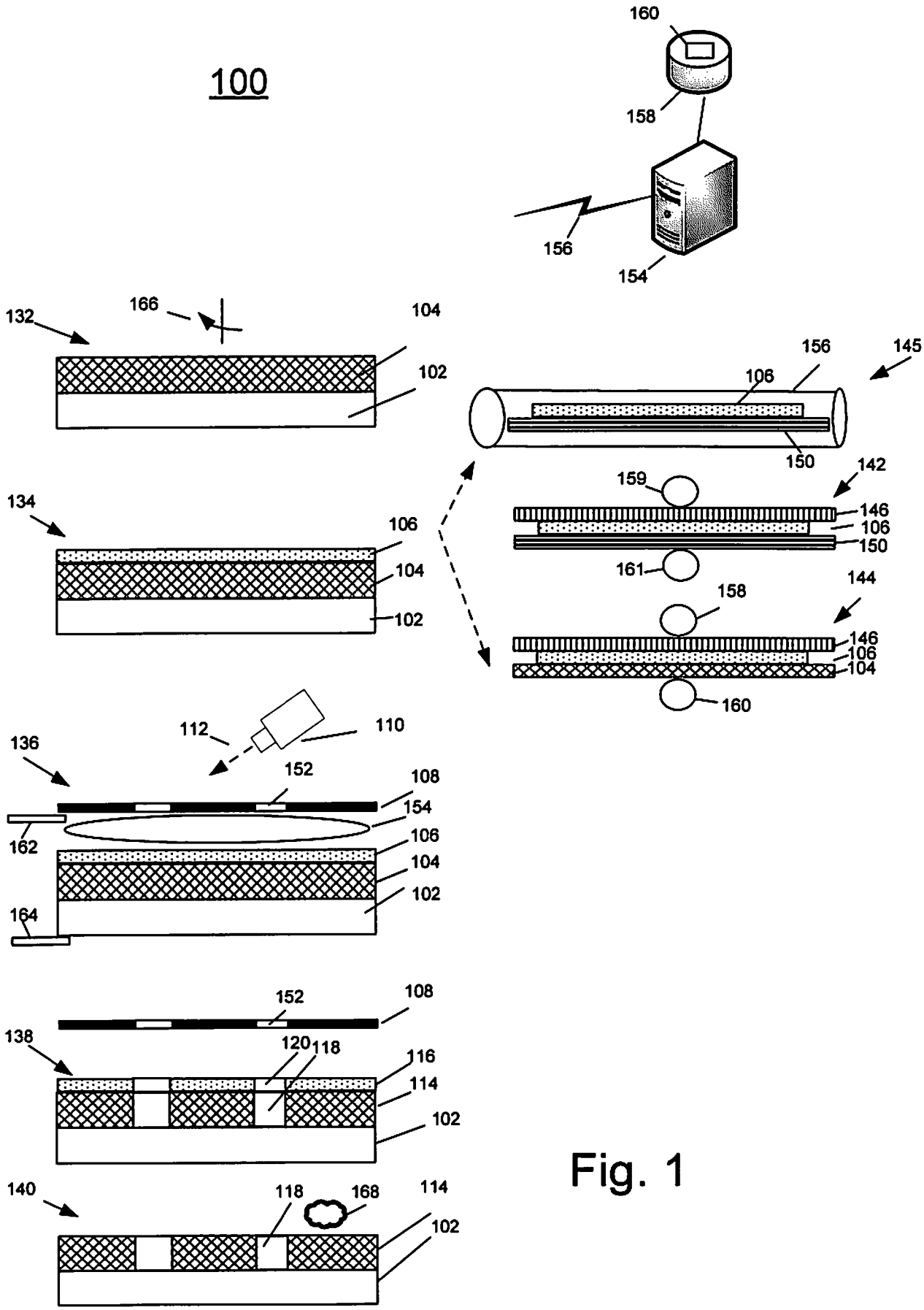

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Fig. 1

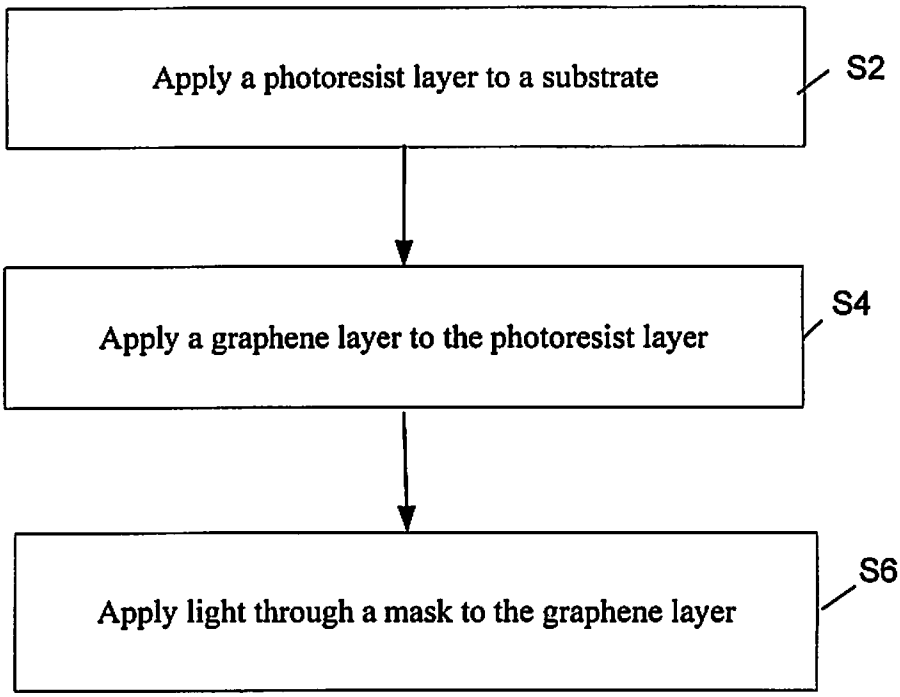

Apply a photoresist layer to a substrate
S2
Apply a graphene layer to the photoresist layer
S4
Apply light through a mask to the graphene layer
S6

Fig. 2

200

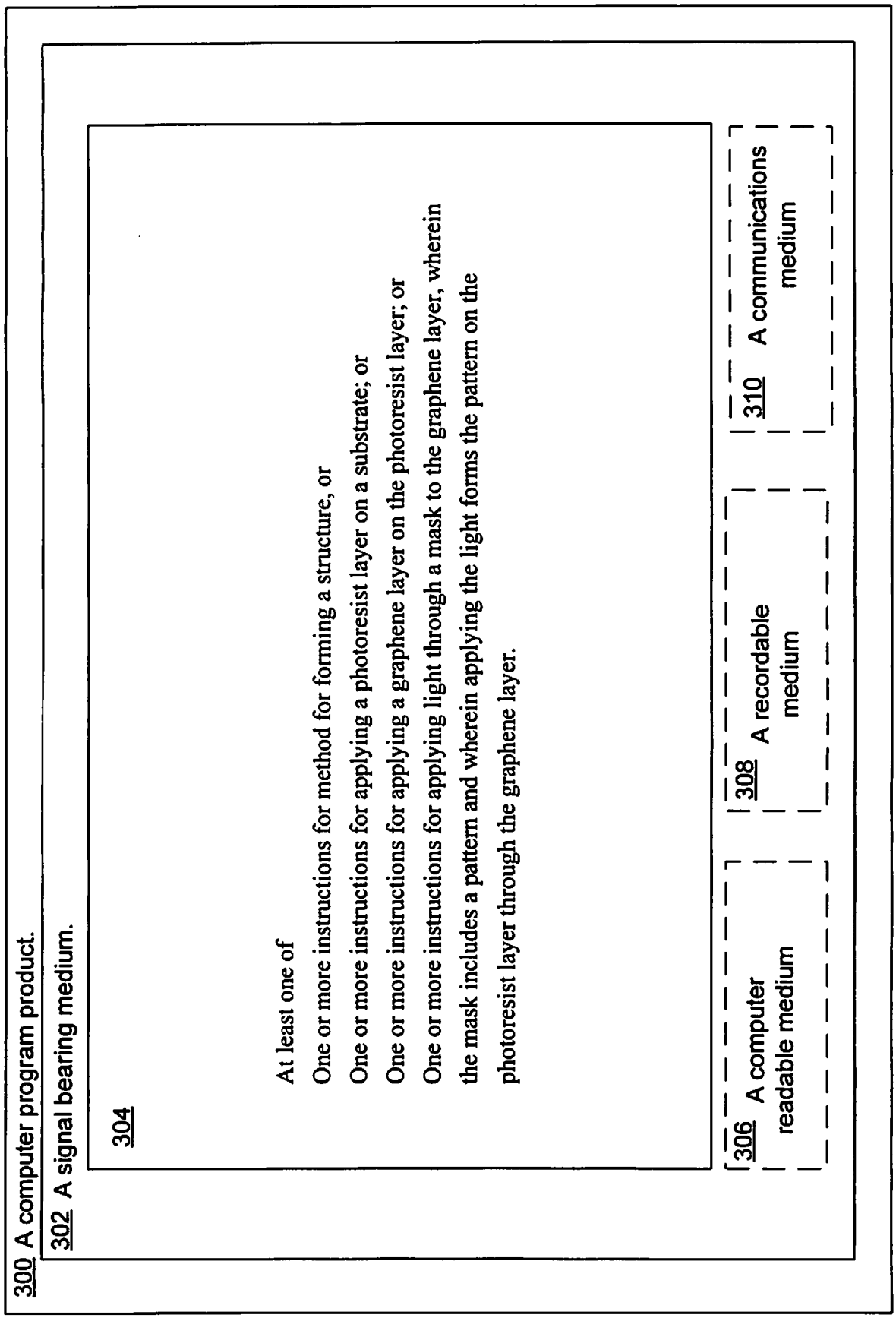
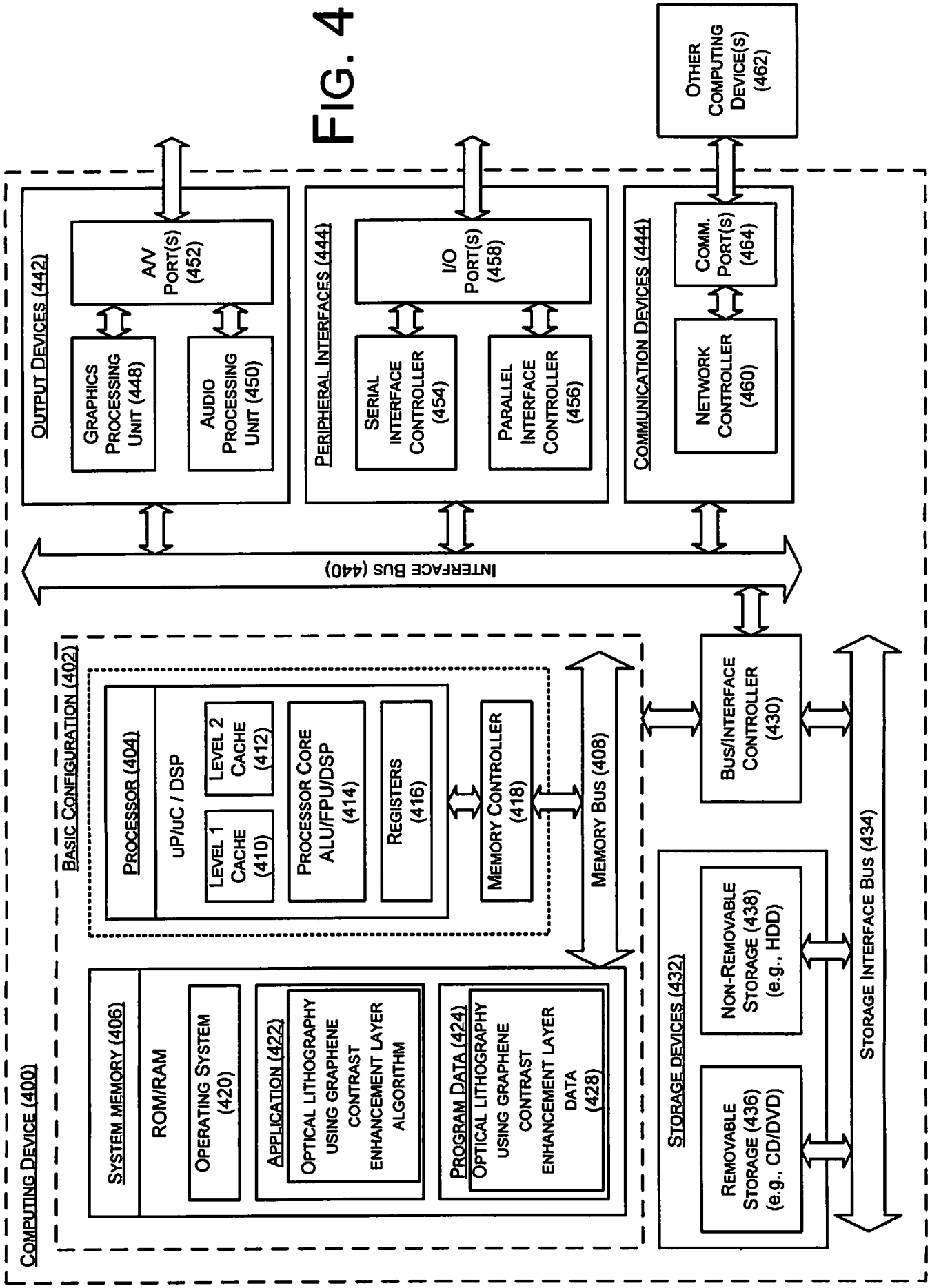

300 A computer program product.
302 A signal bearing medium.
304
At least one of
One or more instructions for method for forming a structure, or
One or more instructions for applying a photoresist layer on a substrate; or
One or more instructions for applying a graphene layer on the photoresist layer; or
One or more instructions for applying light through a mask to the graphene layer, wherein the mask includes a pattern and wherein applying the light forms the pattern on the photoresist layer through the graphene layer.
306 A computer readable medium
308 A recordable medium
310 A communications medium

Fig. 3

FIG. 4


COMPUTING DEVICE (400)
BASIC CONFIGURATION (402)
PROCESSOR (404)
UP/UC / DSP
LEVEL 1 CACHE (410)
LEVEL 2 CACHE (412)
PROCESSOR CORE ALU/FPU/DSP (414)
REGISTERS (416)
MEMORY CONTROLLER (418)
SYSTEM MEMORY (406)
ROM/RAM
OPERATING SYSTEM (420)
APPLICATION (422)
OPTICAL LITHOGRAPHY USING GRAPHENE CONTRAST ENHANCEMENT LAYER ALGORITHM
PROGRAM DATA (424)
OPTICAL LITHOGRAPHY USING GRAPHENE CONTRAST ENHANCEMENT LAYER DATA (428)
MEMORY BUS (408)
BUS/INTERFACE CONTROLLER (430)
STORAGE DEVICES (432)
REMOVABLE STORAGE (436) (e.g., CD/DVD)
NON-REMOVABLE STORAGE (438) (e.g., HDD)
STORAGE INTERFACE BUS (434)
INTERFACE BUS (440)
OUTPUT DEVICES (442)
GRAPHICS PROCESSING UNIT (448)
AUDIO PROCESSING UNIT (450)
A/V PORT(S) (452)
PERIPHERAL INTERFACES (444)
SERIAL INTERFACE CONTROLLER (454)
PARALLEL INTERFACE CONTROLLER (456)
I/O PORT(S) (458)
COMMUNICATION DEVICES (444)
NETWORK CONTROLLER (460)
COMM. PORT(S) (464)
OTHER COMPUTING DEVICE(S) (462)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/050668

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

G03F 7/00 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
wpi, epodoc and inspec using keywords: graphene, +lithograph+, photoresist, contrast, anti_reflect, resolution, sharp, enhance, improve and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0308520 A1 (SHIN et al.) 17 December 2009 Figures 3, 6; Paragraphs [0006], [0019], [0035], [0037], [0042], [0071-0072], [0078-0082]; Claim 6	10-13

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 November 2010	8 NOV 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **ANDREW WALKER** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3676

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/US2010/050668**

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Member				
US	2009308520	JP	2009298683	KR	20090129176

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX