Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

CA 2218373 C 2007/08/21

(11)(21) 2 218 373

(12) BREVET CANADIEN
CANADIAN PATENT

(13) C

(86) Date de dépôt PCT/PCT Filing Date: 1996/04/18
(87) Date publication PCT/PCT Publication Date: 1996/10/24
(45) Date de délivrance/Issue Date: 2007/08/21
(85) Entrée phase nationale/National Entry: 1997/10/16
(86) N° demande PCT/PCT Application No.: CA 1996/000248
(87) N° publication PCT/PCT Publication No.: 1996/033553
(30) Priorité/Priority: 1995/04/18 (US08/423,951)

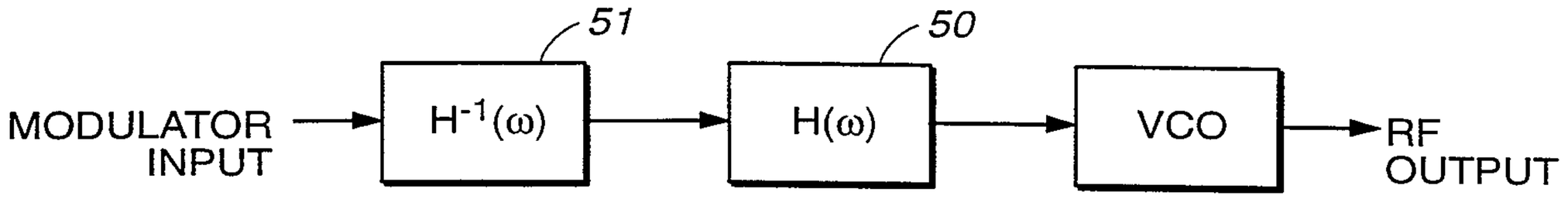
(51) Cl.Int./Int.Cl. *H03C 3/00* (2006.01),
H03C 3/09 (2006.01)

(72) Inventeur/Inventor:
MCCONNELL, PETER, CA

(73) Propriétaire/Owner:
SIERRA WIRELESS, INC., CA

(74) Agent: BLAKE, CASSELS & GRAYDON LLP

(54) Titre : EGALISATION DE COMPROMIS FIXE POUR UN MODULATEUR F.M. A DEUX PORTS
(54) Title: FIXED COMPROMISE EQUALIZATION FOR A DUAL PORT FM MODULATOR



(57) Abrégé/Abstract:
A dual port frequency modulator and method for eliminating the undesired effects caused by high port/low port phase differences in a standard dual port frequency modulator. The frequency modulator includes an inverse filter stage coupled to the input of a modulator stage including a first high port processing path for processing high frequency components of a modulation signal and a second low port processing path for processing low frequency components of a modulation signal. The outputs of the high and low paths are coupled to separate ports of a voltage controlled oscillator. The impulse response of the inverse filter is designed to be the inverse of the impulse response of the modulator stage. The filter functions to counteract the adverse effects caused by the delay difference in the high and low processing paths of the modulator stage such that the overall response of the dual port frequency modulator is significantly improved.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03C 3/09	A1	(11) International Publication Number: WO 96/33553
		(43) International Publication Date: 24 October 1996 (24.10.96)

(21) International Application Number: PCT/CA96/00248

(22) International Filing Date: 18 April 1996 (18.04.96)

(30) Priority Data:
08/423,951 18 April 1995 (18.04.95) US

(71) Applicant: SIERRA WIRELESS, INC. [CA/CA]; 13151 Vanier Place #260, Richmond, British Columbia V6V 2J2 (CA).

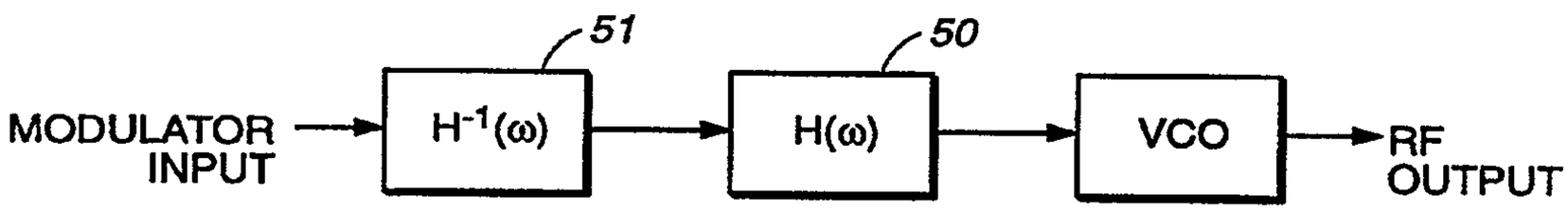
(72) Inventor: MCCONNELL, Peter; 5970 Empress Avenue, Burnaby, British Columbia V6V 2J2 (CA).

(74) Agents: GRAY, Brian et al.; Blake, Cassels & Graydon, Commerce Court West, P.O. Box 25, Toronto, Ontario M5L 1A9 (CA).

(81) Designated States: AU, BR, CA, CN, CZ, FI, JP, KR, MX, NO, NZ, RU, SG, SK, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: FIXED COMPROMISE EQUALIZATION FOR A DUAL PORT FM MODULATOR



(57) Abstract

A dual port frequency modulator and method for eliminating the undesired effects caused by high port/low port phase differences in a standard dual port frequency modulator. The frequency modulator includes an inverse filter stage coupled to the input of a modulator stage including a first high port processing path for processing high frequency components of a modulation signal and a second low port processing path for processing low frequency components of a modulation signal. The outputs of the high and low paths are coupled to separate ports of a voltage controlled oscillator. The impulse response of the inverse filter is designed to be the inverse of the impulse response of the modulator stage. The filter functions to counteract the adverse effects caused by the delay difference in the high and low processing paths of the modulator stage such that the overall response of the dual port frequency modulator is significantly improved.

FIXED COMPROMISE EQUALIZATION FOR A DUAL PORT FM MODULATOR

FIELD OF THE INVENTION

The present invention generally relates to dual port modulators and, more particularly, to systems for reducing distortion in dual port modulators.

BACKGROUND OF THE INVENTION

It is known in the field of signal processing that frequencies close to DC (i.e. zero frequency) are difficult to modulate. One prior art circuit used to overcome this problem is a dual port frequency modulator. The dual port frequency modulator is designed to modulate frequencies from zero frequency and greater.

The conventional dual port frequency modulator includes two data processing paths: a high frequency processing path for modulating high frequency components of the modulation signal and a low frequency processing path for modulating low frequency components. The high frequency processing path typically comprises a buffer and a variable gain amplifier which function to account for frequency deviation and gain imbalances, respectively, between the high and low processing paths. The low frequency processing path, on the other hand, comprises considerably more signal components than the high path due to the additional signal processing needed to modulate lower frequency signals. The lower path often includes a series coupled temperature controlled crystal oscillator (TCXO), two frequency counters, a first phase detector, and a

loop filter. The outputs of the high and low frequency paths are both coupled to a separate input of a voltage controlled oscillator (VCO). The VCO effectively adds the two input signals and outputs the desired frequency modulated signal.

The main drawback for the above described modulator design is that, due to the different structures of the high and low paths, the systems have different time delays between the modulation input and the inputs to the VCO. This time delay difference equates to a phase delay difference between the high and low paths which results in a non-linear phase response in the vicinity of the loop filter cut-off frequency for the above described dual port modulator. Due to this non-linear phase response, signals in the vicinity of the loop filter cut-off frequency have approximately the same amplitudes but different phases. As a result, out-of-phase signals cancel and some attenuation occurs in the output signal of the modulator, thereby affecting the impulse response (i.e. gain and magnitude response) of the modulator. The manner in which the impulse response is affected is that the gain of the modulator in the region of the loop filter frequency "dips". The magnitude response, in turn, affects the modulation index, and in particular, degrades the frequency deviation versus time response of the prior art modulator.

JP-A-0 7 030 332 provides an FM modulator enabling a completely flat amplitude frequency of FM modulated signal, wherein this FM modulator enables FM modulation by creating a flat high frequency and low frequency region on both sides of VCO, using a VCO and a standard VCO for this purpose.

The construction comprises VCO which generates a transmission output signal, divider, which divides one part of this transmission output signal, phase comparator, which provides the output of direct current voltage corresponding to the phase difference between the standard frequency of the output frequency signal of this divider, loop filter, which removes the high cycle components, etc., included in said direct current voltage, synthesizer, connected between

AMENDED SHEET
IPEA/EP

this loop filter and VCO, and an input terminal used to input signal which is to be subject to FM modulation through attenuators, which are used for adjustments of the synthesizer and of SVCO ; including compensating circuit compensating mainly for low pass components of the modulated frequency region between terminal and attenuator.

US-A-4 242 649 describes a phase locked loop which provides frequency modulation over an extended frequency range by summing a modulation signal with the loop signal at two separate points within the loop. The modulation signal is directly applied to the control input terminal of the voltage controlled oscillator. In addition, the modulation signal is processed to compensate for the transfer functions of loop components, and the processed signal is summed with the loop signal at an additional point between the output terminals of the phase detector and the lowpass filter of the loop. The processing of the modulation signal consists of preshaping of the signal to compensate for the transfer functions of loop circuitry located between the voltage controlled oscillator and the summing junction.

SUMMARY OF THE INVENTION

The present invention provides a method and system for eliminating the undesired effects caused by high port/low port phase differences in a dual port frequency modulator. The present invention is achieved by pre-distorting the modulation signal with an "inverse filter", referred to as a fixed compromise equalizer, prior to being coupled to the input of the dual port modulator. The inverse filter has a magnitude and phase response (i.e. impulse response) that is essentially the inverse of the impulse response of the non-ideal dual port modulator. Specifically, the inverse filter provides an impulse response in which the phase delay is compensated for in the region in which attenuation

AMENDED SHEET
IPEA/EP

occurs in the non-ideal modulator response. In one embodiment of the present invention the inverse filter response is incorporated into a pre-existing pre-filtering stage, such as a pulse shaping filter. In this way little or no additional hardware is needed to implement the improved modulator of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art dual port frequency modulator.

Figure 2 shows the phase response for each of the low and high ports of a prior art dual port frequency modulator, the composite phase response of the prior art dual port frequency modulator, and the ideal phase response for a dual port frequency modulator.

Figure 3 shows the typical magnitude response for a prior art dual port frequency modulator.

Figure 4A shows an ideal eye diagram for GMSK with h=0.50 for a prior art modulator.

Figure 4B shows the effects of phase distortion on the eye diagram for a prior art dual port frequency modulator.

Figure 5 shows the improved dual port modulator of the present invention including a pre-distorter stage.

Figure 6 shows the magnitude response of the fixed compromise equalizer of the present invention.

Figure 7 shows the actual eye diagram for GMSK with h=0.50 for the

dual input modulator as shown in Figure 5.

DETAILED DESCRIPTION

In Figure 1, which shows a conventional dual port frequency modulator, the input of the dual port frequency modulator is typically coupled to a GMSK bandwidth limiter 10 which functions to initially bandlimit the modulation signal to a particular frequency range. Next, the bandlimited input signal is passed through buffer 11 which functions to adjust the overall deviation frequency of the modulator. This is performed to ensure that the peak-to-peak voltage of the modulation input signal corresponds to a standardized deviation frequency (f_d). Typically, the deviation frequency is adjusted such that a 1.00 volt peak-to-peak voltage corresponds to a deviation frequency of 4.8 kHz. The output signal from buffer 11 is coupled to two signal processing paths within the modulator: a high frequency processing path and a low frequency processing path.

The low frequency path is responsible for modulating lower spectral frequency components. This path comprises temperature compensated crystal oscillator 12 (TCXO) which generates a reference frequency in the 10 MHz range. This reference frequency is divided down by a frequency counter 13 to a lower reference frequency in the 10-50 kHz range. This reference frequency signal is coupled to a first input of phase detector 14. Phase detector 14 functions to output a voltage signal proportional to the phase difference between the reference frequency signal coupled to its first input and the signal coupled to its second input. The output signal of the phase detector is passed through loop filter 15 which filters out all frequency components below the loop filter cut-off frequency ($f_{loop\ cut\text{-}off}$). The filtered signal is then coupled to a first input of voltage controlled oscillator 16 (VCO). VCO 16 essentially adds the two signals from each of the high and low paths and outputs a signal having a frequency proportional to the voltages of the inputs signals.

The high frequency path is responsible for modulating the higher spectral frequency components. This path comprises buffer 17 and variable gain amplifier 18. Buffer 17 functions to balance the deviation frequency between the high and low signal processing paths and amplifier 18 functions to scale the output signal of the second buffer so as to balance the gain between the first and second signal processing paths. The output of amplifier 18 is coupled to a second port of VCO 16. The second port of the VCO effectively bandlimits the high frequency signal from the high frequency signal processing path such that only frequency components above the loop filter cut-off frequency affect the VCO from this port. The output of VCO 16 is fed back to the second input of phase detector 14 through frequency counter 19.

Figure 2 shows a composite phase response 22 of the prior art dual port modulator shown in Figure 1. In Figure 2, the phase response 20 is shown for the high path and the phase response 21 for the low path. Because the low path contributes a signal only having significant amplitude below $f_{loop\ cut\text{-}off}$, the frequency components of phase response 22 below $f_{loop\ cut\text{-}off}$ (section A) appear to have a phase response that is the same as low path response 21. Similarly, because the high path contributes a signal only having significant amplitude above $f_{loop\ cut\text{-}off}$, frequency components of phase response 22 above $f_{loop\ cut\text{-}off}$ (section C) appear to have a phase response that is the same as high path response 20. However, the phase response 22 at frequencies in the vicinity of $f_{loop\ cut\text{-}off}$ (section B) is determined by a composite signal originating from both of the high and low paths. This composite signal causes phase response 22 to be non-linear for frequencies within section B resulting in phase distortion within that frequency region.

Due to the above-described phase delay distortion, the signals from each of the high and low paths at the frequencies in the vicinity of $f_{loop\ cut\text{-}off}$ have approximately the same amplitude but different phases. As a result, some of these out-of-phase signals cancel each out and cause attenuation in the magnitude response of the modulator.

Figure 3 shows the attenuation effect on the amplitude response of the prior art modulator having a loop cut-off frequency of approximately 3.6 kHz, (i.e. $f_{loop\ cut\text{-}off} = 3.6$ kHz). As seen in Figure 3, a "dip" (indicated by 30) in gain occurs approximately at 3.6 KHz indicating gain attenuation. Similarly, some of the signals in the vicinity of the loop filter cut-off frequency add together resulting in peak 31 indicating a boost in gain.

This attenuation can be mathematically described in the following manner. The output voltage signal from VCO 16, S(t), can be represented as the sum of two signals, $v_1(t)$ and $v_2(t)$. Because $v_1(t)$ and $v_2(t)$ are low pass and high pass filtered versions of the same signal, S(t) can be expressed as follows:

eq. 1 $$S(t) = v_1(t) + v_2(t) = m(t)h_{lp}(t) + m(t)h_{hp}(t)$$

where m(t) is the modulation input signal and $h_{lp}(t)$ and $h_{hp}(t)$ are the impulse response functions of the low and high ports, respectively. At low frequencies, the signal S(t) is primarily the resultant convolution of the low pass response with modulation signal m(t). In other words $m(t)h_{hp}(t)$ @ 0 in equation 1 and $S(t) = m(t)h_{lp}(t)$. At high frequencies, the signal S(t) is primarily the resultant convolution of the high pass response with signal m(t), (i.e. $m(t)h_{lp}(t)$ @ 0 and $S(t) = m(t)h_{hp}(t)$).

However, at the floop cut-off both v1 and v2 contribute to signal S(t). Thus, S(t) at floop cut-off can be expressed, using $m(t) = \cos(f_c t)$ and $h_{lp}(t) = h_{hp}(t) = 0.50$, as follows:

eq. 2

$$\begin{aligned} S(t) &= v_1(t) + v_2(t) \\ &= 0.50\cos(f_c t) + 0.50\cos(f_c t + F) \\ &= 0.50\{\cos(f_c t) + \cos(f_c t + F)\} \\ &= 0.50\{\cos(f_c t) + \cos(f_c t)\cos(F) - \sin(f_c t)\sin(F)\} \\ &= 0.50\cos(f_c t)\{1 + \cos(F)\} - 0.50\sin(f_c t)\sin(F)\} \end{aligned}$$

For small F, sin(F) @ 0, so that we can approximate the above expression as:

eq. 3

$$\begin{aligned} S(t) &= 0.50\cos(f_c t)\{1 + \cos(F)\} \\ &= \cos(f_c t)\cos^2(F/2) \end{aligned}$$

If the phase difference of the signals in the two paths is zero, there will be no gain attenuation of the signal m(t) at the corner frequency. If however there is a non-zero phase difference between the two signals, $\cos^2(F/2) < 1.0$ and there will be attenuation at $f_{loop\ cut\text{-}off}$. For example, a phase difference in the high port and low port paths of 40 degrees results in an attenuation of approximately 1.08 dB at the corner frequency. As described above, due to a difference in time delay between the two paths, a phase difference between the high and low path of the prior art modulator results and $\cos^2(F/2) < 1.0$.

The affect of the attenuation of the magnitude response also causes the degradation of the frequency deviation versus time response of the modulator, in particular, it causes an error in the modulation index. Figure 4A shows an ideal frequency versus time eye

diagram for a modulator having a modulation index equal to 0.50 and Figure 4B shows the frequency deviation versus time eye diagram for a typical prior art modulator. As shown in Figure 4B, the phase distortion of the prior art modulator not only causes variations along the frequency deviation axis (i.e. modulation index error), but it also causes variations along the time axis (i.e. phase jitter) as illustrated in Figure 4B.

In accordance with the present invention, Figure 5 shows a system including a dual port modulator 50 and fixed compromise equalizer 51. The system provides improved overall impulse responses by modulator 50 by applying fixed compromise equalizer 51 to the modulation signal prior to coupling to the input of modulator 50. The equalizer functions as an inverse filter and *pre-distorts* the modulation signal such that it essentially counteracts the undesired deviations in modulator 50 magnitude response. As indicated in Figure 5, the response of modulator 50 is H(w) and the response of equalizer 51 is $H^{-1}(w)$. In other words, fixed compromise equalizer 51 is designed to provide the opposite response as that of modulator 50. It is well known in the art of signal processing how to implement a circuit that provides a particular response. For instance, a stereo equalizer is designed such that gain can be manually varied to specific frequencies to provide the desired response to a listener. Another example of a circuit that is designed to provide a given response is a data modem where a fixed compromise equalizer is used to compensate for magnitude and phase distortions in a telephone channel.

Figure 6 shows the magnitude response of a fixed compromise equalizer as described by the present invention designed to be utilized with a modulator having a magnitude response as illustrated in Figure 3. As shown, the magnitude response of the equalizer *peaks*

(indicated by 60) at the same frequency at which the modulator magnitude response shown in Figure 3 *dips*. In other words, equalizer 51 increases the gain for frequencies at which attenuation occurs in modulator 50 magnitude response. It may be noted that equalizer 50 is designed to account for peak 31 shown in Figure 3. As shown in Figure 6, the equalizer response dips (indicated by 61) at the same frequency at which peak 31 (Figure 3) occurs in the modulator response.

Figure 7 shows the actual frequency deviation versus time eye diagram for the improved modulator of the present invention in which $h=0.50$. As can be seen in Figure 7 all adverse effects (as seen in Figure 4B) due to the phase delay difference between the high and low modulation paths are eliminated.

One aspect of the present invention is that the inverse response may be convolved with the response of a pre-existing transmitter pulse shaping filter that is coupled to the input of the dual port modulator. Thus, the present invention may be implemented with the addition of very few (if anymore) components.

In the foregoing, a method and system was described for eliminating the undesired effects caused by high port/low port phase differences in a dual port frequency modulator is described. In the description, numerous specific details were set forth, such as particular frequencies and modulation indexes, to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well-known signal processing theory has not been described in detail in order to avoid unnecessarily obscuring the present invention.

Thus, although the elements of the present invention have been described in conjunction with a certain embodiment, it is appreciated that the invention may be implemented in a variety of other ways. Consequently, it is to be understood that the particular embodiment shown and described by way of illustration are in no way intended to be considered limiting. Reference to the details of this embodiment is not intended to limit the scope of the claims which themselves recite only those features regarded as essential to the invention.

CLAIMS

What is claimed is:

1. A dual port frequency modulator having two input modulation ports associated with two paths (1, 2), comprising: a means (50) for modulating a reference signal with a modulating signal, said modulating means having an impulse response with associated magnitude and phase characteristics; and a means (51) for filtering said modulating signal, said filtering means being coupled to input of said modulating means, characterized in that:

said filtering means has an impulse response with associated magnitude and phase characteristics that counteract the magnitude and phase characteristics of the means for modulation such that both the magnitude as well as the phase characteristics of the means for modulation are compensated.

2. The dual port frequency modulator as described in Claim 1 wherein said modulating means (50) includes a first signal processing path (1) for processing high frequency components of said modulating signal, a second frequency processing path (2) for processing low frequency components of said modulating signal, and a voltage controlled oscillator (16), wherein said first and second signal processing paths have their inputs coupled to said filtering means and their outputs coupled to said voltage controlled oscillator.

3. The dual port modulator as described in Claim 1 wherein said filtering means is a pulse shaping filter.

4. The dual port modulator as described in Claim 1 wherein said associated impulse response of said modulating means is non-linear and wherein an overall impulse response of a combination of said modulating means and said filtering means is essentially linear.

5. A method for eliminating undesirable modulator impulse response of a dual port frequency modulator having a modulation signal coupled to its input port, said modulation signal being processed through a first signal processing path (1) having a first associated delay and a first output and a second signal processing path (2) having a second output and having a second associated delay unequal to the first associated delay, the outputs of said first and second signal processing paths being coupled to a voltage controlled oscillator (16), wherein the inequality of

said first delay and said second delay causes an undesirable modulator impulse response with associated magnitude and phase characteristics, the method comprising pre-distorting said modulation signal prior to coupling it to said input port to generate a pre-distorted signal having a pre-distortion impulse response with associated magnitude and phase characteristics, the method further characterized by:

setting said pre-distortion impulse response such that both the magnitude as well as the phase characteristics of the modulator impulse response are compensated by counteraction from the magnitude and phase characteristics of the pre-distortion impulse response.

6. The method as described in Claim 5 wherein said pre-distortion impulse response is incorporated into a pulse shaping filter.

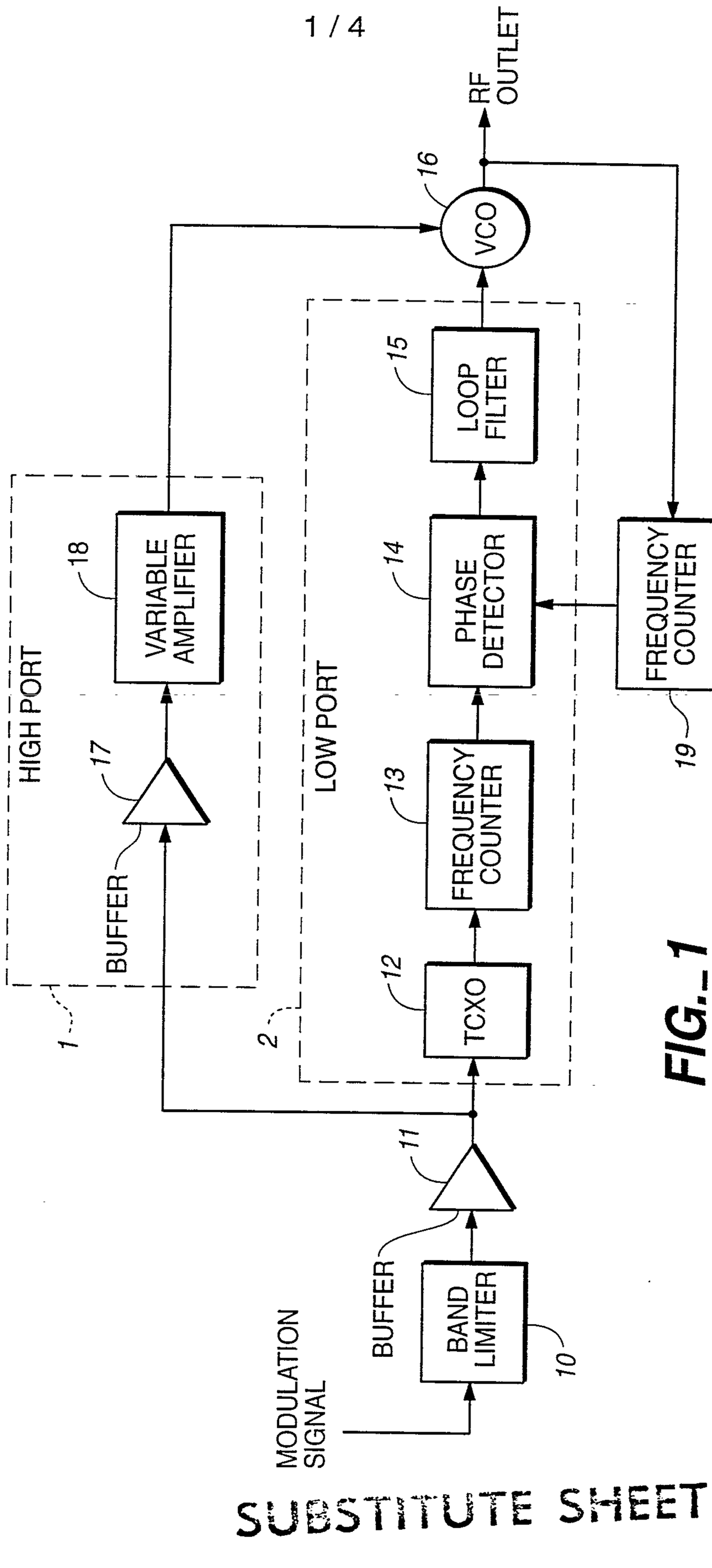


FIG._1
(PRIOR ART)

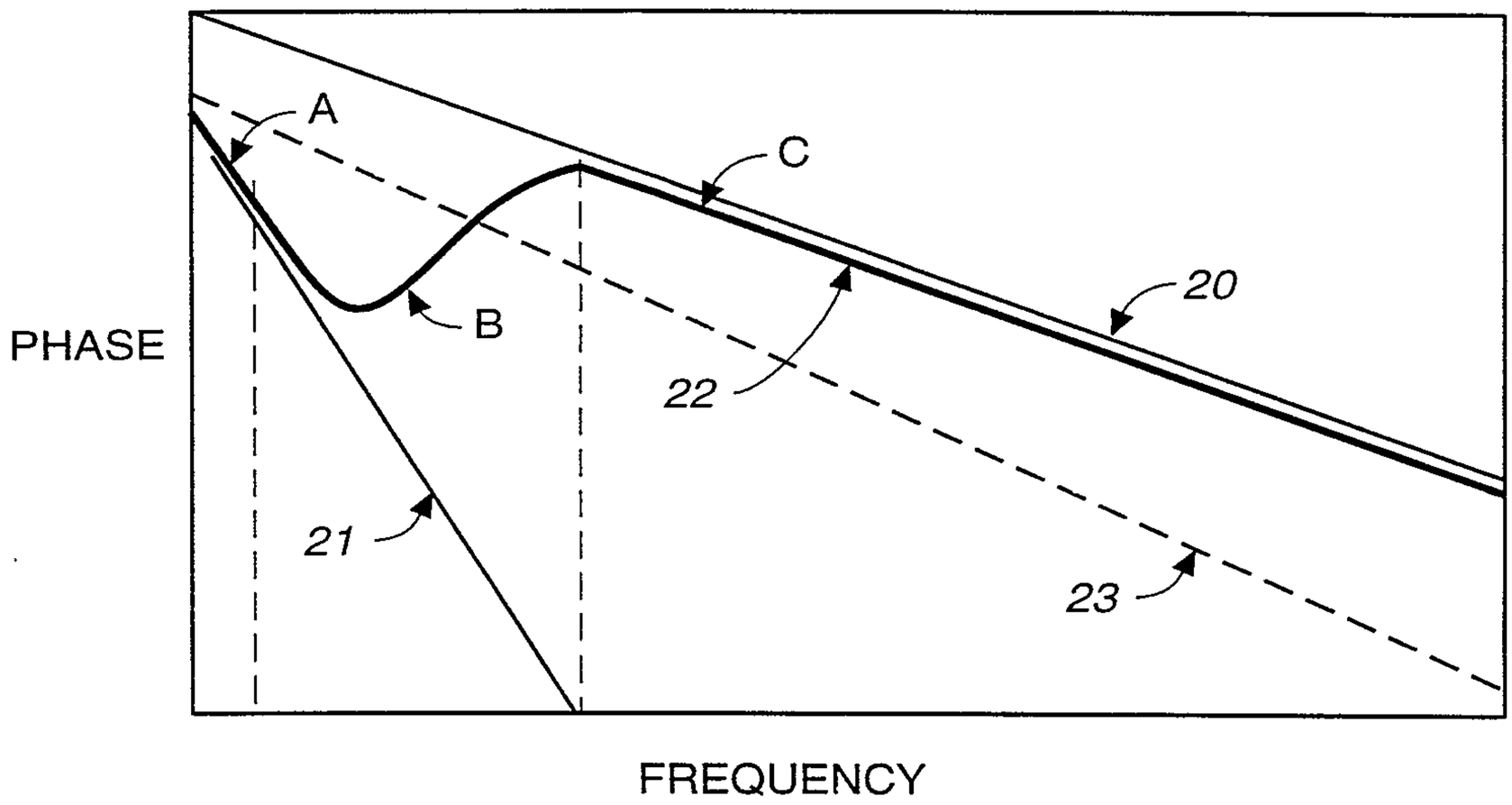

A
B
C
20
22
21
23
PHASE
FREQUENCY

FIG._2

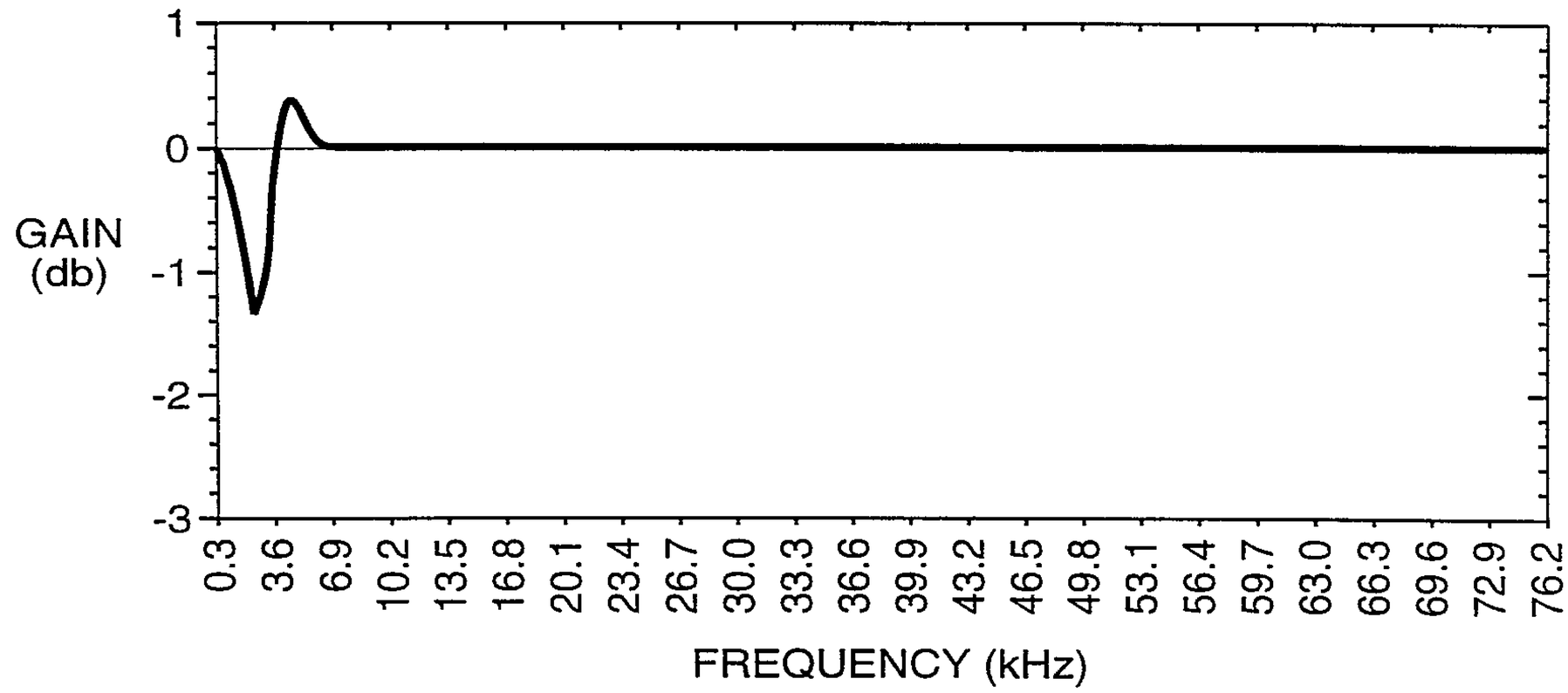

1
0
-1
-2
-3
GAIN
(db)
0.3
3.6
6.9
10.2
13.5
16.8
20.1
23.4
26.7
30.0
33.3
36.6
39.9
43.2
46.5
49.8
53.1
56.4
59.7
63.0
66.3
69.6
72.9
76.2
FREQUENCY (kHz)

FIG._3

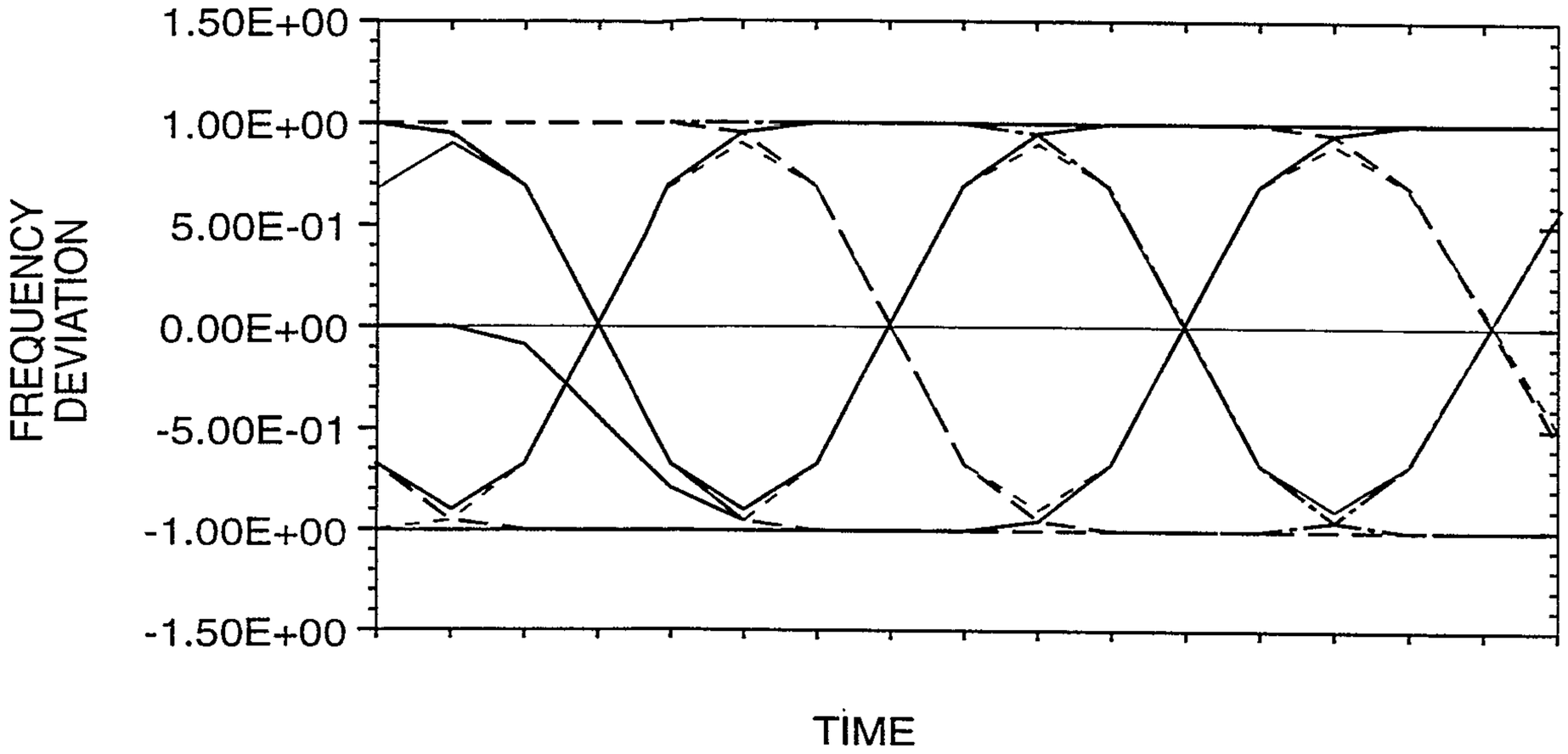

1.50E+00
1.00E+00
5.00E-01
0.00E+00
-5.00E-01
-1.00E+00
-1.50E+00
FREQUENCY DEVIATION
TIME

FIG._4A

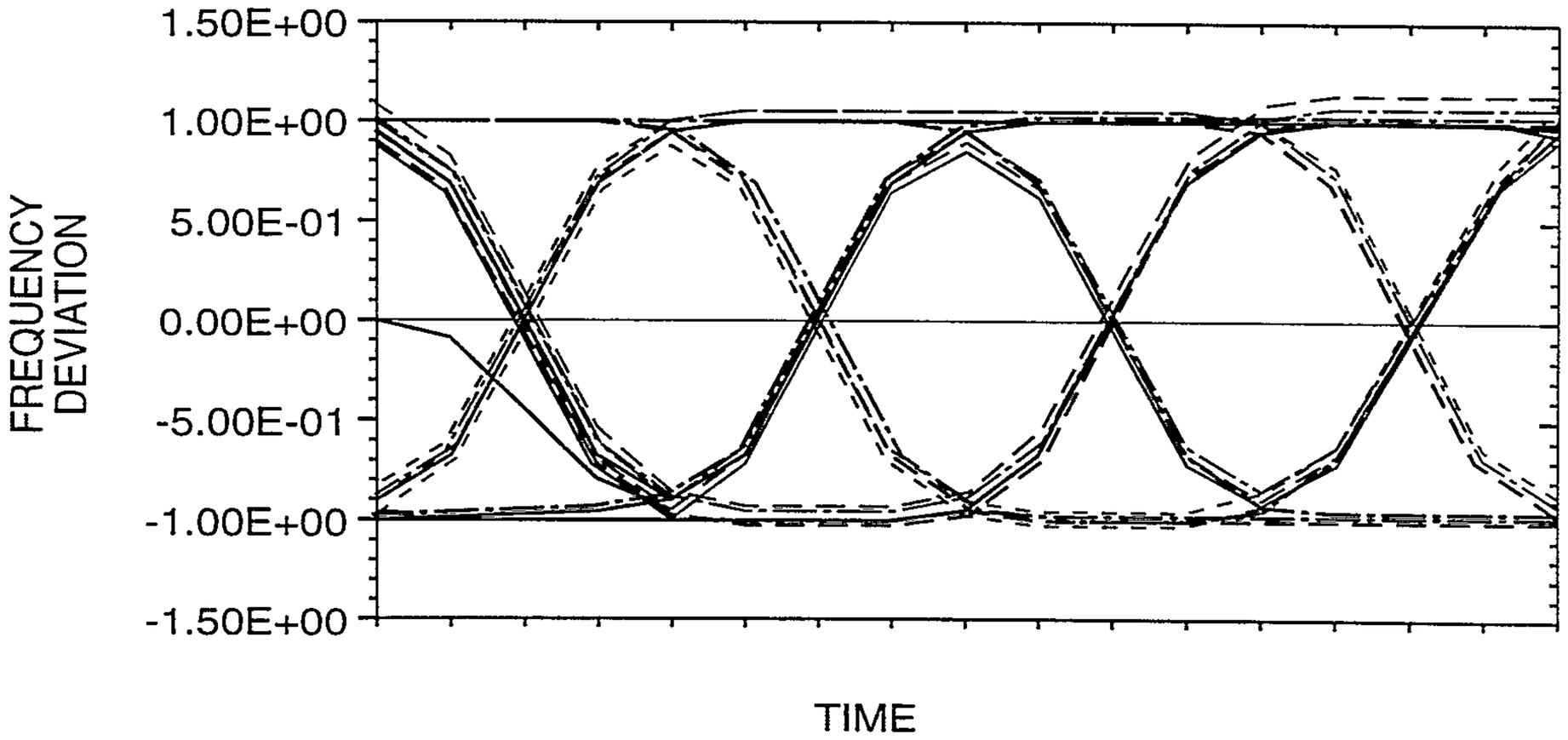

1.50E+00
1.00E+00
5.00E-01
0.00E+00
-5.00E-01
-1.00E+00
-1.50E+00
FREQUENCY DEVIATION
TIME

FIG._4B

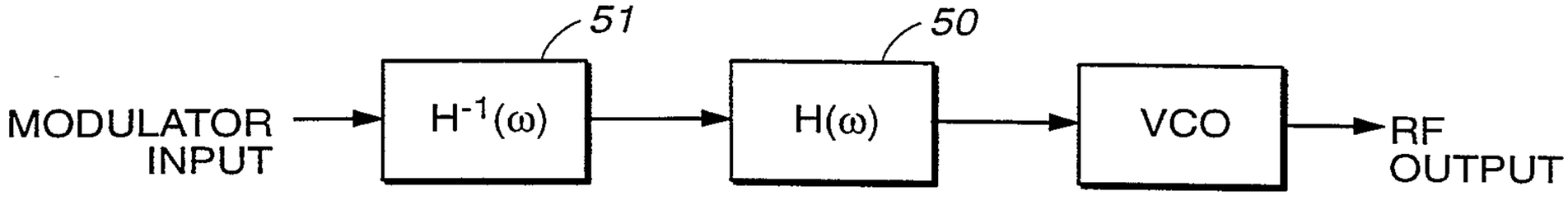


FIG._5

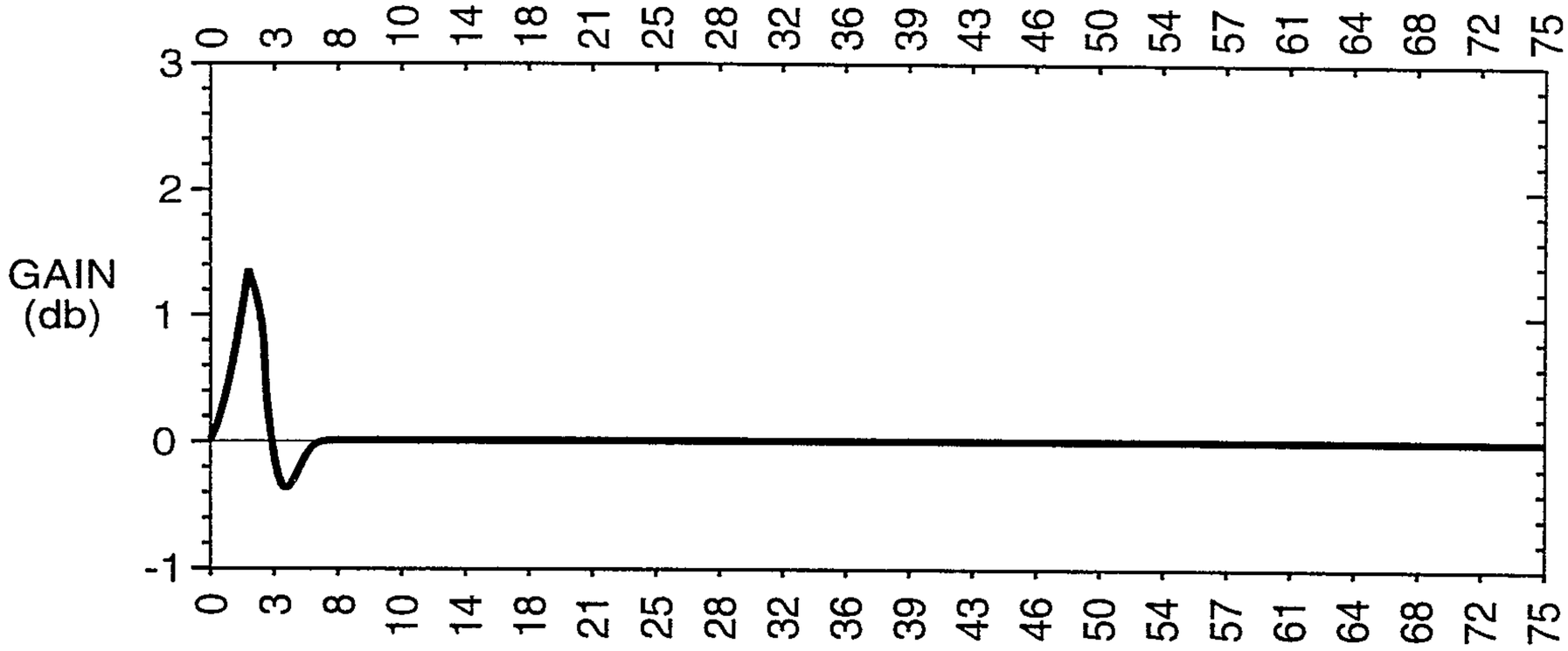


FIG._6

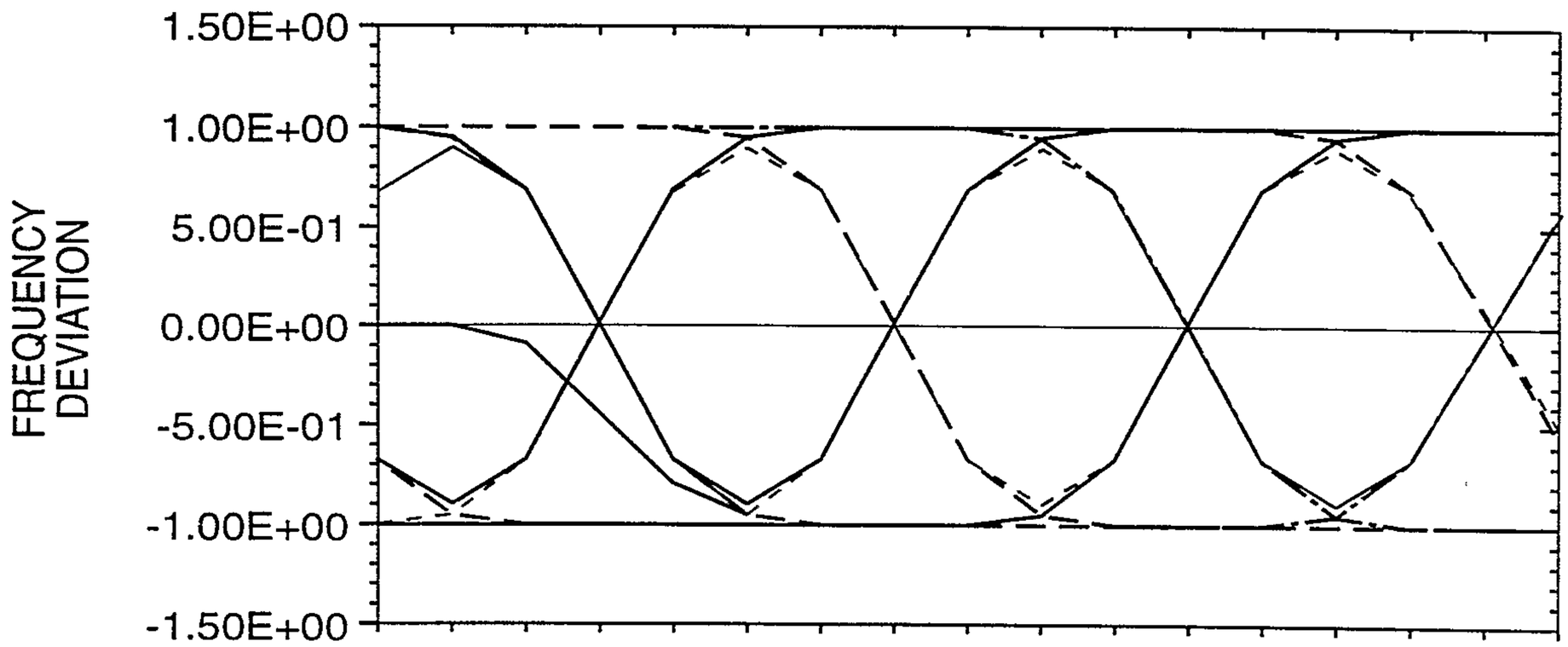
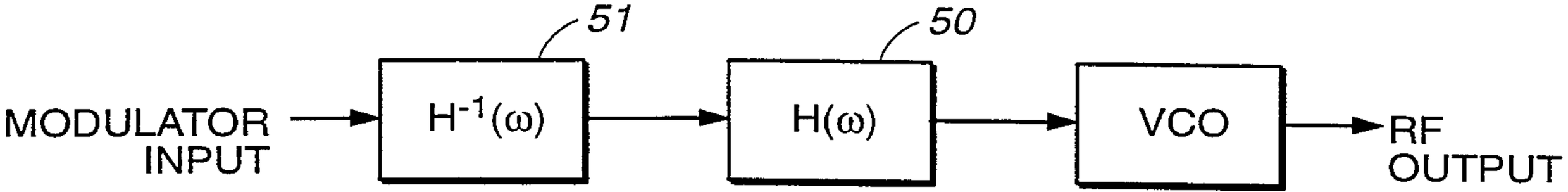


FIG._7


51
50
MODULATOR INPUT
$H^{-1}(\omega)$
$H(\omega)$
VCO
RF OUTPUT