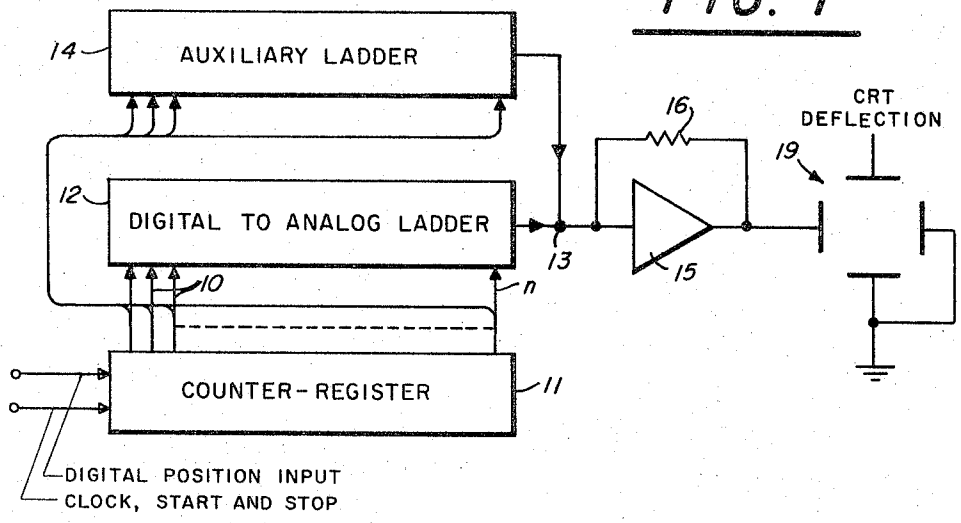
Feb. 28, 1967 A. E. POPODI ET AL 3,307,173

TRANSIENT REDUCTION IN DIGITAL-TO-ANALOG CONVERTERS

Filed April 16, 1964 2 Sheets-Sheet 1

FIG. 1



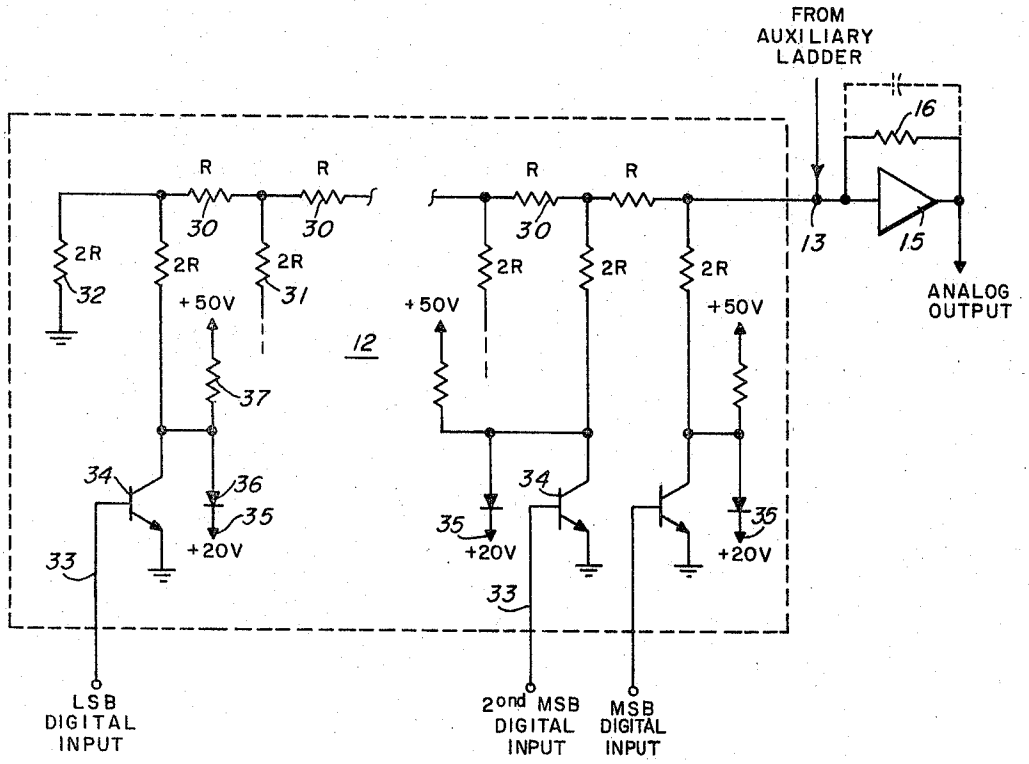




FIG. 2

INVENTORS
ALFRED E. POPODI
CHARLES R. PEARMAN

BY

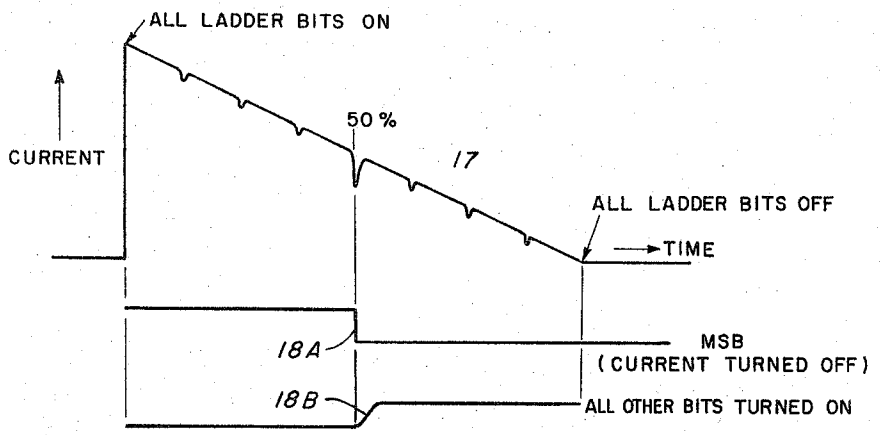
ATTORNEYS

Feb. 28, 1967 A. E. POPODI ET AL 3,307,173

TRANSIENT REDUCTION IN DIGITAL-TO-ANALOG CONVERTERS

Filed April 16, 1964 2 Sheets-Sheet 2

FIG. 3



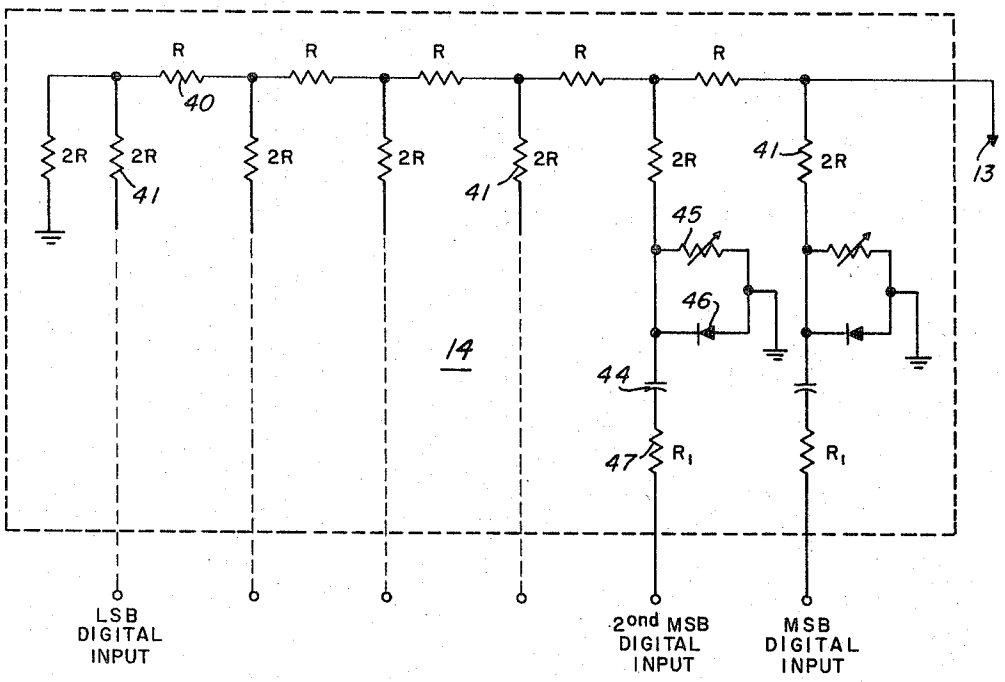




FIG. 4

INVENTORS
ALFRED E. POPODI
CHARLES R. PEARMAN
BY
Paul u. Gutchlon
T. L. Stymer
ATTORNEYS

United States Patent Office 3,307,173
Patented Feb. 28, 1967



3,307,173

# TRANSIENT REDUCTION IN DIGITAL-TO-ANALOG CONVERTERS

Alfred E. Popodi, Glen Burnie, and Charles R. Pearman, Baltimore, Md., assignors, by mesne assignments, to the United States of America as represented by the Secretary of the Navy

Filed Apr. 16, 1964, Ser. No. 360,464
4 Claims. (Cl. 340—347)

This invention relates to digital-to-analog converters and is particularly directed to means for reducing switching transients in the analog output circuit.

The conventional digital-to-analog converter comprises a ladder network of resistances, the input of a summing amplifier connected to one end of the ladder, and switches for applying either of two voltages, corresponding to logical 1's and 0's, to each of the sections of the ladder. Where high switch speeds are employed and measurable currents are interrupted transient voltages inevitably result. Smoothing condensers cannot be employed in the output circuit because of the non-uniform nature of the transients arriving at the output from different points along the ladder. Added capacity, of course, reduces the speed with which the converter can be operated.

An object of this invention is to provide an improved digital-to-analog converter.

A more specific object of this invention is to provide a digital-to-analog converter in which the switching transients are minimized.

The objects of this invention are attained by constructing two ladder networks and connecting the output terminals of each ladder into a summing amplifier. The digits of the binary number to be converted are fed into the principal ladder through conventional switching elements The digit voltages are at the same time fed into corresponding sections of the auxiliary ladder through differentiating R.C. networks to simultaneously produce a voltage spike at each resistance section corresponding to the expected transient spike in the principal ladder. The two simultaneous spikes for corresponding sections are equal distances from the output terminal and may be so polarized as to oppose and neutralize each other in the output circuit. Each differentiating network is easily adjusted so as to balance out each switching transient.

Other objects and features of this invention will become apparent to those skilled in the art by referring to the preferred embodiment described in the following specification and shown in the accompanying drawings in which:

FIG. 1 is a block diagram of the digital-to-analog converter of this invention;

FIG. 2 is a schematic circuited diagram of one principal resistance ladder network of the type which may be used in the system of FIG. 1;

FIG. 3 is a graph of the output voltage of the converter of this invention; and

FIG. 4 is a schematic circuit diagram of the auxiliary resistance ladder of the system of FIG. 1.

Referring to FIG. 1, it will be assumed that the two voltages representing the logical ones and zeros of each of the significant places in a binary number appear in parallel on $n$ output lines, **10**, of the counter-register **11**. The digital number is converted in the principal resistance ladder **12** to a voltage at junction **13** corresponding in amplitude to the digital number. Details of one resistance ladder **12** are shown by way of example in FIG. 2.

According to this invention, each digit of the digital number is applied simultaneously to corresponding inputs of the auxiliary ladder **14**. The output of the auxiliary ladder is connected directly to the junction **13**. To convert the currents added at junction **13** to an analog voltage, the conventional summing operational amplifier **15** is employed with the resistive feedback **16** connected between the output of the amplifier and the summing point **13** at the input of the amplifier. As will appear below, the output of the auxiliary ladder contains voltage spikes which are equal in amplitude and opposed in phase to the transient voltage spikes created by the switching circuits in the principal ladder **12**.



It will be assumed that a sweep voltage is to be generated and that the analog output of the amplifier **15** is applied to the deflection circuit of the cathode ray tube **19** where the most minute transients can be seen on the screen. FIG. 3 shows the graph of a sweep voltage that could be applied to one pair of deflection plates where the deflection voltage descends from a miximum voltage value of one polarity to a maximum voltage of opposite polarity. At the center of the deflection the switch of the most significant binary digit at the input of the counter operates. It has been found that the current of the most significant bit, when turned off, changes rapidly as shown at **18A**, FIG. 3, whereas the bits of the other digits change slowly, as shown at **18B**.

The problem of generating a smooth ramp is acute since the cathode ray beam remains on during the entire ramp period. Tansients on the ramp not only appear as undesired deflections but also as intensity changes with the changing duty cycle of the logic inputs. Intensity changes confuse the video data input which is presented as intensity modulations on the control grid of the cathode ray tube. The generation of accurate, fast and spike free ramp functions by digital means has presented difficult problems because spike amplitudes with less than one-tenth of one percent of full CRT deflection can be easily seen by the operator. As stated, the object of this invention is to eliminate the voltage spikes shown at **18** in FIG. 3 from the sweep voltage of the converter.

FIG. 2 shows a simplified diagram of a digital-to-analog converter using a resistance ladder network with the associated summing amplifier **15** at the output terminal of the ladder. The amplifier **15** converts the ladder output current to its voltage equivalent. The series resistances **30** are uniformly of one unit of resistance while the shunt resistances **31** are each two units of resistance. The left end of the ladder is grounded through the terminal resistance **32**, also of two units of resistance. The junction **13** is connected to the right hand end or output of the ladder. The number of sections in the ladder network correspond, of course, with the number of significant places in the binary number to be converted. Each logical 0 or 1 from the least to the most significant digit is applied to the control circuit **33** from the binary number source **11**.

The particular switching elements shown comprise transistors **34**. The transistors are of the NPN type so that any one of the transistors can be turned off by a negative base voltage. When turned off, the collector will be clamped at the reference potential applied, in all sections, to the terminal **35**. The collector is connected through the diode **36** to the terminal, the diode being forwardly biased through high resistances **35**. Hence when the various transistors are turned off and the collectors are clamped to a positive voltage, in the example shown, the various voltage divisions are summed at point **13** according to the significance of the digits involved.

Zero logic inputs to terminals **33** causes the transistors to turn on and ground the reference voltage. It has been found that the negative going edge of the binary pulse at input terminals **33** which turns off the transistor is

always slower than the positive going edge. The negative going edge of the switching voltage turns the ladder bit current on, and the turn-on of a ladder current is always slower than its turn-off time. In addition to this there exists the inherent time delay between the triggered and the non-triggered output side of the flip-flops of the counter register **11** which is the source of the binary digits. When the most significant bit is switched off by a relatively fast positive-going switching pulse edge, the other bits are simultaneously switched on by their relatively slower negative-going inputs. This causes a current deficiency in the ramp producing a negative current spike. Likewise, other spikes are generated at different times by the ladder bits. Fortunately, all transients have the same polarity which is negative in the example here assumed.

Novel means for spike compensation according to this invention are shown in FIG. 4. For the downgoing current ramp here assumed, where all transients have negative polarities, compensation is achieved by adding weighted, positive, correcting currents to the operational amplifier. According to this invention these oompensating currents are derived from the same binary source that drives the digital-to-analog converter **12**. That is, the compensating current is derived from the logic switching voltage itself. The necessary weighting is performed in a simple auxiliary ladder network so proportioned as to simulate the propagation delays in the main ladder, FIG. 2, of the converter.

In FIG. 4, ladder **14** comprises series resistance **40** and shunt resistances **41** of the same relative values as resistances **30** and **31** of the principal ladder network, FIG. 2. The auxiliary ladder is similarly terminated at each end and the output end is connected to the summing point **13**. Each shunt resistor **41** is connected to the digital input through a differentiating circuit. The differentiating circuit comprises, here, the series coupling condenser **44** and the grounded shunt resistance **45**. The resistance **45** is paralleled with the diode **46** and is connected between the condenser **44** and ground. Resistances **47** are for isolating and voltage dividing. Because of the polarization of diode **46**, only positive correcting pulses can enter the auxiliary ladder. Negative going switching voltages are clamped to ground by diode **46** and cannot contribute negative corrections. Resistors **45** can each be made variable to permit optimizing the corrective effect of each digit.

The component values shown in the drawings have been successfully used for 0 to −8 voltage logic signals with approximately 220 nanoseconds rise and 80 nanoseconds fall times. There was a 7 to 1 reduction in the transient amplitude and the equally important decrease in pulse duration was about 10 to 1.

By connecting the auxiliary ladder in parallel with the digital-to-analog converter, the operating speed of the converter can be increased and where the output of the converter is employed to generate a sweep voltage the elimination of transients is particularly important. The polarities of voltages and component values may, of course, be changed without departing from the scope of this invention.

What is claimed is:

**1.** In combination in a digital-to-analog converter;
a register having a series of output terminals for generating binary digit voltages of progressive significance,
a first and a second ladder network, each network including a plurality of serially connected attenuation sections corresponding in number to the number of said binary digits, said networks having a common output terminal,
a source of reference potential,
a plurality of switch elements, said elements being connected, respectively, between said reference source and the sections of said first ladder network and being responsive, respectively, to different digit voltages to selectively add the attenuation of different sections to produce a voltage at said output terminal which is the analog of the digital number of said register,
means to buck transient voltages at said output terminal generated by said contributing elements comprising a differentiating circuit connected between each attenuating section of said second ladder network and one terminal of said register for generating voltage spikes equal and opposite in polarity to said transient voltages.

**2.** In combination in a digital-to-analog converter;
a register having a series of output terminals for generating binary digit voltages of progressive significance,
a ladder network including a plurality of serially connected attenuation sections corresponding in number of the binary digits.
a summing amplifier connected to the output terminal of said network,
a source of reference potential,
a plurality of switch elements, said elements being connected respectively between said reference source and the sections of said ladder network and being responsive, respectively, to said binary voltages,
means to minimize transient switching voltages at the input of said amplifier comprising a plurality of differentiating circuits, said differentiating circuits being connected, respectively, between each output terminal of said register and the input of said amplifier.

**3.** In combination in a digital-to-analog converter;
a register having a series of output terminals for a series of binary number digits,
a principal resistance ladder network, said network including a plurality of serially connected attenuation sections, said sections corresponding in number to the number of digits,
a summing amplifier connected to the output end of said ladder,
an auxiliary ladder, said auxiliary ladder including a plurality of serially connected attenuation sections corresponding to the sections of said principal ladder,
differentiating circuits connected, respectively, between each register output terminal and each section of said auxiliary ladder and means for adjusting the amplitude of each differentiated voltage to equal and oppose each switch transient voltage of said principal ladder.

**4.** The combination defined in claim **3** further comprising a cathode ray tube, one deflection circuit of said tube being connected to the output of said summing amplifier.

No references cited.

MAYNARD R. WILBUR, *Primary Examiner.*

J. WALLACE, *Assistant Examiner.*