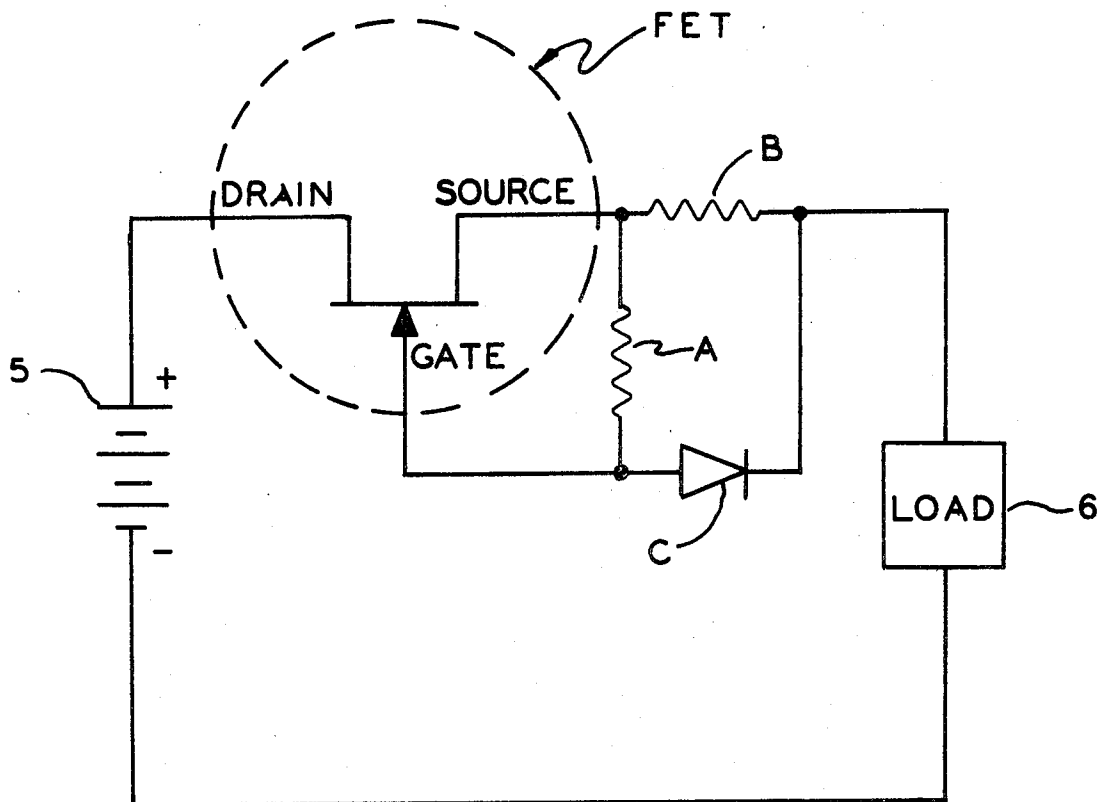
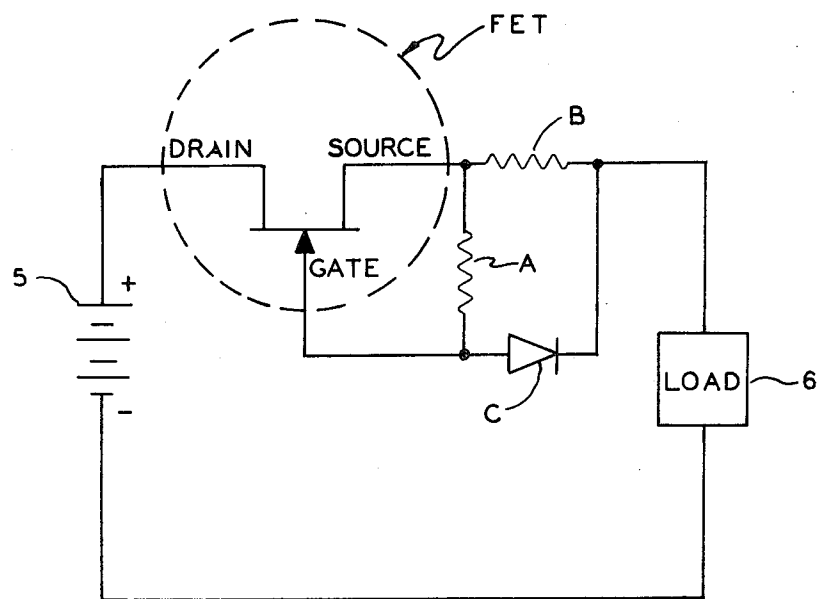


Swain

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INVENTOR.
CHARLES GARDNER SWAIN
BY *Norman E. Saliba*
ATTORNEY

TEMPERATURE-COMPENSATED CURRENT REFERENCE

This invention relates to simple electrical devices for maintaining a constant direct current through a load substantially independent of temperature from 0° to 60°C. and substantially independent of voltage from 5 to 12 volts. More specifically it is directed to a circuit comprising a field-effect transistor (FET), another semi-conductor, and at least two resistors which can be selected or adjusted to give a temperature coefficient below 0.01%/°C., with a voltage coefficient below 0.1%/volt from 5 to 12 volts.

Prior art current-limiter or current-regulator diodes involving field-effect transistors (like IN5283) have been manufactured and specified only for currents of 200 microamperes or more, because temperature coefficients become relatively high (typically above 0.3%/°C.) at lower currents. Temperature-compensated (0.01%/°C.) zener reference diodes (like IN4565) can be used to regulate voltage instead of current, but they require even heavier currents, have poorer voltage coefficients, and are not suitable for regulating at voltages below 6 volts. However, in portable, small-size, battery-operated equipment such low current drains as 10 microamperes may be a real advantage because they may permit such equipment to be left on continuously without the necessity of frequently replacing the batteries. A low voltage requirement is advantageous because it also allows the use of smaller batteries. If battery cost, weight, and frequency of replacement can be kept sufficiently low, the greater simplicity, portability and immunity to power failure of battery-operated devices makes them often preferable to A.C. line-operated devices. This invention is well suited for furnishing a constant current at the often desirable 10-microampere level, where prior art devices are inadequately temperature compensated or much more complicated.

Although field-effect transistors at a fixed gate-source voltage exhibit positive temperature coefficients for drain currents below a certain critical current level, the situation is reversed and they show negative temperature coefficients at higher currents. Prior art devices have been manufactured and specified for use only near the critical current level where their temperature dependence is close to zero. The present invention, by a novel circuit modification, also allows temperature compensation above this critical current level, again by selection of proper values for two resistors.

It is therefore, the primary object of this invention to provide a device for predetermining and maintaining a constant current through a load which is substantially independent of temperature in the range of about 0° to 60° C., having a temperature coefficient of about 0.005 percent per degree or less over this range. Another object is to provide a device which will allow battery-powered equipment to operate for long periods of time at a low constant current level such as 10 microamperes without frequently replacing the batteries and without exceeding the capacity of the batteries. A further object is a device that will supply a load with a constant current having a voltage coefficient of about 0.05 percent per volt from about 5 to 12 volts. Other objects will in part be obvious and apparent from the disclosure herein.

The essential feature of this invention as illustrated in the circuit diagram of the accompanying figure is the use of two resistors, A and B, to adjust the fraction of the field-effect transistor (FET) source-drain current that passes through C, a diode or other semiconductor, to a value such that the temperature coefficient of the voltage across this semiconductor C compensates the temperature coefficient of the FET. Two resistors is the minimum number required for both setting the source-drain current to the desired level and also reducing the temperature dependence essentially to zero in this way.

The Figure illustrates a simple embodiment of my invention where FET is the field-effect transistor, C is a diode, A is a resistor in series with C, B is a resistor that shunts A and C, 5 is the external voltage source such as battery and 6 is the external load to which the constant current is being supplied. The FET may be an N-channel type like 2N5484 or 2N5457 and the diode C may be a 1N457. The optimum values of resistors A and B are sensitive to the type of FET and its pinchoff voltage; they are typically $500K \pm 100K$ ohms and $250K \pm 100K$ ohms respectively when using a 2N5484 to regulate at 10 microamperes; the smaller values being associated with transistors with smaller (less negative) pinchoff voltages. The temperature compensation by the diode C would be inadequate if all of the current were passed through it, but it increases as more of the current is shunted around it and through resistor B.

In another embodiment, a P-channel FET may be used if the polarities of the diode, voltage source and current are all reversed. Alternatively, C may be a thermistor or some other semiconductor with a negative temperature coefficient of voltage or resistance (or positive temperature coefficient of current), instead of a diode, such as for example another transistor (either bipolar or field-effect type) appropriately biased by additional resistors. It is possible to control high currents rather than very low currents by substitution of a high-power FET for the very low power 2N548 type.

In another embodiment, temperature compensation may be accomplished at high currents above that at which no compensation is required, by connecting the gate of the FET to the junction of resistor B and diode C rather than to the junction of resistor A and diode C. Alternatively a positive temperature-coefficient thermistor or another semiconductor with a positive temperature coefficient may be used for C.

Determination of optimum resistance values of the two resistors A and B for the desired current is complicated by the fact that current level and temperature dependence are interdependent. Nevertheless, measurements at the extremes of the required temperature range with two or more pairs of values can be used to calculate values that are acceptable over the whole range. A practical procedure is as follows: As initial values of R_A (resistance of A) pick the closest two values still expected to bracket its optimum value, based on previous experience with the type and pinchoff voltage of the FET used, or pick values of 200K and 800K ohms if previous experience is lacking. At the lowest temperature required, determine the R_B value corresponding to each R_A for the desired current. At the highest temperature required, determine the change in current (D =current at highest temperature minus current at lowest temperature) for each com-

ination. If D for neither combination is within the desired limit, calculate a better R_A from the previous R_A values (A and A') and their corresponding D values (D and D') by $R_A = A + [D/(D-D')] (A'-A)$ and pick a second R_A smaller (or larger) than the better R_A by the amount that the previous R_A with the smallest D was larger (or smaller). While still at the highest temperature, determine the R_B value corresponding to each of the two new R_A values for the current desired. At the lowest temperature, determine D for each new combination. The above interpolation formula gives a better value, and a second R_A can be picked and the process repeated again if a still smaller D is desired. With experience, the temperature sensitivity is generally below 0.005%/°C. at this point or earlier, based on measurements at the temperature extremes, and the variation of current from one extreme to the other is generally smooth and unidirectional.

While the invention has been disclosed in connection with certain embodiments it is not to be construed as limiting, but is susceptible to various changes and modifications, without departing from the spirit and scope of the invention as described in the specification and defined by the appended claims.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. An electrical circuit to regulate direct current with temperature compensation, comprising a field-effect transistor (FET), a second semiconductor and two resistors, the source lead of the said FET connected to one side of each of said resistors, said second semiconductor connected between the opposite sides of said resistors, the FET gate connected to one side of said second semiconductor, the other side of said second semiconductor connected to one end of the series combination of the voltage source and the load to be regulated, and the FET drain connected to the other end of said series combination of the said voltage source and the said load.

2. An electrical circuit in accordance with claim 1 wherein said second semiconductor is a diode, the said FET is an N-channel field-effect transistor, the said FET gate connected to the anode side of said diode with the cathode side of said diode connected to the negative end of said series combination of voltage source and load, and the said FET drain connected to the positive end of said series combination of voltage source and load.

3. An electrical circuit in accordance with claim 1 wherein said second semiconductor is a diode, the said

FET is a P-channel field-effect transistor, the said FET gate connected to the cathode side of said diode with the anode side of said diode connected to the positive end of said series combination of voltage source and load, and the said FET drain connected to the negative end of said series combination of voltage source and load.

4. An electrical circuit in accordance with claim 1 wherein said second semiconductor is a thermistor.

5. An electrical circuit in accordance with claim 1 wherein said second semiconductor is a transistor, appropriately biased by resistors.

6. An electrical circuit to regulate direct current with temperature compensation, comprising a field-effect transistor (FET), a second semiconductor and two resistors, the first of said resistors shunted by a series combination of said second semiconductor and the second of said resistor, the FET gate connected to one side of said first resistor and to one end of the series combination of voltage source and load to be regulated, the FET source lead connected to the other side of said first resistor, and the FET drain connected to the other end of said series combination of the said voltage source and the said load.

7. An electrical circuit in accordance with claim 6 wherein said second semiconductor is a diode, the FET is an N-channel field-effect transistor, the FET gate connected to the cathode end of said series combination of said diode and said second resistor and to the negative end of said series combination of voltage source and load, the FET source lead connected to the anode end of said series combination of said diode and said second resistor, and the FET drain connected to the positive end of said series combination of voltage source and load.

8. An electrical circuit in accordance with claim 6 wherein said second semiconductor is a diode, the FET is a P-channel field-effect transistor, the FET gate connected to the anode end of said series combination of said diode and said second resistor and to the positive end of said series combination of voltage source and load, the FET source lead connected to the cathode end of said series combination of said diode and said second resistor, and the FET drain connected to the negative end of said series combination of voltage source and load.

9. An electrical circuit in accordance with claim 6 wherein said second semiconductor is a thermistor.

10. An electrical circuit in accordance with claim 6 wherein said second semiconductor is a transistor, appropriately biased by resistors.

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