(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

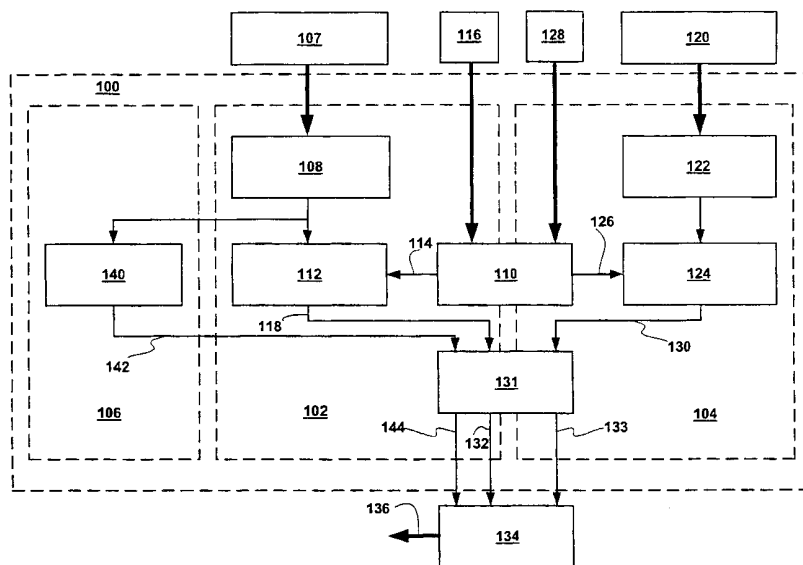**(19) World Intellectual Property Organization**
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WO 01/67208 A3

(54) Title: METHOD AND APPARATUS FOR ADAPTIVE CO-VERIFICATION OF SOFTWARE AND HARDWARE DESIGNS

(57) Abstract: A simulation system (100) is provided for simulating behavior of a device for implementing an algorithm using a software model (107) and a hardware model (120) which are converted to a common programming language and mathematical notation. The simulation system (100) uses the same input user interface (110) for the software model (107) and the hardware model (120). Further, the simulation system (100) uses the same output user interface for generating the simulation results for both the software model (107) and the hardware model (120) in the common programming language and mathematical notation, thereby allowing a user to easily verify and analyze the software and hardware simulation results (133) for optimization of the device.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER	

IPC(7) : G06F 9/455, 17/50, 19/00
US CL : 703/2, 14, 22; 709/102; 716/5
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED	

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 703/2, 13, 14, 22; 709/102, 104; 712/28; 716/1, 5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IEL/IEEE, STN: USPATFULL, INSPEC, EUROPATFULL

C. DOCUMENTS CONSIDERED TO BE RELEVANT	

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US 6,086,628 A (DAVE et al) 11 July 2000, Background of the Invention, Summary of the Invention.	1-10
A, P	US 6,097,886 A (DAVE et al) 01 August 2000, Background of the Invention, Summary of the Invention.	1-10
X	ELES et al., P. VHDL System-Level Specification and Partitioning in a Hardware/Software Co-Synthesis Environment, Proceedings of the Third International Symposium on Hardware/Software Codesign, 1994, pages 49-55.	1-10

[X] Further documents are listed in the continuation of Box C.		[ ] See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	
"E" earlier document published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 AUGUST 2001	13 SEP 2001
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INTERNATIONAL SEARCH REPORT

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ALLARA et al., A. A Flexible Model for Evaluating the Behavior of Hardware/Software Systems, Proceedings of the International Workshop on Hardware/Software Codesign, 1997, CODES/CASHE '97, pages 109-114.	1-10
X	EGOLF et al., T.W. Fixed-Point Co-Design in DSP, VLSI SIgnal Processing, VII, 1994, pages 113-126.	1-10