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(54) **Title**: HIGH DENSITY MEMORY ARCHITECTURE USING BACK SIDE METAL LAYERS

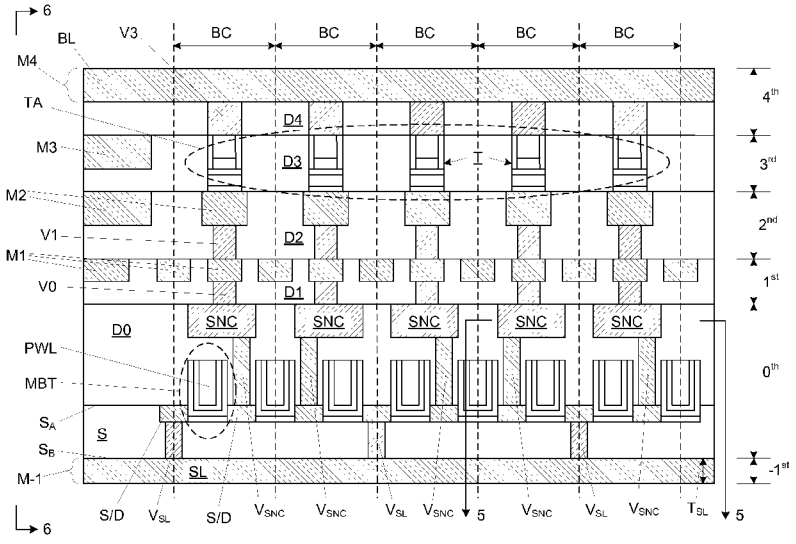

FIG. 4

(57) **Abstract**: A microelectronic memory having metallization layers formed on a back side of a substrate, wherein the metallization layers on back side may be used for the formation of source lines and word lines. Such a configuration may allow for a reduction in bit cell area, a higher memory array density, and lower source line and word line resistances. Furthermore, such a configuration may also provide the flexibility to independently optimize interconnect performance for logic and memory circuits.

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HIGH DENSITY MEMORY ARCHITECTURE USING BACK SIDE METAL LAYERS

TECHNICAL FIELD

Embodiments of the present description relate to the field of microelectronic devices, and, more particularly, to the fabrication of non-volatile microelectronic memory, which include a least one back side metal layer.

BACKGROUND

Modern microelectronic processors, such as central processing units (CPUs), use embedded cache memory to speed up the performance of the microelectronic processor and/or to meet memory bandwidth requirements, such as with System-on-Chip (SoC) devices. To implement an embedded cache memory with the highest level of integration density, as many bit cells as possible are placed on each bit line, source line and word line of the embedded cache memory. As will be understood to those skilled in the art, the lengths of bit line and word line increase proportionally with the number of bit cells on each. For example, the typical lengths of bit line and word line in an embedded cache memory can be in the order of tens of micrometers in a 22nm logic process technology. However, the use of long bit lines and word lines may result in the performance of embedded cache memory becoming ever more increasingly sensitive to interconnect resistance, particularly as the size of the embedded cache memory is scaled down and width of the bit lines and word lines reduces. Such resistance may be particularly problematical for resistance-based memory technologies, such as Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) and ReRAM (Resistive Random Access Memory), wherein reducing source line, bit line, and word line resistances with the minimum bit cell area has become one of the top challenges for successful integration of these resistance-based memory technologies. Therefore, there is a need to develop new memory architectures for resistance-based memory to alleviate performance and density limitations caused by high source line and word line resistance and to accommodate limited pitch scaling of the widths of the bit lines and word lines.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the

accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The present disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 illustrates side cross sectional view of a microelectronic memory, as known in the art.

FIG. 2 illustrates side cross sectional view of source lines and storage node contacts of the microelectronic memory along line 2-2 of FIG. 1, as known in the art.

FIG. 3 illustrates side cross sectional view of a microelectronic memory along line 3-3 of FIG. 1, as known in the art.

FIG. 4 illustrates side cross sectional view of a microelectronic memory having at least one metallization layer formed proximate a back side of a substrate, according to an embodiment of the present description.

FIGs. 5a and 5b illustrates side cross sectional view of source lines and storage node contacts of the microelectronic memory having at least one metallization layer formed proximate a back side of a substrate, viewed along line 5-5 of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates side cross sectional view of a microelectronic memory along line 6-6 of FIG. 3, according to an embodiment of the present description.

FIG. 7 illustrates side cross sectional view of a word line strap of the microelectronic memory along line 7-7 of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a computing device in accordance with one implementation of the present description.

DESCRIPTION OF EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is

included in at least one implementation encompassed within the present description. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

The terms "over", "to", "between" and "on" as used herein may refer to a relative position of one layer or component with respect to other layers or components. One layer/component "over" or "on" another layer/component or bonded "to" another layer/component may be directly in contact with the other layer/component or may have one or more intervening layers/components. One layer/component "between" layers/components may be directly in contact with the layers/components or may have one or more intervening layers/components.

It is understood that the cross-sectional view may not be a perfect cross-sectional view in the strict sense, as portions of microelectronic memory may not be shown in order to not block the view of components, which allows for an understand of the positions of the relevant components. Furthermore, for the purpose of clarity and conciseness, various layers, components, and materials are not shown (such as diffusion barriers, adhesion/wetting layers, barrier liners, conductive fill materials, and the like).

FIG. 1 illustrates a cross-sectional view of a portion of a microelectronic memory 100, as known in the art. The microelectronic memory 100 may include a plurality of levels, illustrated as 0^{th}, 1^{st}, 2^{nd}, 3^{rd} and 4^{th}. The 0^{th} level may include a substrate S having an front side S_f and an opposing back side S_b. A plurality of memory bitcell transistors MBT may be formed on and/or in the substrate S at the front side S_f thereof. The memory bitcell transistors MBT each include a word line, such as a polysilicon word line PWL, as a part of the memory bitcell transistors MBT. A plurality of source/drain structures S/D may be formed in the substrate S for the operation of the memory bitcell transistors MBT. The source/drain structures S/D may be formed by doping the substrate S with an appropriate n-type or p-type dopant, as will be understood to those skilled in the art. The components, structure, and functioning of such memory bitcell transistors MBT

are well known in the art, and, for the sake of brevity and conciseness, will not be described herein. A dielectric material D0 may be formed over the substrate front side S_f and the memory bitcell transistors MBT and a metallization layer M0 may be formed on or in the dielectric material D0, wherein the metallization layer M0 may be used to form source lines SL and storage node contacts SNC, as well as other signal routing structures (not shown). The source lines SL may be connected to their respective source/drain structure S/D with a source line conductive via V_{SL} and the storage node contacts SNC may be connected to their respective source/structure S/D with a storage node contact via V_{SNC}.

As further shown in FIG. 1, at least one addition level, shown as the 1st level and the 2nd level may be formed, respectively, on the 0th level. The 1st level may include a metallization layer M1 (traces/lines) that may be in communication with respective storage node contacts SNC through vias V0 extending through the dielectric layer D1 and the 2nd level may include a metallization layer M2 (trace/lines) that may be in communication with respective storage node contacts SNC through vias V1 extending through the dielectric layer D2.

The microelectronic memory 100 may include a plurality of memory cell transistors T (illustrated as magnetic tunnel junction transistors) in an array TA. The memory cell transistors T are illustrated as being formed in the 3rd level and may each be connected to storage node contacts SNC through the metallization layers M1 and M2, and vias V0 and V1, of the 1st level and the 2nd level, respectively.

As further shown in FIG. 1, the 4th level may be formed on the 3rd level, wherein the 4th level may include a metallization layer M4 including a bit line BL, wherein the bit line BL is electrically connected to the memory cell transistors T through vias V3 extending through a dielectric layer D4 of the 4th level.

FIG. 2 illustrates the top cross-sectional view of the metallization layer M0 of the 0th level illustrating the source lines SL and storage node contacts SNC, and the demarcation of bit cells BC with dash lines (see also FIG. 1). As illustrated, the formation of the source lines SL and the storage node contacts SNC within the metallization layer M0 may limit the dimension of each bit cell BC. As shown, a bit cell height BCH is equal to two times of a pitch P (center-to-center distance between the structures) or 4F, where F is a half pitch P of the structures. As the bit cell height BCH is limited by the pitch P, widths of the structures (i.e. the source line width W_{SL} and the storage node contact width W_{SNC}) may be reduced in order to reduce an area A of each bit cell BC. However, this may increase resistance and degrade performance, as will be understood to those skilled in the art. Furthermore, reducing resistances by increasing the thickness the structure may not be an option in conventional processes as dimensions of the structures are

typically determined by the performance requirement of logic circuits outside of memory area.

FIG. 3 illustrates a cross sectional view of the microelectronic memory 100 along line 3-3 of FIG. 1 with an additional level, 5th level, formed on the 4th level, and without all the structures of the 0th level for clarity. The 5th level may include a dielectric layer D5 and a metallization layer M5, wherein the metallization layer includes a word line WL. The word line WL may be electrically connected to the metallization layer M4 through at least one via V4 extending through the dielectric layer D5. As illustrated in FIG. 3, the microelectronic memory 100 would have a word strap line WL_{strap} that would extend from the poly word line PWL of the 0th level to the word line WL of the 5th level through the various metallizations (e.g. M0, M1, M2, M3, and M4) and vias (e.g. V_{poly}, V0, V1, V2, V3, and V4). As will be understood to those skilled in the art, the placement of the word line strap WL_{strap} interrupts the memory cell transistor array TA in the 3rd level, and, as there will be numerous word line straps WL_{strap} within the microelectronic memory in order reduce word line resistance and deal, the word line straps WL_{strap} may have a significant impact on a density of the memory cell transistor array TA.

The dielectric layers (e.g. D0-D5) may be any appropriate dielectric material, including but not limited to, silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4) and silicon carbide (SiC), liquid crystal polymer, epoxy resin, bismaleimide triazine resin, polyimide materials, and the like, as well as low-k and ultra low-k dielectrics (dielectric constants less than about 3.6), including but not limited to carbon doped dielectrics, fluorine doped dielectrics, porous dielectrics, organic polymeric dielectrics, silicon based polymeric dielectrics, and the like, and may be formed by any known technique, including, but not limited, chemical vapor deposition, physical vapor deposition, coating, lamination, and the like.

The metallization layers (e.g. M0-M5) and vias (e.g. V_{poly} and V0-V4) may be made by any known process, such as photolithography and plating, and may be any appropriate conductive material, such as metals, including but not limited to copper, silver, nickel, gold, aluminum, tungsten, cobalt, and alloys thereof, and the like. The substrate S may be any appropriate substrate, including, but not limited to, a silicon-containing substrate.

Embodiments of the present description relate to forming a microelectronic memory having metallization layers formed on a back side of a substrate, wherein the metallization layers may be used for the formation of source lines and word lines. Such a configuration may allow for a reduction in bit cell area, a higher memory array density, and lower source line and word line resistances. Furthermore, such a configuration may also provide the flexibility to independently optimize interconnect performance for logic and memory circuits.

As illustrated in FIG. 4, a microelectronic memory 150 may be formed with the source line

SL proximate the substrate back side S_b within a metallization layer M-1 of a -1th level. By moving the source line SL from a position proximate the substrate front side S_f to a position proximate the substrate back side S_b, the bit cell area A (see FIG. 5a and 5b) may be reduced as the source lines SL are no longer required to be in the same metallization as the storage node contacts SNC, as shown in FIG. 2, which will enable higher bit cell BC performance by reducing resistances.

As further shown in FIG. 4, the source line SL may be connected to the source/drain structure S/D through a deep diffusion contact DDC. The deep diffusion contact DDC may be formed by implanting a n-type dopant or a p-type dopant into the substrate S, as will be understood to those skilled in the art.

FIGs. 5a and 5b illustrate a view along line 5-5 of FIG. 4 showing only the source lines SL and the storage node contacts SNC without any intervening structures, so that the relative positions and sizes of the source lines SL and the node contacts SNC can be seen. As shown in FIG. 5a, the source line width W_{SL} can be optimized for a high-speed application, wherein the source line width W_{SL} can be increased by up to 3 times compared to the source line width W_{SL} of FIG. 3, while maintaining the same area A of each bit cell BC, wherein the storage node contacts SNC are position directly, vertically over the source line SL. The increase in the source line width W_{SL} can reduce the resistance thereof and result in increased read and write margin and increased speed, as will be understood to those skilled in the art. Furthermore, a thickness T_{SL} of source line SL (see FIG. 4) can be further optimized to reduce source line resistance for resistance based memory.

As shown in FIG. 5b, the source line width W_{SL} can be sized at its minimum for a high-density application, wherein the storage node contacts SNC may have a storage node contact width W_{SNC} substantially the same as the source line width W_{SL} and wherein the storage node contacts SNC may be positioned directly, vertically over the source line SL. This configuration allows for a reduction of the bit cell height BCH by as much as two times as compared to the bit cell height BCH of FIG. 2. Again, the thickness T_{SL} of source line SL (see FIG. 4) can be further optimized to reduce source line resistance for resistance based memory.

FIG. 6 illustrates a cross sectional view of the microelectronic memory 150 along line 6-6 of FIG. 4 with an additional level, -2nd level, formed on the -1st level. The -1st level may include a dielectric layer D-1 and the -2nd level may include a metallization layer M-2, wherein the metallization layer includes the word line WL. The word line WL may be electrically connected to the metallization layer M-1 through at least one via V-1 extending through the dielectric layer D-1. A thickness T_{WL} of word line WL can be optimized to reduce word line delay.

As illustrated in FIG. 6, the microelectronic memory 150 would have the word line strap WL_{strap} that would extend through the 0^{th} level, the -1^{st} level, and the -2^{nd} level. FIG. 7, which is a cross sectional view along line 7-7 of FIG. 5, illustrates the word line strap WL_{strap} in greater detail without the dielectric layers. As shown in FIG. 7, the word line strap WL_{strap} comprises an electrical path between the word line WL and the polysilicon word line PWL through the previously described structures including the deep diffusion contacts DDC and the source/drain structure S/D without additional area in substrate. Furthermore, the word line straps WL_{strap} no longer disrupt the memory cell transistor array TA, as previously discussed.

FIG. 8 illustrates a computing device 200 in accordance with one implementation of the present description. The computing device 200 houses a board 202. The board may include a number of microelectronic components, including but not limited to a processor 204, at least one communication chip 206A, 206B, volatile memory 208, (e.g., DRAM), non-volatile memory 210 (e.g., ROM), flash memory 212, a graphics processor or CPU 214, a digital signal processor (not shown), a crypto processor (not shown), a chipset 216, an antenna, a display (touchscreen display), a touchscreen controller, a battery, an audio codec (not shown), a video codec (not shown), a power amplifier (AMP), a global positioning system (GPS) device, a compass, an accelerometer (not shown), a gyroscope (not shown), a speaker (not shown), a camera, and a mass storage device (not shown) (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the microelectronic components may be physically and electrically coupled to the board 202. In some implementations, at least one of the microelectronic components may be a part of the processor 204.

The communication chip enables wireless communications for the transfer of data to and from the computing device. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device may include a plurality of communication chips. For instance, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless

communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

Any of the microelectronic components within the computing device 400 having embedded memory may include metallization layers proximate the substrate back side of the embedded memory, as described herein.

In various implementations, the computing device may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device may be any other electronic device that processes data.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-8. The subject matter may be applied to other microelectronic device and assembly applications, as will be understood to those skilled in the art.

The following examples pertain to further embodiments, wherein Example 1 is a conductive connector, comprising a microelectronic memory comprising a substrate having a front surface and an opposing back surface, a source line proximate the substrate back surface; and a memory bitcell transistor proximate the substrate front surface.

In Example 2, the subject matter of Example 1 can optionally include the memory bitcell transistor including at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure.

In Example 3, the subject matter of Example 2 can optionally include the source line being electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

In Example 4, the subject matter of any of Examples 1 to 3 can optionally include a word line formed proximate the substrate back surface.

In Example 5, the subject matter of Example 4 can optionally include a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor.

In Example 6, the subject matter of Example 5 can optionally include the word line proximate the substrate back surface being electrically connected to a word line within a memory

bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

In Example 7, the subject matter of any of Examples 1 to 4 can optionally include a memory cell transistor array proximate the substrate front surface.

In Example 8, the subject matter of Example 7 can optionally include the memory cell transistor array comprising a plurality of resistance based memory transistors.

In Example 9, the subject matter of Example 8 can optionally include the plurality of resistance based memory transistors comprising a plurality of Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) transistors.

In Example 10, the subject matter of Example 8 can optionally include the plurality of resistance based memory transistors comprising a plurality of ReRAM (Resistive Random Access Memory).

The following examples pertain to further embodiments, wherein Example 11 is a microelectronic memory comprising a substrate having a front surface and an opposing back surface, a word line proximate the substrate back surface, and a memory bitcell transistor proximate the substrate front surface.

In Example 12, the subject matter of Example 11 can optionally include a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor.

In Example 13, the subject matter of Example 11 can optionally include the word line proximate the substrate back surface being electrically connected to a word line within a memory bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

In Example 14, the subject matter of Example 11 can optionally include a source line formed proximate the substrate back surface.

In Example 15, the subject matter of Example 14 can optionally include the memory bitcell transistor including at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure.

In Example 16, the subject matter of Example 15 can optionally include the source line being electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

In Example 17, the subject matter of Example 11 to 16 can optionally include a transistor array proximate the substrate front surface.

In Example 18, the subject matter of Example 17 can optionally include the transistor array

comprising a plurality of resistance based memory transistors.

In Example 19, the subject matter of Example 18 can optionally include the plurality of resistance based memory transistors comprising a plurality of Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) transistors.

In Example 20, the subject matter of Example 18 can optionally include the plurality of resistance based memory transistors comprising a plurality of ReRAM (Resistive Random Access Memory).

The following examples pertain to further embodiments, wherein Example 21 is an electronic system, comprising a board; and a microelectronic component attached to the board, wherein the microelectronic component includes a microelectronic memory comprising: a substrate having a front surface and an opposing back surface; a source line proximate the substrate back surface; a memory bitcell transistor proximate the substrate front surface, wherein the memory bitcell transistor includes at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure; a word line formed proximate the substrate back surface; a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor; and a memory cell transistor array proximate the substrate front surface.

In Example 22, the subject matter of Example 21 can optionally include the source line being electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

In Example 23, the subject matter of Example 21 can optionally include the word line proximate the substrate back surface being electrically connected to a word line within a memory bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

In Example 24, the subject matter of Example 21 can optionally include the memory cell transistor array comprising a plurality of resistance based memory transistors.

In Example 25, the subject matter of Example 24 can optionally include the plurality of resistance based memory transistors comprising a plurality of Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) transistors.

In Example 26, the subject matter of Example 24 can optionally include the plurality of resistance based memory transistors comprising a plurality of ReRAM (Resistive Random Access Memory).

Having thus described in detail embodiments of the present description, it is understood that the present description defined by the appended claims is not to be limited by particular

details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic memory comprising:
a substrate having a front surface and an opposing back surface;
a source line proximate the substrate back surface; and
a memory bitcell transistor proximate the substrate front surface.

2. The microelectronic memory of claim 1, wherein the memory bitcell transistor includes at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure.

3. The microelectronic memory of claim 2, wherein the source line is electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

4. The microelectronic memory of any of claims 1 to 3, further including a word line formed proximate the substrate back surface.

5. The microelectronic memory of claim 4, further including a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor.

6. The microelectronic memory of claim 5, wherein the word line proximate the substrate back surface is electrically connected to a word line within a memory bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

7. The microelectronic memory of any of claims 1 to 4, further comprising a memory cell transistor array proximate the substrate front surface.

8. The microelectronic memory of claim 7, wherein the memory cell transistor array comprises a plurality of resistance based memory transistors.

9. The microelectronic memory of claim 8, wherein the plurality of resistance based

memory transistors comprises a plurality of Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) transistors.

10. The microelectronic memory of claim 8, wherein the plurality of resistance based memory transistors comprises a plurality of ReRAM (Resistive Random Access Memory).

11. A microelectronic memory comprising:
a substrate having a front surface and an opposing back surface;
a word line proximate the substrate back surface; and
a memory bitcell transistor proximate the substrate front surface.

12. The microelectronic memory of claim 11, further including a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor.

13. The microelectronic memory of claim 11, wherein the word line proximate the substrate back surface is electrically connected to a word line within a memory bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

14. The microelectronic memory of claim 11, further including a source line formed proximate the substrate back surface.

15. The microelectronic memory of claim 14, wherein the memory bitcell transistor includes at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure.

16. The microelectronic memory of claim 15, wherein the source line is electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

17. The microelectronic memory of any of claims 11 to 16, further comprising a transistor array proximate the substrate front surface.

18. The microelectronic memory of claim 17, wherein the transistor array comprises a

plurality of resistance based memory transistors.

19. The microelectronic memory of claim 18, wherein the plurality of resistance based memory transistors comprises a plurality of Spin-Transfer Torque (STT) MRAM (Magnetoresistive Random Access Memory) transistors.

20. The microelectronic memory of claim 18, wherein the plurality of resistance based memory transistors comprises a plurality of ReRAM (Resistive Random Access Memory).

21. An electronic system, comprising:

a board; and

a microelectronic component attached to the board, wherein the microelectronic component includes a microelectronic memory comprising:

a substrate having a front surface and an opposing back surface;

a source line proximate the substrate back surface;

a memory bitcell transistor proximate the substrate front surface, wherein the memory bitcell transistor includes at least one source/drain structure formed in the substrate, wherein the source line is electrically connected to the at least one source/drain structure;

a word line formed proximate the substrate back surface;

a word line strap comprising the word line proximate the substrate back surface electrically connected to a word line within a memory bitcell transistor; and

a memory cell transistor array proximate the substrate front surface.

22. The electronic system of claim 21, wherein the source line is electrically connected to the at least one source/drain structure through a deep diffusion contact within the substrate.

23. The electronic system of claim 21, wherein the word line proximate the substrate back surface is electrically connected to a word line within a memory bitcell transistor through a source/drain structure and a deep diffusion contact within the substrate.

24. The electronic system of claim 21, wherein the memory cell transistor array comprises a plurality of resistance based memory transistors.

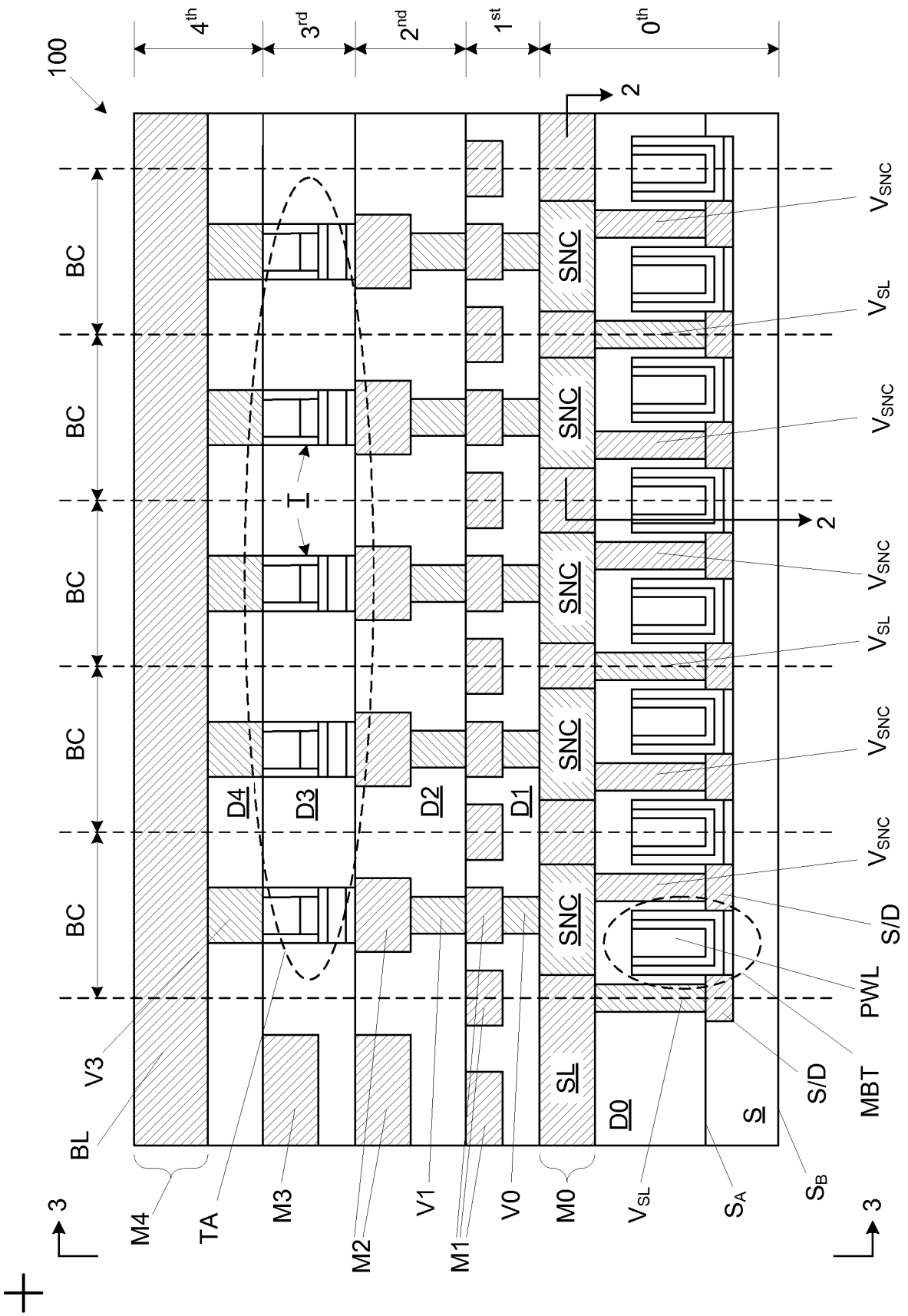

FIG. 1 (Prior Art)

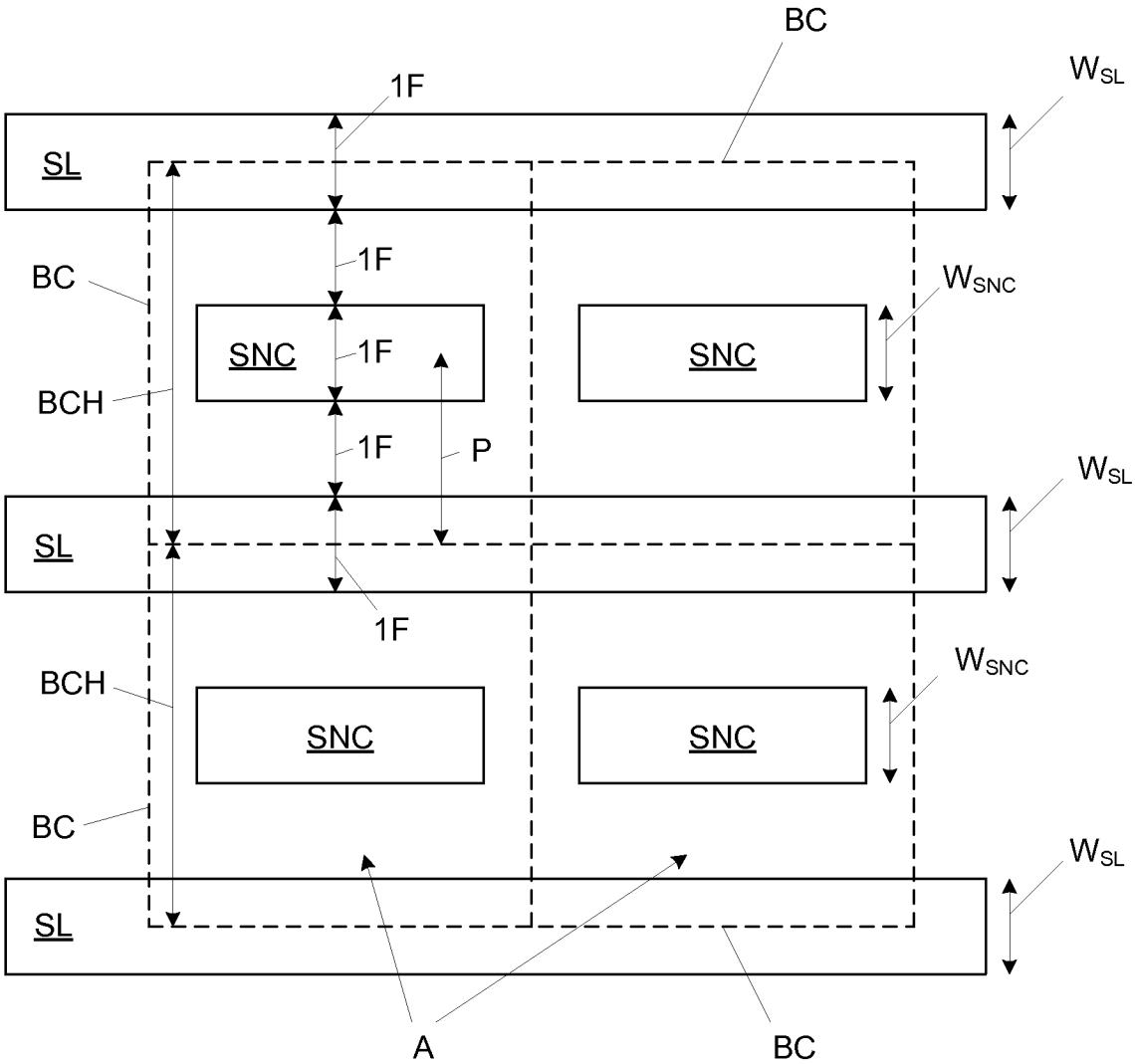

FIG. 2 (Prior Art)

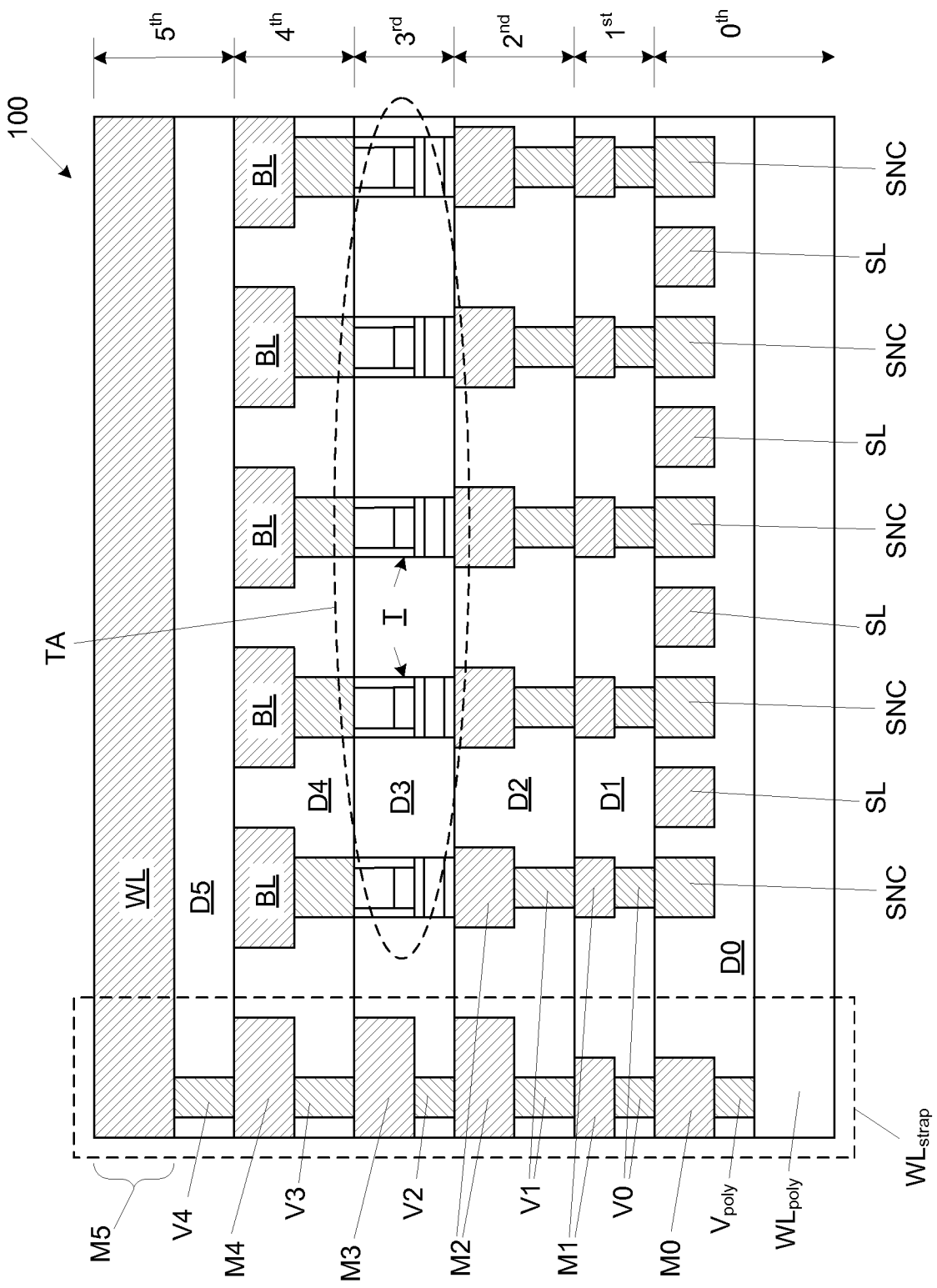

FIG. 3 (Prior Art)

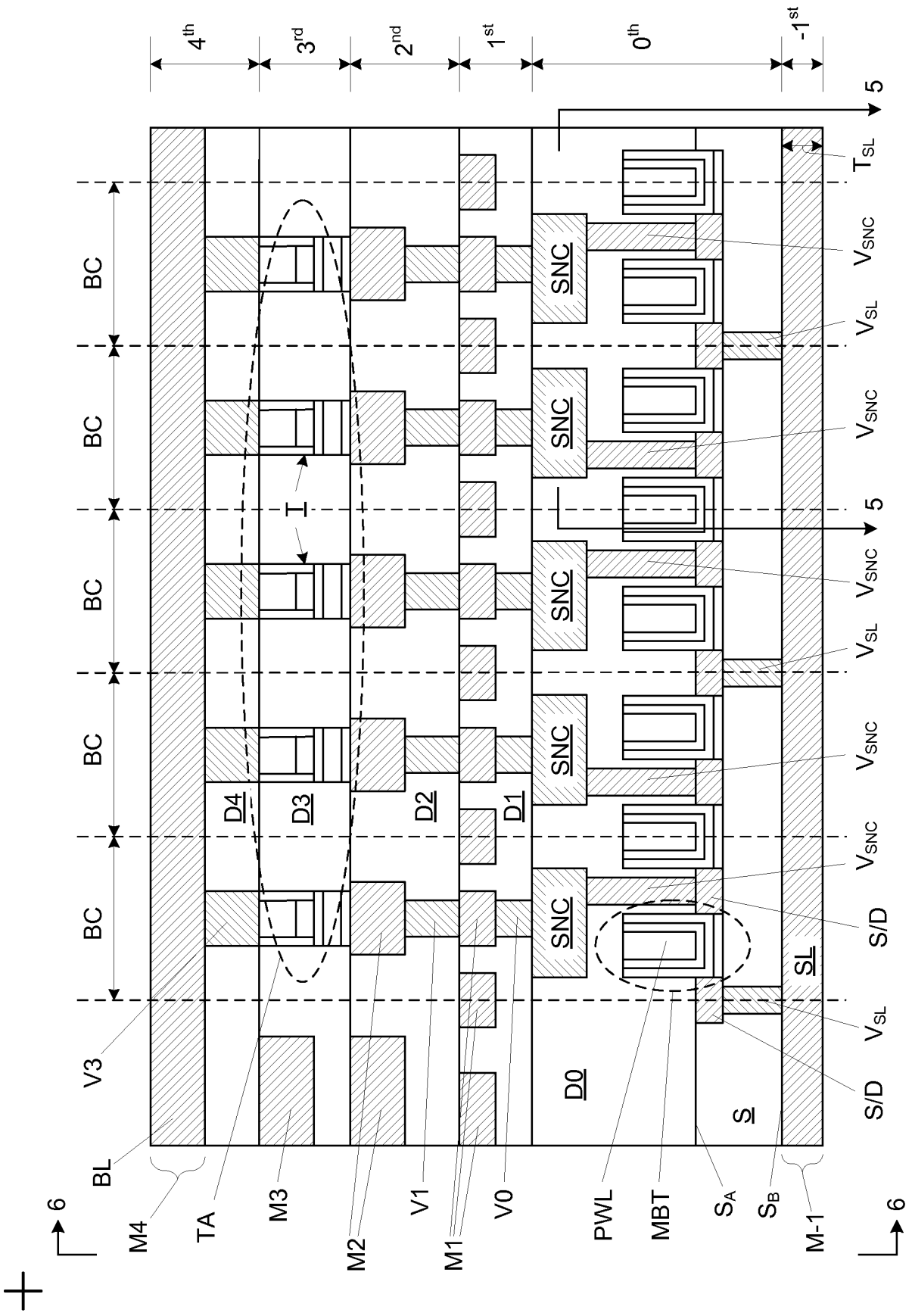
4th
3rd
2nd
1st
0th
-1st
5
5
6
6
BC
BC
BC
BC
BC
BC
I
D4
D3
D2
D1
D0
SNC
SNC
SNC
SNC
SNC
SL
S
V3
BL
M4
TA
M3
M2
V1
M1
V0
PWL
MBT
S_A
S_B
M-1
S/D
S/D
V_{SL}
V_{SNC}
V_{SL}
V_{SNC}
V_{SNC}
V_{SL}
V_{SNC}
V_{SNC}
T_{SL}

FIG. 4

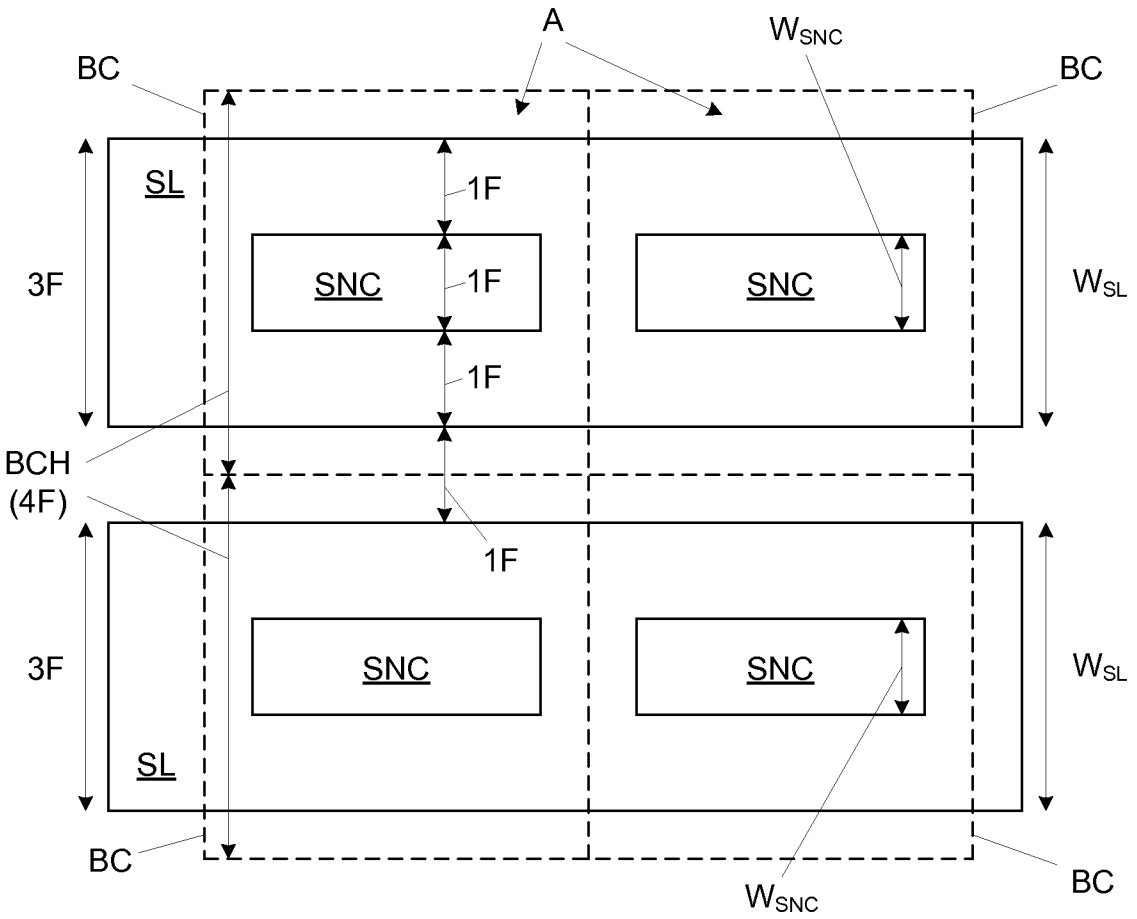
A
W_{SNC}
BC
BC
SL
1F
3F
SNC
1F
SNC
W_{SL}
1F
BCH
(4F)
1F
3F
SNC
SNC
W_{SL}
SL
BC
W_{SNC}
BC

FIG. 5a

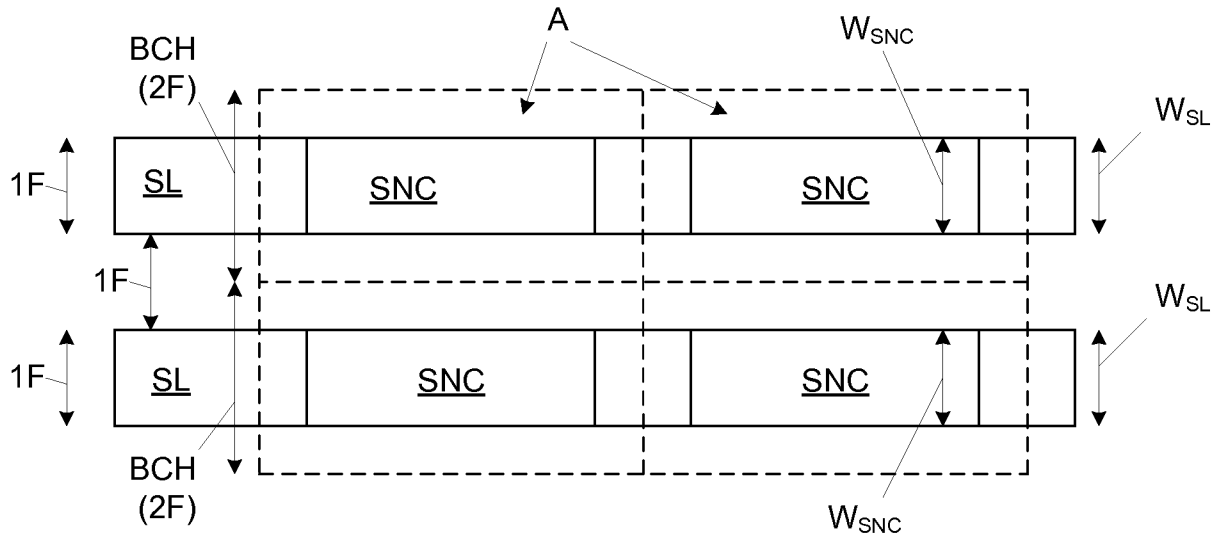
A
W_{SNC}
BCH
(2F)
W_{SL}
1F
SL
SNC
SNC
1F
W_{SL}
1F
SL
SNC
SNC
BCH
(2F)
W_{SNC}

FIG. 5b

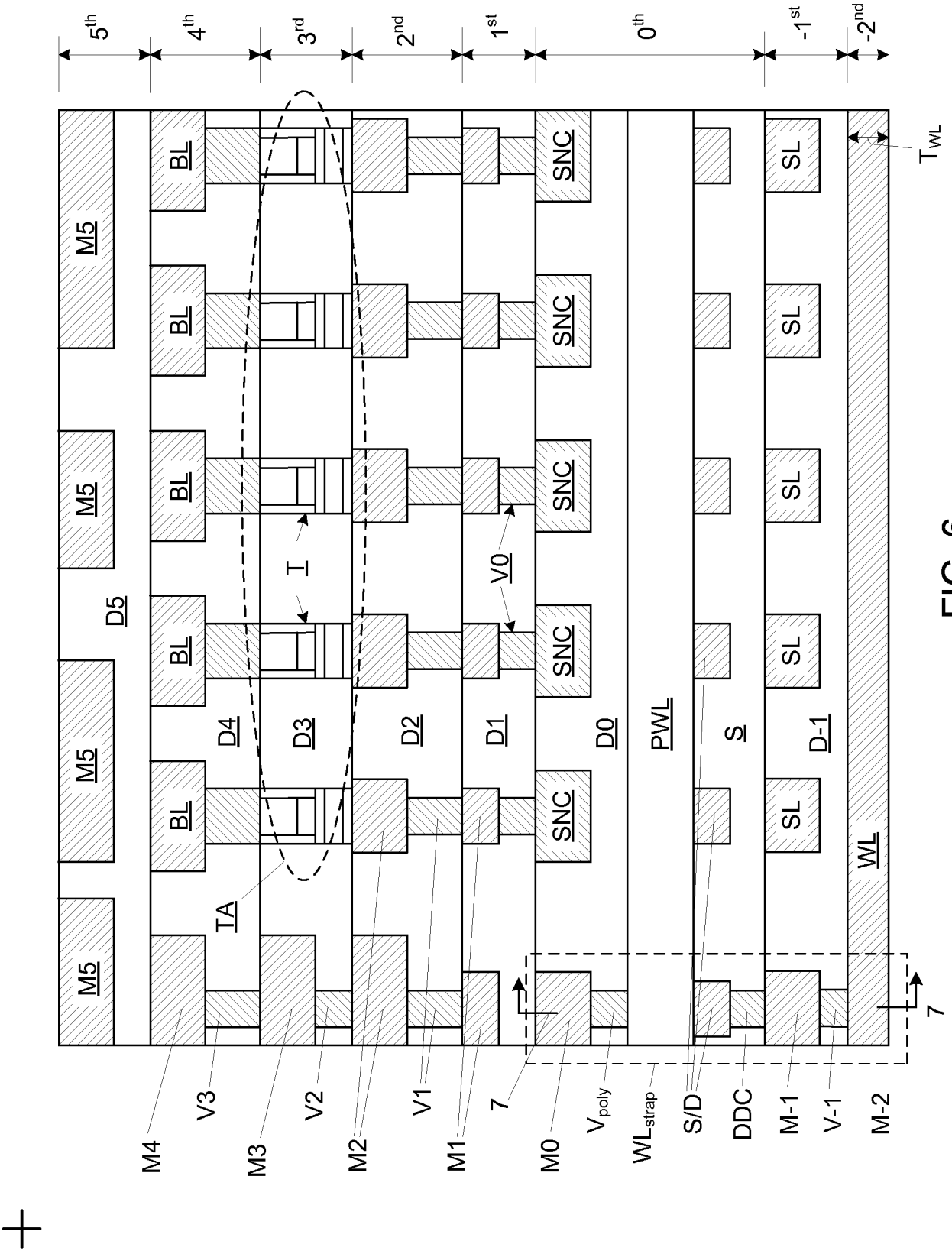
5th
4th
3rd
2nd
1st
0th
-1st
-2nd
M5
BL
SNC
SL
WL
T_{WL}
D5
D4
D3
D2
D1
D0
PWL
S
D-1
TA
I
V0
7
M4
V3
M3
V2
M2
V1
M1
M0
V_{poly}
WL_{strap}
S/D
DDC
M-1
V-1
M-2

FIG. 6

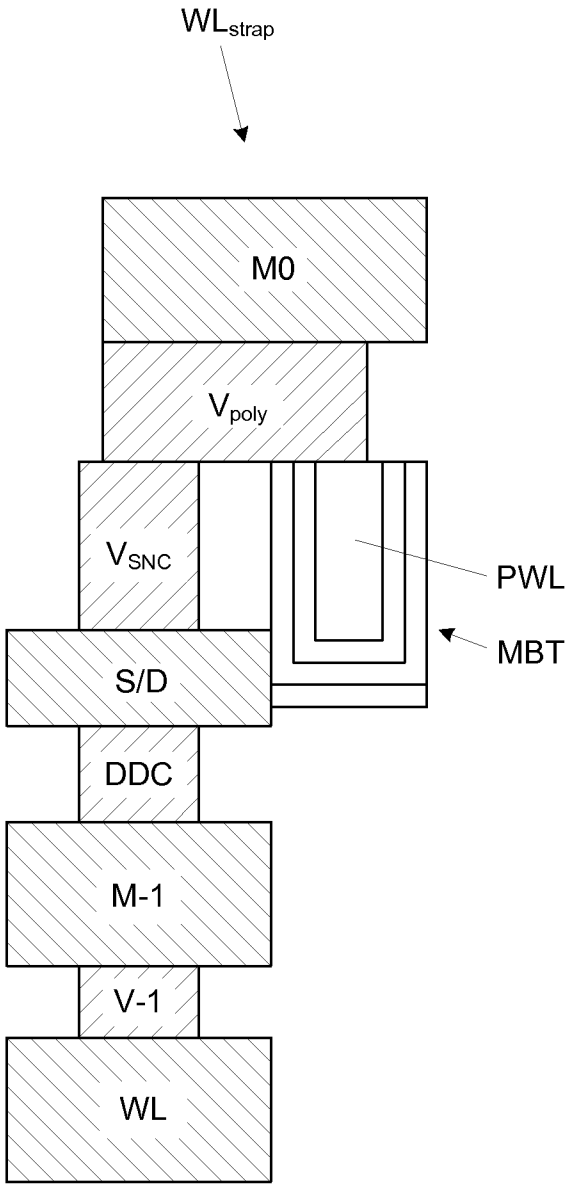

FIG. 7

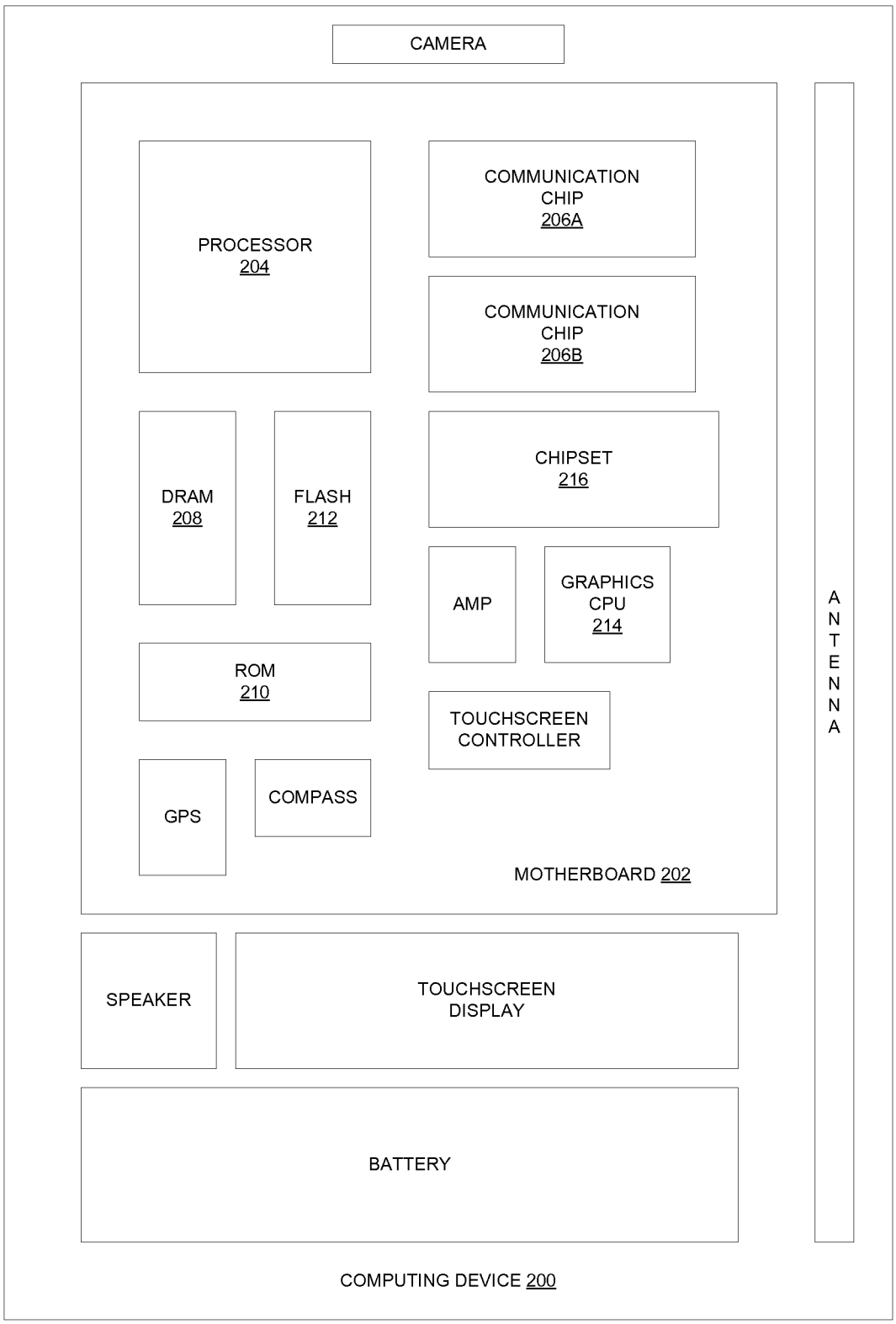
CAMERA
PROCESSOR
204
COMMUNICATION
CHIP
206A
COMMUNICATION
CHIP
206B
DRAM
208
FLASH
212
CHIPSET
216
AMP
GRAPHICS
CPU
214
ROM
210
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD 202
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE 200

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/033757

A. CLASSIFICATION OF SUBJECT MATTER

G11C 13/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 13/00; G11C 11/56; H01L 21/8222; H01L 29/94; H01L 23/48; H01L 21/02; H01L 45/00; H01L 23/522

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: microelectronic, memory, substrate, front, back, surface, source, word, line, board, bitcell, transistor, ReRAM, MRAM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0230735 A1 (HUILONG ZHU) 16 September 2010 See paragraphs [0003], [0006], [0032], [0034], [0058]; and figure 10D.	1-2,4-5,11-12 ,14-15,17
Y		18-21,24
A		3,6,13,16,22-23
Y	US 2014-0264235 A1 (SHUNQIANG GONG et al.) 18 September 2014 See paragraph [0029]; and figure 2.	18-20,24
Y	US 2013-0051115 A1 (WILLIAM G. EN et al.) 28 February 2013 See paragraphs [0004], [0022]-[0024]; and figures 1, 3.	21,24
A	US 2007-0275533 A1 (KUNAL VAED et al.) 29 November 2007 See paragraph [0033]; and figure 2.	1-6,11-24
A	US 8952500 B2 (CHAO-YUAN HUANG et al.) 10 February 2015 See column 4, lines 58-66; and figure 3B.	1-6,11-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 February 2016 (24.02.2016)	**02 March 2016 (02.03.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/033757

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 8-10
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 8-10 refer to unsearchable claim 7.

3. ☒ Claims Nos.: 7
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/033757

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0230735 A1	16/09/2010	US 8361875 B2	29/01/2013
US 2014-0264235 A1	18/09/2014	CN 104051491 A	17/09/2014
		TW 201448172 A	16/12/2014
		US 09111941 B2	18/08/2015
US 2013-0051115 A1	28/02/2013	None	
US 2007-0275533 A1	29/11/2007	CN 101079441 A	28/11/2007
		CN 101079441 B	24/11/2010
		US 7622357 B2	24/11/2009
US 8952500 B2	10/02/2015	US 2014-264912 A1	18/09/2014