ABSTRACT

A four-level FLASH memory device includes an array of singularly addressable preliminarily erased memory cells, with each memory cell capable of storing a two-bit datum. When the threshold voltage of a memory cell is verified to have reached the desired distribution, the cell is read using a test read voltage smaller than or equal to the program voltage. In this situation the voltage $V_s$ on the source node is negligible, and the programmed state of the cell may be correctly verified.
FIG. 4
FIG. 5

Reduced read margin

Sample modulation effect

VVER
VERIFICATION

LSB LATCH

THIRD LATCH

FIG. 10

* WE HAVE 0 IF CELL THRESHOLD VOLTAGE IS UNDER VVFY1-A
Figure 11

Program/verify only cells with threshold voltage under VVFY1-A.
FIG. 12

LSB READ

1001

LSB LATCH

THIRD LATCH

1100

DATA LOAD

MSB LATCH

Vread0

1 1 0 1
FIG. 14

* VVFY2 A LITTLE BIT HIGHER THAN USUAL
PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY2-A

**

PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY3-A

FIG. 19

W-$AHAA RIGIOIN?A ?IÐVITO A CITOHSTIRIHL HJLIAA STITI@HO ?TNO ÄHTEIGIA/JANVYH9OH) 

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**FIG. 24**

WE HAVE A CELL THRESHOLD VOLTAGE IS UNDER VVFY1-Δ

VERIFY

**10**

LSB LATCH

**MSB LATCH**

**THIRD LATCH**
**FIG. 27**

VVFY3* A LITTLE BIT HIGHER THAN USUAL

LSB LATCH

MSB LATCH

THIRD LATCH

PROGRAM

1110

1101

1100
* PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY2- 
** PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY3-A

FIG. 32
FIG. 36

VVFY1

0

1

TRANSFER

10

LSB LATCH

MSB LATCH
FIG. 37

WE HAVE A IF CELL THRESHOLD VOLTAGE IS UNDER \( V_{TH} \)

VERIFY

10^2

LSB LATCH

MSB LATCH
* VVFY2/VVFY3 A LITTLE BIT HIGHER THAN USUAL

FIG. 40
* VVFY2+VVFY3 A LITTLE BIT HIGHER THAN USUAL

**FIG. 41**

- LSB LATCH
- MSB LATCH

Program Verify
** WE HAVE 0 IF CELL THRESHOLD VOLTAGE IS UNDER VVFY2-Δ

* WE HAVE 0 IF CELL THRESHOLD VOLTAGE IS UNDER VVFY3-Δ

1100

VERIFICATION

LSB LATCH

MSB LATCH

FIG. 44
** PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY2-Δ

** PROGRAM/VERIFY ONLY CELLS WITH THRESHOLD VOLTAGE UNDER VVFY3-Δ

FIG. 45
METHOD OF PROGRAMMING A FOUR-LEVEL FLASH MEMORY DEVICE AND A RELATED PAGE BUFFER

FIELD OF THE INVENTION

[0001] The present invention relates in general to memory devices, and in particular, to a method of programming a four-level FLASH memory and to a related page buffer for a four-level FLASH memory.

BACKGROUND OF THE INVENTION

[0002] A logic state is stored in a cell by programming its threshold voltage. In non-volatile memory devices this is done by transferring a certain electrical charge in a floating gate of the cell.

[0003] The storage capacity of memory devices can be multiplied by storing more than one bit of information in each single cell of the same physical structure as if destined to store a single information bit. This is in addition to increasing the integration density of arrays of cells individually addressable through wordlines and bit-lines of the array.

[0004] Though based on the same physical mechanisms, the programming and reading of cells that store more than one bit (multi-level cells) are carried out with techniques that differ from those used for cells that store a single bit (two-level cells).

[0005] To read a two-level memory array cell, a certain voltage is applied to the control gate (wordline) of the cell. The value of such a reading voltage is between the threshold voltage of an erased cell and the threshold voltage of a programmed cell such that when the cell is programmed, the reading voltage is lower than its threshold voltage. As a consequence, no current flows through the cell. In contrast, when the cell is erased, the reading voltage is higher than its threshold voltage and thus a current flows through the cell.

[0006] In four-level cells, two bits of information may be stored by making the programming voltages of the different thresholds that may be set for one memory cell define four different intervals. Each interval is associated to a respective two-bit datum. A reading operation is carried out by comparing an electrical parameter, correlated with the current that flows through the cell, with four distinct reference intervals. The reference intervals are defined by the three different thresholds that may be programmed for each single cell. Each one is associated to a respective two-bit datum. The logic datum associated to the distinct interval of values (threshold voltage distributions) in which the measured electrical parameter falls is thus determined.

[0007] This approach for a multi-level operation of the cells is applicable to volatile memory cells, such as DRAMs, as well as to non-volatile memory devices, such as EEPROMs and FLASH-EPROMs.

[0008] Of course, incrementing the number of information bits that may be stored in a single memory cell makes certain functioning characteristics of the memory array cells more critical, such as their immunity to disturbances (noise), to the spread of information retention characteristics, and to ensure appropriate tolerance ranges of the biasing voltages at which each cell is programmed and read.

[0009] A basic circuit scheme of two memory array bit-lines and a so-called page buffer of a four-level FLASH memory is depicted in FIG. 1 and it is described in great detail in European Patent Application No. 05106972.2. This application is assigned to the current assignee of the present invention, the contents of which are incorporated herein by reference in its entirety. The page buffer manages the operations of reading the information stored in the memory cells of a selected memory page, or of writing new information in the cells.

[0010] The page buffer includes a buffer register of the same size (capacity) of that of a memory page, in which data read (in parallel mode) from the memory cells of a selected memory page are temporarily stored, before being serially output. Similarly, when data are to be written in a memory page, the page buffer is replenished with data that are thereafter written in parallel in the memory cells of a selected memory page. Therefore, a page buffer normally includes a relatively large number of volatile storage elements, typically bistable elements or latches, in a number corresponding to the number of memory cells of the memory page.

[0011] The basic operations that usually are performed on the memory cells are a page read (an operation involving reading data from a selected memory page), a page program (writing data into a selected memory page), and an erase operation, wherein the content of the memory cells is erased.

[0012] In four-level memory devices, a two-bits datum may be stored in each cell by programming the latter in any one of four different states. Each one is associated with a corresponding logic value of the two-bits datum. Usually, the programming state of a memory cell is defined by the threshold voltage value of the transistor structure that is included in the memory cell structure.

[0013] In a memory cell adapted to store two bits, the threshold voltage values of the memory cells may assume one of four different values (or ranges of values). A typical choice is to associate said logic values of the stored bit pair to the four different states according to a binary sequence 11, 10, 01, 00 as shown in FIG. 2, corresponding to increasing threshold voltage values, with the logic value 11 being associated to the state of lowest threshold voltage value (erased state), and the others associated in succession to states of increased threshold voltage value.

[0014] Naturally, for writing data into a two-bit memory cell or for reading data therefrom, it might be necessary to perform up to three read accesses to the memory cells using different read voltage references.

[0015] A known approach for reducing the number of read accesses necessary to retrieve the stored data includes using a different association rule between logic values and states, that make use of the Gray code, as depicted in FIG. 2. In this way, the logic values are associated to the threshold states according to the binary sequence 11, 10, 00, 01 with the logic value 11 being associated to the erased state, and the others associated in succession to states of increased threshold voltage values.

[0016] The main feature of using the Gray code is the fact that adjacent programmed states (in terms of threshold voltage values) have corresponding logic values that differ from each other by only one bit.
In the ensuing description reference will be made to embodiments that employ such a coding, but the same considerations that will be made apply to any kind of coding for storing a two-bit datum in a cell of a four-level memory device.

In order to discriminate the value stored in the cell, the read voltages $V_{read0}$, $V_{read1}$ and $V_{read2}$ should be sufficiently distant from the upper and lower bounds of the distributions of the threshold voltages of the cells, as depicted in FIG. 3.

The cells of a memory page are programmed in parallel by incrementing stepwise their threshold voltage. They do not reach at the same time the desired distributions because there are cells that are faster than the others and require fewer program pulses to reach the programmed threshold. After each program pulse, the cells are read for verifying whether they have been correctly programmed or not. When a cell is found to have a threshold voltage comprised in the desired distribution, it is considered programmed and a configuration switch associated to it is opened so that the programmed cell will not receive any further program pulse.

After having programmed and verified the cells, it is often found that some cells inexplicably no longer have a threshold voltage comprised in the distribution to which they were programmed, and therefore the datum stored therein is not the correct one. More precisely, it appears that the threshold voltage of the fastest cells, that is, the cells that reached first the desired distribution have decreased while the remaining cells were given additional program pulses.

For better understanding the problem, let us refer to the circuit of FIG. 4 and consider a sample case in which all the cells of the wordline WL $<31>$ should be programmed to the logic state 10. All the cells are initially in the erased state, that is, in the state 11. The cell MC31 is subjected to program pulses until its threshold voltage surpasses the voltage $V_{VFP1}$.

This is carried out by applying the voltage $V_{VFP1}$ on the wordline WL $<31>$ and stopping to apply further program pulses to the cell MC31 when there is not anymore current flowing through the cell. In this situation, the cell MC31 is considered to have been programmed to the binary logic state 10.

Unfortunately, it may happen that the read margins, that is the difference between the lower bound voltage of the distribution corresponding to the state 10 and a pre-established read voltage $V_{read0}$ be smaller than the designed safe value ($d$).

What happens is schematically illustrated in FIG. 5. The cell is initially erased (a) and must be programmed in the state 10 while ensuring a certain read margin. Program pulses are applied to the cell (b) and a threshold voltage greater than the level $V_{VFP1}$ is eventually verified. When other cells of the same bitline have been programmed, it seems as the threshold voltage of the cell appears to have shifted to the left (c) and the read margin may become smaller than the designed safe value (d).

SUMMARY OF THE INVENTION

Extensive investigations carried out by the applicant have lead to the conclusion that the above described effect is probably due to the fact that the source line voltage $V_S$ of the circuit of FIG. 4 is not constant nor negligible. As a matter of fact, when the cells of other bitlines of the same page are being programmed, the total current $I_{\text{SECTOR}}$ flowing through these bitlines flows also through the source line transistor $\text{MTSRCTOOGND}$ and through the two resistors $R_{SL1}$ and $R_{SL2}$. Thus, the voltage on the $V_S$ node is not negligible and the cell MC31 is incorrectly verified as having reached the desired programmed state.

When the other cells have been programmed, the current $I_{\text{SECTOR}}$ nullifies, the voltage $V_S$ becomes negligible and it is then observed that the threshold voltage of the cell MC31 is no longer correctly comprised in the distribution corresponding to the state 10. This could explain why it appears that the threshold voltage of cells that first reach the desired program distribution becomes smaller while other cells of the same page are programmed.

The applicants have found a method for overcoming and providing a reliable approach to this problem. According to the invention, when the threshold voltage of a cell is verified to have reached the desired distribution, the cell is read using a test read voltage smaller than or equal to the program voltage. In this situation the voltage $V_S$ on the source node is negligible, and the programmed state of the cell may be correctly verified.

An architecture of a page buffer particularly suitable for implementing the method of the invention is also provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts a page buffer of a four-level FLASH memory according to the prior art.

FIG. 2 illustrates the Gray code of a two-bit datum stored in a four level memory cell according to the prior art.

FIG. 3 shows the read margins of a memory cell storing a two-bit datum according to the Gray code according to the prior art.

FIG. 4 is a simplified view of a page of a FLASH memory device according to the prior art.

FIG. 5 illustrates the apparent shift of the programmed threshold voltage of a cell of a four level FLASH memory according to the prior art.

FIGS. 6 to 11 show method steps for programming and verifying the least significant bit of a two-bit datum to be stored in the memory cell according to a first embodiment of the invention.

FIGS. 12 to 19 show method steps for programming and verifying the most significant bit of a two-bit datum to be stored in the memory cell according to the first embodiment of the invention.

FIGS. 20 to 25 show method steps for programming and verifying the least significant bit of a two-bit datum to be stored in the memory cell according to a second embodiment of the invention.

FIGS. 26 to 32 show method steps for programming and verifying the most significant bit of a two-bit datum to be stored in the memory cell according to the second embodiment of the invention.
FIGS. 33 to 38 show method steps for programming and verifying the least significant bit of a two-bit datum to be stored in the memory cell according to a preferred embodiment of the invention.

FIGS. 39 to 45 show method steps for programming and verifying the most significant bit of a two-bit datum to be stored in the memory cell according to the preferred embodiment of the invention.

FIG. 46 depicts the page buffer disclosed in European Patent Application No. 05106972.2.

FIG. 47 depicts a page buffer for implementing the method steps according to the first and second embodiments of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a four-level memory device, each cell is associated with at least a pair of latches a MSB LATCH and a LSB LATCH of the page buffer for storing the bits of the two-bit datum to be written in the cell; and for inhibiting program operations on an already programmed cell. Three alternate embodiments of the method of the invention will now be described.

First Embodiment

The least significant bit of a two-bit datum to be stored in a cell is loaded into the respective latch LSB LATCH of the page buffer. According to a common practice, but not necessarily, it is first stored in the latch dedicated for the most significant bit MSB LATCH, and then it is transferred to the latch LSB LATCH as schematically illustrated in FIG. 6.

Program pulses are applied to the cell (in parallel to all other cells to be programmed) for increasing its threshold voltage up to surpass the first program voltage VVFY1 (FIG. 7). After each program pulse, it is verified whether the cell has been correctly programmed or not. In the former case, a 1 is stored in the LSB LATCH (FIG. 8) for inhibiting application of further program pulses to the cell.

According to the method, the programmed cell is read using a test read voltage for verifying if effectively the threshold of the programmed cell has reached the desired value by ascertaining that the design read voltage margin has not become reduced because of the above discussed effect on the programming verification of a significant voltage present on the source node VS.

Accordingly, the least significant bit still stored in the MSB LATCH is transferred into the LSB LATCH (FIG. 9), and the cells are read using a first test read voltage VVFY1-Δ smaller than or equal to the program voltage VVFY1 (FIG. 10).

If a cell read confirm to be correctly programmed, a 1 is loaded in the respective LSB LATCH for inhibiting further program pulses from being applied to the cell (FIG. 11). A 0 in the LSB LATCH means that the corresponding cell has not yet been correctly programmed, and further program pulses need to be applied to it up to make its threshold surpass the program voltage VVFY1.

Then the most significant bit (MSB) is loaded in the MSB LATCH. The least significant bit (LSB) stored in the cell is read from the cell using the read voltage Vread0 (FIG. 12) and is transferred to an auxiliary latch THIRD LATCH (FIG. 13).

The cell is or is not programmed depending on the most significant bit and the least significant bit respectively stored in MSB LATCH and in the LSB LATCH. The program voltage VVFY2 or VVFY3 that is used depends on the bits of the two-bit datum to be stored in the cell (FIG. 14). Once the desired threshold voltage has been attained, a 1 is loaded in both latches MSB LATCH and LSB LATCH (FIG. 15).

The auxiliary latch THIRD LATCH stores the least significant bit that was to be stored in the cell, and its content is copied into the latch dedicated to the least significant bit LSB LATCH (FIG. 16).

The most significant bit to be programmed in the cell is established by reading the cell with a second read voltage Vread1 (FIG. 17), and the read MSB is copied into the dedicated latch MSB LATCH. Therefore, the latches LSB LATCH and MSB LATCH now store the pair of bits that should have been stored into the memory cell.

Correctness of the programming is tested by reading the cell with a second VVFY2-Δ or a third test read voltage VVFY3-Δ smaller than or equal to the respective program voltage VVFY2 or VVFY3 (FIG. 18).

If the cell, read with the respective test read voltage, results be programmed, a 1 is loaded in the latches LSB LATCH and MSB LATCH for inhibiting further program pulses from being applied to the cell (FIG. 19). Should a 0 be stored in the LSB LATCH and/or in the MSB LATCH, it means that the cell has not yet been correctly programmed. Further program pulses are applied to it up to achieve a threshold beyond the respective program voltage: VVFY2 or VVFY3.

In brief, according to this first embodiment, the method comprises two procedures for correctly programming the least significant bit and the most significant bit of a two-bit datum, respectively.

The procedure for programming the least significant bit (LSB) comprises the following steps:

1. The LSB is programmed in the cell (FIGS. 6 to 8);
2. The LSB value is recovered from the MSB LATCH where it is still stored (FIG. 9);
3. The LSB programming is tested by reading the cell with a first test read voltage equal to the program voltage decreased by a certain quantity VVFY1-Δ (FIG. 10); and
4. If the test fails, further program pulses are applied in parallel also to the failed cell as far as making its threshold surpass the first program voltage VVFY1 (FIG. 11).

The procedure for programming the most significant bit (MSB) comprises the following steps:

1. Retrieving the value of the programmed LSB by reading the cell using a first read voltage Vread0 (FIG. 12);
B2. Storing in an auxiliary latch the bit read in the previous step (FIG. 13);

B3. Applying program pulses to the cell up to make its threshold surpass a respective program voltage $V_{P2}$ or $V_{P3}$ depending on the LSB and the MSB (FIGS. 14 and 15);

B4. Copying in the LSB LATCH the bit stored in the auxiliary latch (FIG. 16);

B5. Retrieving the value of the programmed MSB by reading the cell with a second read voltage $V_{READ2}$ and loading the read bit into the dedicated latch MSB LATCH (FIG. 17);

B6. Testing the reliability of the programming by reading the cell with a second $V_{P2}$- or a third test read voltage $V_{P3}$ smaller than or equal to the respective second or third program voltage $V_{P2}$ or $V_{P3}$ (FIG. 18); and

B7. If the test at the previous step fails, programming pulses are supplied in parallel to the failed cell up to surpass the respective program voltage (FIG. 19).

Second Embodiment

In the second embodiment, the procedure for programming the least significant bit LSB comprises substantially the same steps A1 to A4 of the first embodiment. The method steps illustrated in FIGS. 20 to 25 correspond to that illustrated in FIGS. 6 to 11, with the sole difference that the auxiliary latch THIRD LATCH plays the role of the latch MSB LATCH.

The procedure for programming the most significant bit is slightly different from that of the first embodiment because the auxiliary latch THIRD LATCH is used for storing the most significant bit and not the least significant bit.

The most significant bit is first written into the auxiliary latch THIRD LATCH and then it is transferred to the corresponding latch LSB LATCH (FIG. 26), then the step B1 is carried out. The step B3 is executed through the operations illustrated in FIGS. 27 and 28 that correspond to FIGS. 14 and 15. Then the following steps are carried out:

B4. Copying in the MSB LATCH the bit stored in the auxiliary latch (FIG. 29); and

B5. Retrieving the least significant bit by reading the cell with a first read voltage $V_{READ0}$ and a third read voltage $V_{READ2}$ and loading the read bit into the LSBC LATCH (FIG. 30).

In the second embodiment the least significant bit is read at step B5.

The steps B6 and B7 are carried out as in the first embodiment, as illustrated in FIGS. 31 and 32, respectively, which correspond to FIGS. 18 and 19.

Both embodiments require an auxiliary latch THIRD LATCH used for storing the least significant bit in the first embodiment, or the most significant bit in the second embodiment. The other bit not stored into the auxiliary latch is read using an appropriate read voltage.

Third Embodiment

In this embodiment no auxiliary latch is required because both the least significant bit and the most significant bit are read using appropriate read voltages. As shown in FIGS. 33 to 38, the steps A1 to A4 of the procedure for programming the least significant bit are exactly the same as in the first embodiment.

As far as the procedure for programming the most significant bit is concerned, the step B1 is the same as in the first embodiment as illustrated in FIG. 39. The step B2 is not carried out because there is no auxiliary latch, and the step B3 is identical as in the first embodiment as illustrated in FIGS. 40 and 41.

The least and the most significant bit are retrieved by executing the steps B5 of the first embodiment as illustrated in FIG. 42, and the step B5 of the second embodiment as illustrated in FIG. 43. The steps B6 and B7 are carried out as in the first embodiment as illustrated in FIGS. 44 and 45, respectively.

The third embodiment may be implemented by the page buffer circuit disclosed in European Patent Application No 05106972.2, which is assigned to the current assignee of the present invention. This embodiment is schematically depicted in FIG. 46. The meaning of each label is made clear in the above referenced application.

A novel page buffer suitable for implementing the first and second embodiments is depicted in FIG. 47, in which the same elements in common with FIG. 46 are identified by the same labels. This novel page buffer includes the additional latch THIRD LATCH and a switch M23 controlled by the signal TRANSFER for transferring the bit stored in the THIRD LATCH to the LSB LATCH and vice versa.

Another difference between the novel page buffer of the invention and the page buffer disclosed in the cited prior European patent application is that the latch MSB LATCH is not directly connected to the switches M7 and M8 controlled by the signal DATA LOAD N and DATA LOAD. This is due to the fact that, when the DATA LOAD signal is asserted, a bit must be loaded into the auxiliary latch THIRD LATCH and not in the latch MSB LATCH, before being transferred to the latch LSB LATCH.

That which is claimed:

1. A method of programming a four-level FLASH memory device including an array of singularly addressable preliminarily erased memory cells, each capable of storing a two-bit datum, by programming first the least significant bit in all the cells and then the most significant bit in all the cells, comprising the following steps:

   a) applying program pulses in parallel to all the cells in which a least significant bit of a certain logic value (0) must be stored, increasing stepwise the threshold voltage up to make it surpass a first program voltage (VVFI1), and leaving in the erased state the other cells in which a least significant bit of opposite logic value (1) must be stored,

   b) applying program pulses in parallel to all the cells in which a least significant bit of said certain logic value (0) must be stored, increasing stepwise the threshold voltage up to make it surpass a second program voltage
(VVFY2) to all the cells in which the least significant bit equals said certain logic value (0), or a third program voltage (VVFY3) to all the cells in which the least significant bit differs from said certain logic value, and leaving all the cells, in which a most significant bit of opposite logic value (1) must be stored, as they are at the end of step a), characterized in that the method comprises performing after step a) the following additional steps before step b):

a1) testing the least significant bit programming by reading the array cells using a first test read voltage (VVFY1) smaller than or equal to said first program voltage (VVFY1);

a2) if any cell fails the test, applying program pulses in parallel to all the failed cells increasing stepwise their threshold voltage up to make it surpass said first program voltage (VVFY1).

2. The method of claim 1, further comprising performing after step b) the following additional steps:

b1) testing the most significant bit programming carried out in step b) by reading the array cells either using a second test read voltage (VVFY2) or a third test read voltage (VVFY3), respectively, said second and third test read voltages (VVFY2, VVFY3) being smaller than or equal to said second program voltage (VVFY2) or third program voltage (VVFY3), respectively;

b2) if any cell fails the test, applying program pulses in parallel to all the failed cells increasing stepwise their threshold voltage up to make it surpass the second program voltage (VVFY2) or the third program voltage (VVFY3), respectively.

3. The method of claim 1, wherein said FLASH memory comprises a page buffer including at least a first latch (LSB LATCH) and a second latch (MSB LATCH) for each memory cell for temporarily storing the least significant bit and the most significant bit, respectively, wherein said step a) is carried out through the following operations:

aa) loading in both said latches the least significant bit of a two-bit string to be written in the memory cell,

ab) applying program pulses in parallel to all the cells in which the bit stored in the respective first latch (LSB LATCH) surpasses said first program voltage (VVFY1), loading the inverse of said certain logic value (1) in the respective first latch (LSB LATCH);

wherein step a1) is carried out through the following operations:

a1a) copying the value stored in each of said second latches (MSB LATCH) in the corresponding first latch (LSB LATCH);

a1b) testing the least significant bit programming by reading the array cells the respective first latch (LSB LATCH) of which stores a bit of said certain logic value (0) using said first test read voltage (VVFY1), and loading the inverse of said certain logic value (1) in the first latch (LSB LATCH) if said test is verified;

wherein step a2) is carried out through the following operations:

a2a) applying program pulses in parallel to all the cells the first latch (LSB LATCH) of which stores said certain logic value (0),

a2b) as soon as the threshold voltage of each cell surpasses said first program voltage (VVFY1), loading the inverse of said certain logic value (1) in the respective first latch (LSB LATCH).

4. The method of claim 2, wherein said page buffer comprises an auxiliary latch (THIRD LATCH) for each memory cell, said step b) being carried out through the following operations:

ba) reading the array cells using a first read voltage (Vread0) for discriminating programmed cells from erased cells and loading in said first latch (LSB LATCH) a bit of said certain logic value (0) or its inverse (1), respectively,

bb) loading in said second latches (MSB LATCH) the respective most significant bits,

bc) copying in said auxiliary latches (THIRD LATCH) the bits stored in the respective first latch (LSB LATCH),

bd) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which stores said certain logic value (0), by increasing stepwise the threshold voltage of all the cells the first latch (LSB LATCH) of which stores said certain logic value (0) up to make it surpass the second program voltage (VVFY2) or of all the cells the first latch (LSB LATCH) of which stores the inverse logic value (1) up to make it surpass the third program voltage (VVFY3),

be) as soon as the threshold voltage of each cell surpasses said second (VVFY2) or third program voltage (VVFY3), respectively, loading said inverse logic value (1) in the respective first latch (LSB LATCH) and in the second latch (MSB LATCH), wherein step b1) is carried out through the following operations:

b1a) copying the value stored in said auxiliary latches (THIRD LATCH) in the corresponding first latches (LSB LATCH),

b1b) reading the array cells using a second read voltage (Vread1) smaller than said second program voltage (VVFY2) and loading in said second latches (MSB LATCH) the most significant bits that have been read,

b1c) testing the most significant bit programming by reading the array cells the second latch (MSB LATCH) of which stores said certain logic value (0) using a second test read voltage (VVFY2) if the least significant latch (LSB LATCH) stores said certain logic value (0) or a third test read voltage (VVFY3) if the least significant latch (LSB LATCH) stores said inverse logic value (1), smaller than or equal to said second program voltage (VVFY2) or third program voltage
(VVFY3), respectively, and loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH) if the read most significant bit equals said certain logic value (0);

wherein step b2) is carried out through the following operations:

b2a) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which and the first latch (LSB LATCH) of which store said inverse logic value (1),

b2b) as soon as the threshold voltage of each cell surpasses said program voltage (VVFY2) or said program voltage (VVFY3), loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH).

5. The method of claim 2, wherein said page buffer comprises an auxiliary latch (THIRD LATCH) for each memory cell, the auxiliary latch (THIRD LATCH) being used for carrying out steps a) to a2b) instead of the second latch (MSB LATCH), said step b) being carried out through the following operations:

ba) loading in said auxiliary latch (THIRD LATCH) the most significant bit of the two-bit string to be stored therein,

bb) copying in second latch (MSB LATCH) the bit stored in said auxiliary latch (THIRD LATCH),

bc) reading the array cells using a first read voltage (Vread0) for discriminating programmed cells from erased cells and loading in said first latch (LSB LATCH) a bit of said certain logic value (0) or its inverse (1), respectively,

bd) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which stores said certain logic value (0), by increasing stepwise the threshold voltage of all the cells the first latch (LSB LATCH) of which stores said certain logic value (0) up to make it surpass the second program voltage (VVFY2) or of all the cells the first latch (LSB LATCH) of which stores the inverse logic value (1) up to make it surpass the third program voltage (VVFY3),

be) as soon as the threshold voltage of each cell surpasses said second (VVFY2) or third program voltage (VVFY3), respectively, loading said inverse logic value (1) in the respective first latch (LSB LATCH) and in the second latch (MSB LATCH);

wherein step b1) is carried out through the following operations:

b1a) copying the value stored in said auxiliary latches (THIRD LATCH) in the corresponding second latches (MSB LATCH),

b1b) reading the array cells using a first read voltage (Vread0) or a third read voltage (Vread2), that are smaller than said first program voltage (VVFY1) or said third program voltage (VVFY3), respectively, and loading in said first latches (LSB LATCH) the least significant bits that have been read,

b1c) testing the most significant bit programming by reading the array cells the second latch (MSB LATCH) of which stores said certain logic value (0) using a second test read voltage (VVFY2-A ) if the least significant latch (LSB LATCH) stores said certain logic value (0) or a third test read voltage (VVFY3-A ) if the least significant latch (LSB LATCH) stores said inverse logic value (1), smaller than or equal to said second program voltage (VVFY2) or third program voltage (VVFY3), respectively, and loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH) if the read most significant bit equals said certain logic value (0);

wherein step b2) is carried out through the following operations:

b2a) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which and the first latch (LSB LATCH) of which store said inverse logic value (1),

b2b) as soon as the threshold voltage of each cell surpasses said second program voltage (VVFY2) or third program voltage (VVFY3), loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH).

6. The method of claim 2, wherein said step b) is carried out through the following operations:

ba) loading in said second latches (MSB LATCH) the respective most significant bits,

bb) reading the array cells using a first read voltage (Vread0) for discriminating programmed cells from erased cells and loading in said first latch (LSB LATCH) a bit of said certain logic value (0) or its inverse (1), respectively,

bc) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which stores said certain logic value (0), by increasing stepwise the threshold voltage of all the cells the first latch (LSB LATCH) of which stores said certain logic value (0) up to make it surpass the second program voltage (VVFY2) or of all the cells the first latch (LSB LATCH) of which stores the inverse logic value (1) up to make it surpass the third program voltage (VVFY3),

bd) as soon as the threshold voltage of each cell surpasses said second (VVFY2) or third program voltage (VVFY3), respectively, loading said inverse logic value (1) in the respective first latch (LSB LATCH) and in the second latch (MSB LATCH),

wherein step b1) is carried out through the following operations:

b1a) reading the array cells using a second read voltage (Vread1) smaller than said second program voltage (VVFY2) and loading in said second latches (MSB LATCH) the most significant bits that have been read,

b1b) reading the array cells using a first read voltage (Vread0) or a third read voltage (Vread2), that are smaller than said first program voltage (VVFY1) or said third program voltage (VVFY3), respectively, and loading in said first latches (LSB LATCH) the least significant bits that have been read,

b1c) testing the most significant bit programming by reading the array cells the second latch (MSB LATCH)
of which stores said certain logic value (0) using a second test read voltage (VVFY2) if the least significant latch (LSB LATCH) stores said certain logic value (0) or a third test read voltage (VVFY3) if the least significant latch (LSB LATCH) stores said inverse logic value (1), smaller than or equal to said second program voltage (VVFY2) or third program voltage (VVFY3), respectively, and loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH) if the read most significant bit equals said certain logic value (0);

wherein step b2) is carried out through the following operations:

b2a) applying program pulses in parallel to all the cells the second latch (MSB LATCH) of which and the first latch (LSB LATCH) of which store said inverse logic value (1).

b2b) as soon as the threshold voltage of each cell surpasses said second program voltage (VVFY2) or third program voltage (VVFY3), loading said inverse logic value (1) in the second latch (MSB LATCH) and in the first latch (LSB LATCH).

7. A page buffer for a four-level FLASH memory device including an array of singularly addressable preliminarily erased memory cells, each capable of storing a two-bit datum, said FLASH memory comprising a page buffer including at least a first latch (LSB LATCH) and a second latch (MSB LATCH) for each memory cell for temporarily storing the least significant bit and the most significant bit, respectively, characterized in that it comprises

an auxiliary latch (THIRD LATCH) for each memory cell;

controlled circuit means for coupling the auxiliary latch (THIRD LATCH) to said first latch (LSB LATCH) or to said second latch (MSB LATCH) for implementing the method of claim 4, respectively.

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