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## (54) Semiconductor Device with an Inclined Source/Drain and Associated Methods

(57) A semiconductor device includes a semiconductor substrate having a channel region therein, a gate structure above the channel region, and source and drain regions on opposite sides of the gate structure. A respective contact is on each of the source and drain regions. At least one of the source and drain regions has an inclined upper contact surface with the respective contact. The inclined upper contact surface has at least a 50% greater area than would a corresponding flat contact surface.

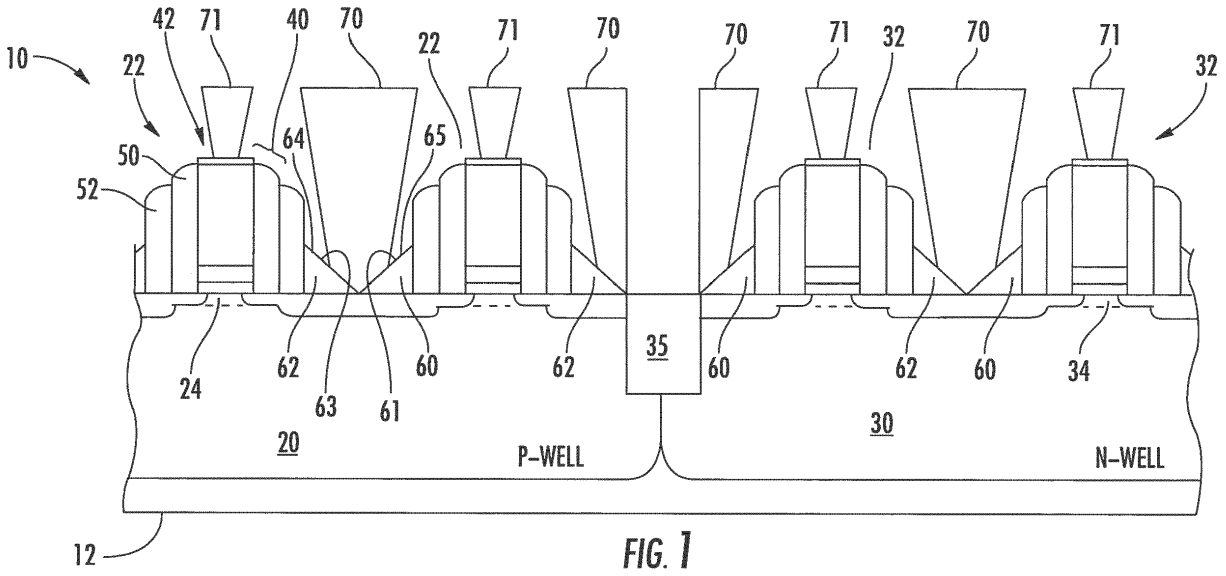


FIG. 1

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## Description

### Field

**[0001]** Some embodiments relate to the field of semiconductor devices, and in particular but not exclusively, to a semiconductor device with a reduced contact resistance between a contact and a source/drain region, and related methods.

### Background

**[0002]** Semiconductor devices, such as semiconductor integrated circuits (ICs), include numerous semiconductor device structures. Example semiconductor device structures are interconnected complementary metal oxide semiconductor (CMOS) transistors, which include both P-channel and N-channel MOS transistors. Interconnectivity between various device structures is accomplished by metalized contacts forming interlayer connections between the device structures.

**[0003]** Semiconductor device structures, including CMOS transistors, are being designed to have smaller and smaller feature sizes (e.g., gate structures). Based on this trend, as the gate pitch becomes smaller, the contacts that connect the source/drain regions of the transistor with metalized contacts also become smaller. As the contacts decrease in size, there is an increase in contact resistance. Contact resistance, which is decided by contact area and sheet resistivity, is becoming a limiting factor in further device performance improvement.

**[0004]** One approach to reduce contact resistance is disclosed in U.S. Patent No. 8,101,489. A semiconductor substrate having doped regions is provided. A pre-amorphous implantation process and neutral (or non-neutral) species implantation process is performed over the doped regions. Subsequently, a silicide is formed in the doped regions. By conducting a pre-amorphous implantation combined with a neutral species implantation, the contact resistance between the silicide contact area and source/drain substrate interface is reduced.

**[0005]** Another approach to reduce contact resistance is disclosed in U.S. Patent No. 8,134,208. A semiconductor device includes a semiconductor device structure and a contact, and the contact is electrically and physically coupled to the semiconductor device structure at both a surface portion and a sidewall portion of the semiconductor device structure.

**[0006]** While the above approaches may be effective in reducing contact resistance, further improvements may be desired.

### Summary

**[0007]** In view of the foregoing background, it is therefore an aim of some embodiments to provide a semiconductor device with a reduced contact resistance that is readily manufactured.

**[0008]** This and other objects, features, and advantages may be provided by a semiconductor device comprising a semiconductor substrate having a channel region therein, a gate structure above the channel region, and source and drain regions on opposite sides of the gate structure. A respective contact may be on each of the source and drain regions. At least one of the source and drain regions may have an inclined upper contact surface with the respective contact.

**[0009]** The inclined upper contact surface may advantageously be formed using an additional etching step on the source and drain regions, with the etching step being self-limiting on tight pitch devices. This may advantageously provide better control of the upper contact surface for device optimization. Source and drain implantation may be performed after the additional etching step.

**[0010]** The inclined upper contact surface may be inclined downwardly away from the gate structure, and the incline may be at an angle in a range of 30-45 degrees. The inclined upper contact surface may have at least a 50% greater area than would a corresponding flat contact surface.

**[0011]** The source and drain regions may comprise respective raised source and drain regions. The raised source and drain regions may be provided by an epitaxial layer formed on the semiconductor substrate. The gate structure may comprise a gate stack and at least one sidewall spacer on opposite sides of the gate stack.

**[0012]** Another aspect is directed to a method for making a semiconductor device as described above. The method may comprise providing a semiconductor substrate having a channel region therein, forming a gate structure above the channel region, forming source and drain regions on opposite sides of the gate structure, and forming a respective contact on each of the source and drain regions. At least one of the source and drain regions has an inclined upper contact surface with the respective contact.

**[0013]** A semiconductor device may comprise a semiconductor substrate having a channel region therein; a gate structure above the channel region; source and drain regions on opposite sides of said gate structure; and a respective contact on each of said source and drain regions; at least one of said source and drain regions having an inclined upper contact surface with said respective contact.

**[0014]** The inclined upper contact surface may be inclined downwardly away from said gate structure.

**[0015]** The inclined upper contact surface may be inclined at an angle in a range of 30-45 degrees.

**[0016]** The source and drain regions may comprise respective raised source and drain regions.

**[0017]** The inclined upper contact surface may have at least a 50% greater area than would a corresponding flat contact surface.

**[0018]** The gate structure may comprise a gate stack and at least one sidewall spacer on opposite sides of said gate stack.

**[0019]** The gate stack may comprise a dielectric layer adjacent the channel region and a conductive layer on said dielectric layer.

**[0020]** A complementary metal oxide semiconductor (CMOS) semiconductor device may comprise a semiconductor substrate having a p-channel region and an n-channel region therein; a respective gate structure above the p-channel region and the n-channel region; respective source and drain regions on opposite sides of each gate structure; and a respective contact on each of said source and drain regions; at least one of said source and drain regions having an inclined upper contact surface with said respective contact, with the inclined upper contact surface being inclined downwardly away from said gate structure at an angle in a range of 30-45 degrees.

**[0021]** The respective source and drain regions may comprise respective raised source and drain regions.

**[0022]** The inclined upper contact surface may have at least a 50% greater area than would a corresponding flat contact surface.

**[0023]** Each gate structure may comprise a gate stack and at least one sidewall spacer on opposite sides of said gate stack.

**[0024]** Each gate stack may comprise a dielectric layer adjacent the channel region and a conductive layer on said dielectric layer.

## Brief Description of the Drawings

**[0025]** FIG. 1 is a cross-sectional view of semiconductor devices with inclined contacts.

**[0026]** FIGS. 2-4 are cross-sectional views of a portion of the semiconductor devices shown FIG. 1 illustrating the process steps for making the same.

**[0027]** FIG. 5 is an image of a cross-sectional view of semiconductor devices with inclined contacts and having an 80 nm gate pitch.

**[0028]** FIG. 6 is an image of a cross-sectional view of a semiconductor device with inclined contacts and having a 200 nm gate pitch.

**[0029]** FIG. 7 is a flowchart illustrating a method for making a semiconductor device.

## Detailed Description of Embodiments

**[0030]** The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set fourth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout, and prime notation is used to indicate similar elements in alternative embodiments.

**[0031]** Referring initially to FIG. 1, the illustrated semiconductor device **10** is a complementary metal oxide semiconductor (CMOS) semiconductor device. The semiconductor device **10** includes a semiconductor substrate **12** with at least one p-well **20** and at least one n-well **30** separated by a shallow trench isolation (STI) region **35**. The p-well **20** is for n-channel transistors **22,** whereas the n-well **30** is for p-channel transistors **32.**

**[0032]** Each p-channel transistor **32** includes a p-channel region **34** in the semiconductor substrate **12.** Similarly, each n-channel transistor **22** includes an n-channel region **24** in the semiconductor substrate **12**. Respective gate structures **40** are above the p-channel regions **34** and the n-channel regions **24.** Each gate structure **40** includes a gate stack **42** and at least one pair of sidewall spacers **50, 52** on opposite sides of the gate stack.

**[0033]** Source and drain regions **60, 62** are on opposite sides of each gate structure **40.** As will be discussed in greater detail below, the source and drain regions **60, 62** may be raised. A respective contact **70** is on each of the source and drain regions **60, 62.** To reduce contact resistance between the contacts **70** and the source and drain regions **60, 62,** the upper contact surfaces **61, 63** of the source/drain regions are inclined with the respective contacts **70**.

**[0034]** The inclined upper contact surface **61, 63** as illustrated is inclined downwardly away from the gate structure **40.** The illustrated inclined upper contact surface **61, 63** is inclined at an angle in a range of 30-45 degrees. The inclined upper contact surface **61, 63** may have at least a 50% greater area than would a corresponding flat contact surface. The larger the area the lower the contact resistance.

**[0035]** As will be discussed in greater detail below, the inclined upper contact surface may advantageously be performed using an additional etching step on the source and drain regions, with the etching step being self-limiting on tight pitch devices. This advantageously provides better control of the upper contact surface for device optimization. Source and drain implantation may be performed after the additional etching step.

**[0036]** Referring now to FIGS. 2-4, the process steps for forming the CMOS semiconductor device **10** as described above will now be discussed. The shallow trench isolation region **35** is formed in the semiconductor substrate **12,** and the p-well **20** and n-well **30** are respectively doped, as show in FIG. 2.

**[0037]** Gate structures **40** are formed on the semiconductor substrate **12**. Each gate structure **40** includes a gate stack **42** and at least one sidewall spacer **50** on opposite sides of the gate stack. The gate stack **42** includes an oxide layer **43,** a gate dielectric **44** on the oxide layer, a conductive layer **46** on the dielectric layer, and a silicide layer **48** on the conductive layer. The first pair of sidewall spacers **50** protects the gate structure **40.** The first pair of spacers **50** may be silicon nitride, for example. A hard mask spacer **51** is also formed on the silicide layer **48.**

**[0038]** After formation of the first pair of sidewall spacers **50,** lightly doped drain/source extension regions **80** are formed on each side of the channel regions **24, 34.** As would be readily appreciated by those skilled in the art, the lightly doped extension regions typically reduce the electric field near the channel regions **24, 34** and thus the hot-carrier reliability of the transistors is improved. The extension regions **80** reduce the electric field by effectively dropping a portion of the source/drain voltages across the extension regions.

**[0039]** After formation of the extension regions **80,** a second pair of sidewall spacers **52** is formed, as illustrated in FIG. 3. As will be readily appreciated by those skilled in the art, the second pair of sidewall spacers **52** allows a heavier implantation dose to be performed while reducing the punchthrough effect between the source and drain regions **60, 62.**

**[0040]** The source and drain regions **60, 62** as illustrated in FIG. 1 are raised. Still referring to FIG. 3, this is accomplished by growing an epitaxial layer **90** on the substrate **12**. Alternatively, the source and drain regions **60, 62** may be formed without being raised.

**[0041]** Referring now to FIG. 4, the hard mask spacers **51** above the gates stacks **42** are removed. The epitaxial layer **90** is etched to form the inclined upper contact surfaces **61, 63** for corresponding source and drain regions **60, 62.** As readily appreciated by those skilled in the art, the etching may be a wet etch or a dry etch. An example etch uses hydrochloric acid (HCL), for example. The epitaxial layer **90** has a <100> plane but after the etching it becomes a <111> plane, as also readily appreciated by those skilled in the art.

**[0042]** Due to the pitch of the gate stacks **42,** the etching step may be self-limiting on tight pitch devices. This advantageously provides better control of the upper contact surfaces **61, 63** for device optimization. As noted above, the inclined upper contact surfaces **61, 63** may be inclined downwardly away from the gate stack **42,** and the incline may be at an angle in a range of 30-45 degrees. The inclined upper contact surfaces **61, 63** may have at least a 50% greater area than would corresponding flat contact surfaces.

**[0043]** After the etching step, source and drain implantations are performed. This may be followed by a rapid thermal anneal to activate the dopants from the implantation. Next, silicide **64, 65** may be formed on the inclined upper contact surfaces **61, 63,** as illustrated in FIG. 4. Contacts **70** may then be formed on the source and drain regions **60, 62** and contacts **71** may be formed on the gate stacks **42,** as initially illustrated in FIG. 1.

**[0044]** As noted above, the source and drain regions **60, 62** may be formed without being raised. As best illustrated in FIG. 5, the source and drain regions **60', 62'** are formed in the semiconductor substrate **12'**. The upper contact surfaces **61', 63'** are still inclined downwardly away from the gate stack **42'.** The pitch between the gate stacks **42'** is 80 nm, which in turn is self-limiting to the etching step.

**[0045]** As the pitch between the gate stacks **42'** increases, the pitch is not as self-limiting. As illustrated in FIG. 6, the gate pitch is 200 nm. The upper contact surfaces **61', 63'** are still inclined downwardly away from the gate stack **42'** but there is now a flat surface **66'** between the inclined upper contact surfaces.

**[0046]** Referring now to the flowchart **100** illustrated in FIG. 7, a method for making a semiconductor device **10** as described above will now be discussed. From the start (Block **102),** the method comprises providing a semiconductor substrate **12** having a channel region **24** therein at Block **104**, and forming a gate structure **40** above the channel region at Block **106.** At Block **108,** source and drain regions **60, 62** are formed on opposite sides of the gate structure **40**. A respective contact **70** is formed on each of the source and drain regions **60, 62** at Block **110.** At least one of the source and drain regions **60, 62** has an inclined upper contact surface 61, **63** with the respective contact **70** as provided at Block **112.** The method ends at Block **114.**

**[0047]** Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

## Claims

**1.** A semiconductor device comprising:

a semiconductor substrate having a channel region therein;
a gate structure above the channel region;
source and drain regions on opposite sides of said gate structure; and
a respective contact on each of said source and drain regions;
at least one of said source and drain regions having an inclined upper contact surface with said respective contact.

**2.** The semiconductor device according to Claim 1 wherein the inclined upper contact surface is inclined downwardly away from said gate structure.

**3.** The semiconductor device according to Claim 1 or 2 wherein the inclined upper contact surface is inclined at an angle in a range of 30-45 degrees.

**4.** The semiconductor device according to any preceding claim wherein said source and drain regions comprise respective raised source and drain regions.

**5.** The semiconductor device according to any preced-

ing claim wherein the inclined upper contact surface has at least a 50% greater area than would a corresponding flat contact surface.

**6.** The semiconductor device according to any preceding claim wherein said gate structure comprises a gate stack and at least one sidewall spacer on opposite sides of said gate stack.

**7.** The semiconductor device according to Claim 6 wherein said gate stack comprises a dielectric layer adjacent the channel region and a conductive layer on said dielectric layer.

**8.** A device as claimed in any preceding claim, wherein the semiconductor device is a complementary metal oxide semiconductor CMOS semiconductor device, said channel region comprises a p-channel region and an n-channel region with a respective gate structure above the p-channel region and the n-channel region, and respective source and drain regions provided on opposite sides of each gate structure.

**9.** A method for making a semiconductor device comprising:

providing a semiconductor substrate having a channel region therein;
forming a gate structure above the channel region;
forming source and drain regions on opposite sides of the gate structure; and
forming a respective contact on each of the source and drain regions;
with at least one of the source and drain regions having an inclined upper contact surface with the respective contact.

**10.** The method according to Claim 9 wherein forming the inclined upper contact surface comprises an etching step.

**11.** The method according to Claim 9 or 10 wherein the inclined upper contact surface is inclined downwardly away from the gate structure.

**12.** The method according to any of Claims 9 to 11 wherein the inclined upper contact surface is inclined at an angle in a range of 30-45 degrees.

**13.** The method according to any of Claims 9 to 12 wherein the source and drain regions comprise respective raised source and drain regions.

**14.** The method according to Claim 13 wherein forming the respective raised source and drain regions comprising forming an epitaxial layer on the semiconductor substrate.

**15.** The method according to any of Claims 9 to 14 wherein the inclined upper contact surface has at least a 50% greater area than would a corresponding flat contact surface.

**16.** The method according to any of Claims 9 to 15 wherein the gate structure comprises a gate stack and at least one sidewall spacer on opposite sides of the gate stack.

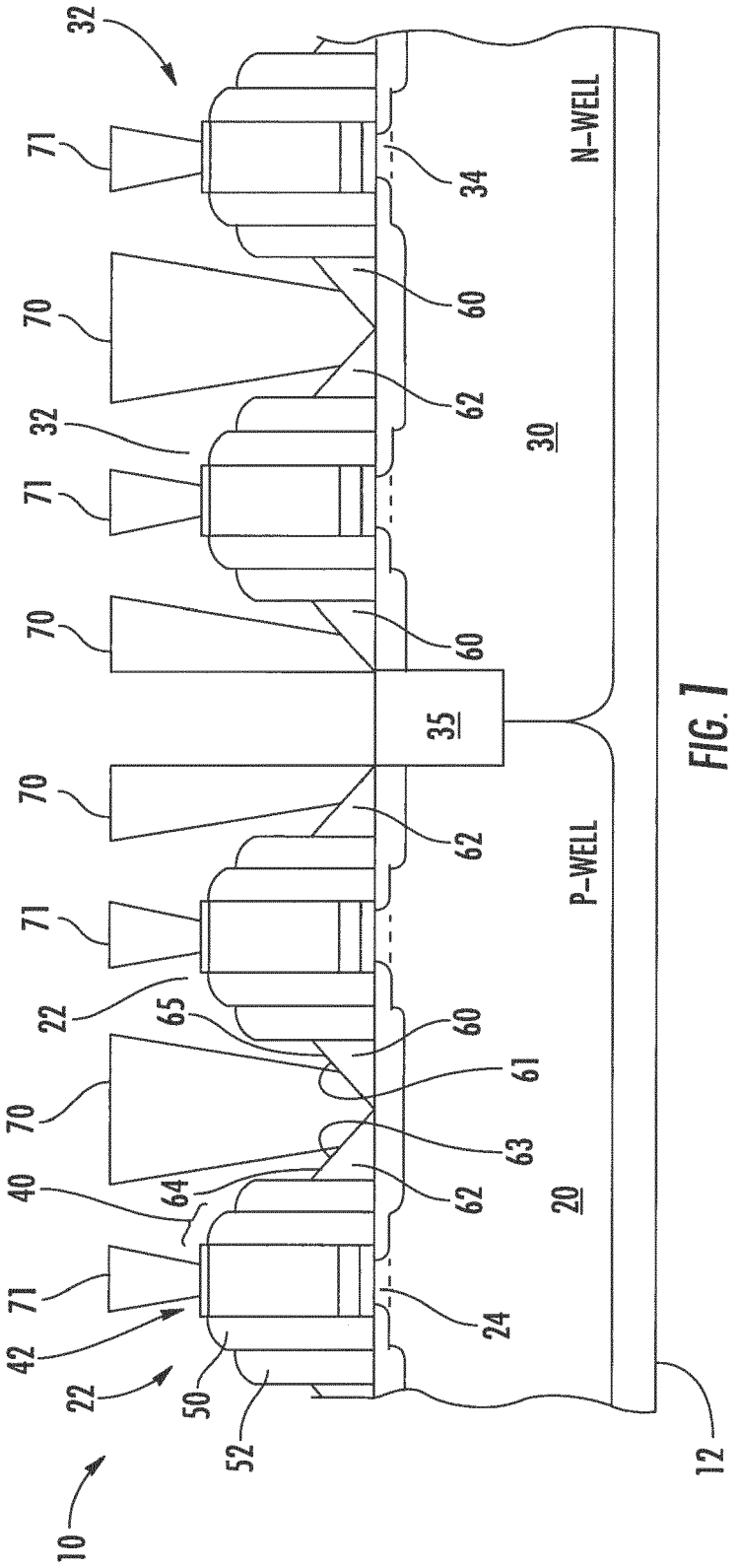
32
71
34
N-WELL
70
60
62
30
32
71
70
60
35
70
62
71
22
65
60
61
70
63
40
64
62
20
71
24
42
22
50
52
10
12
P-WELL

FIG. 1

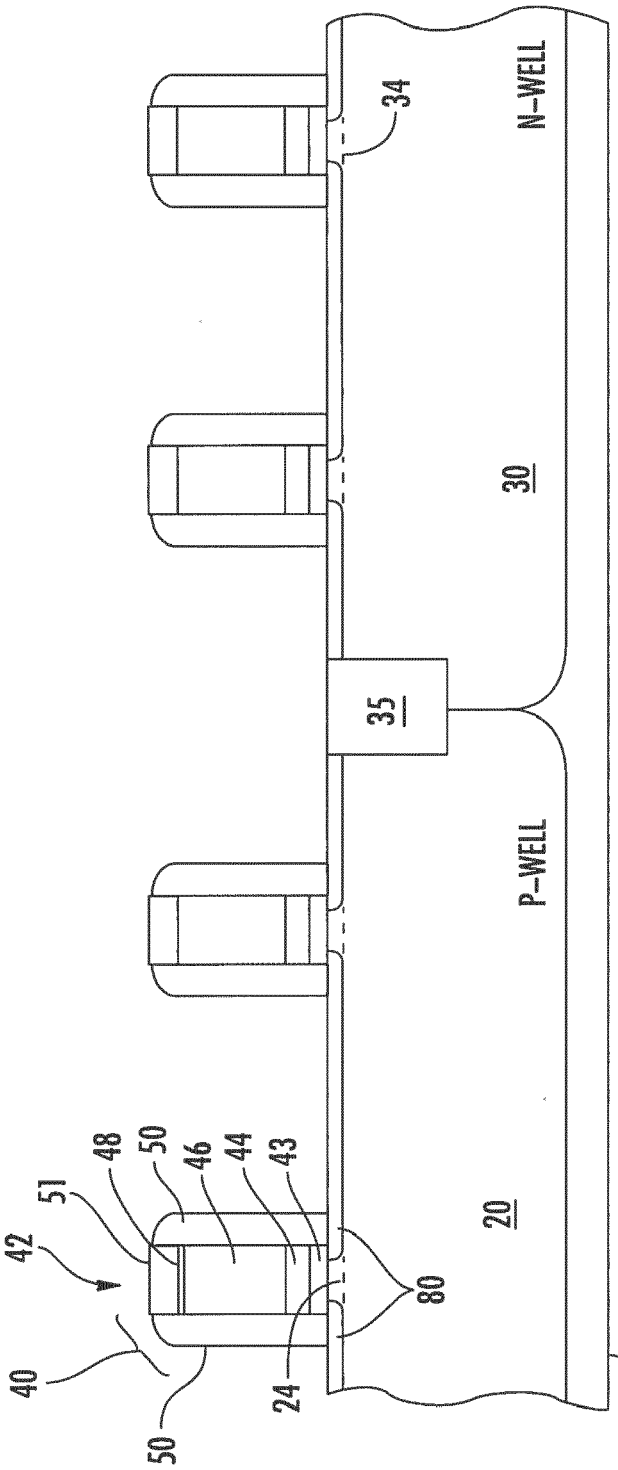


FIG. 2

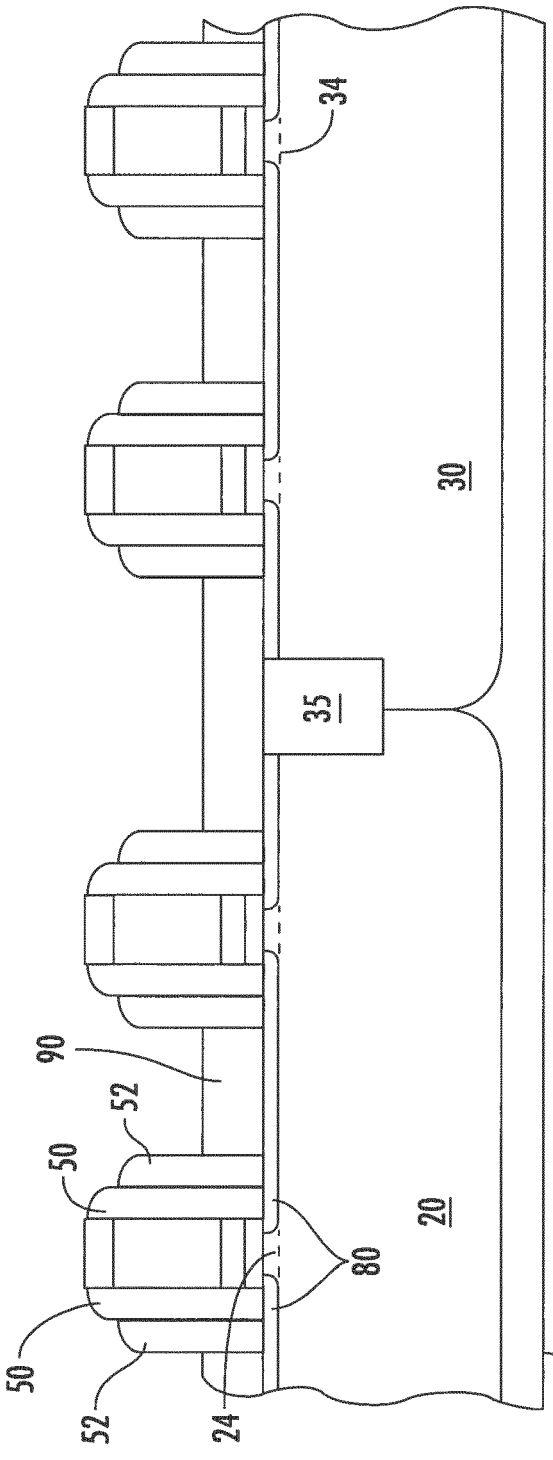


FIG. 3

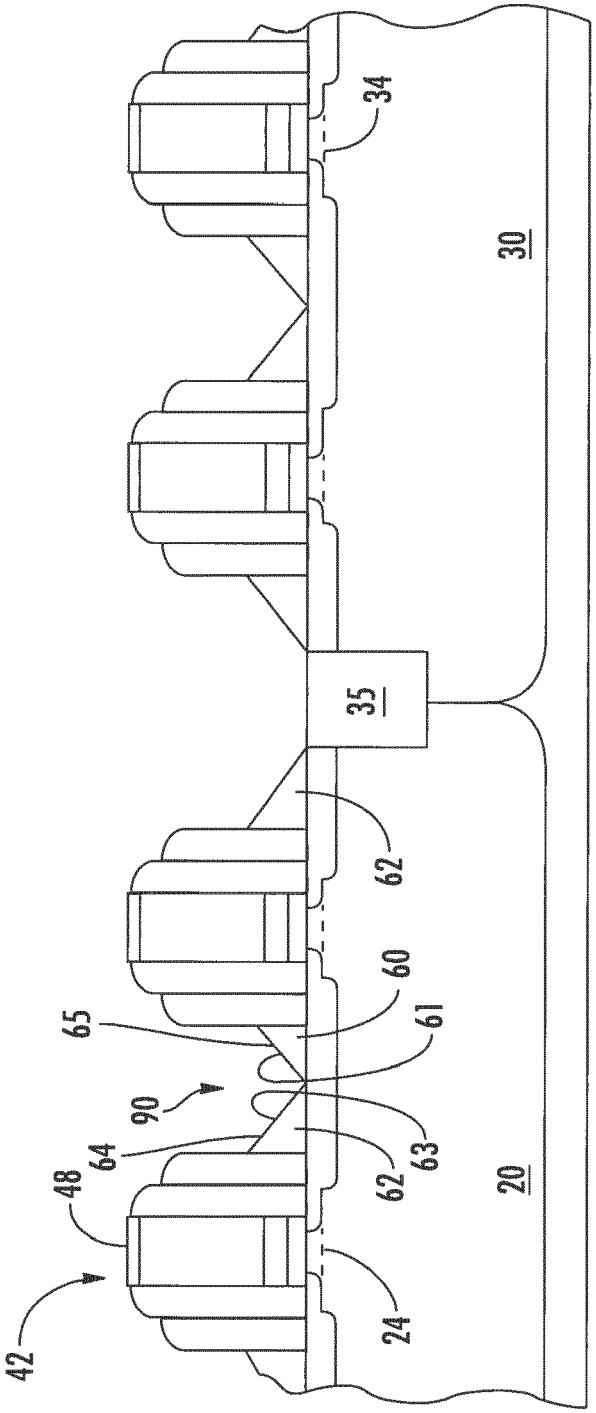


FIG. 4

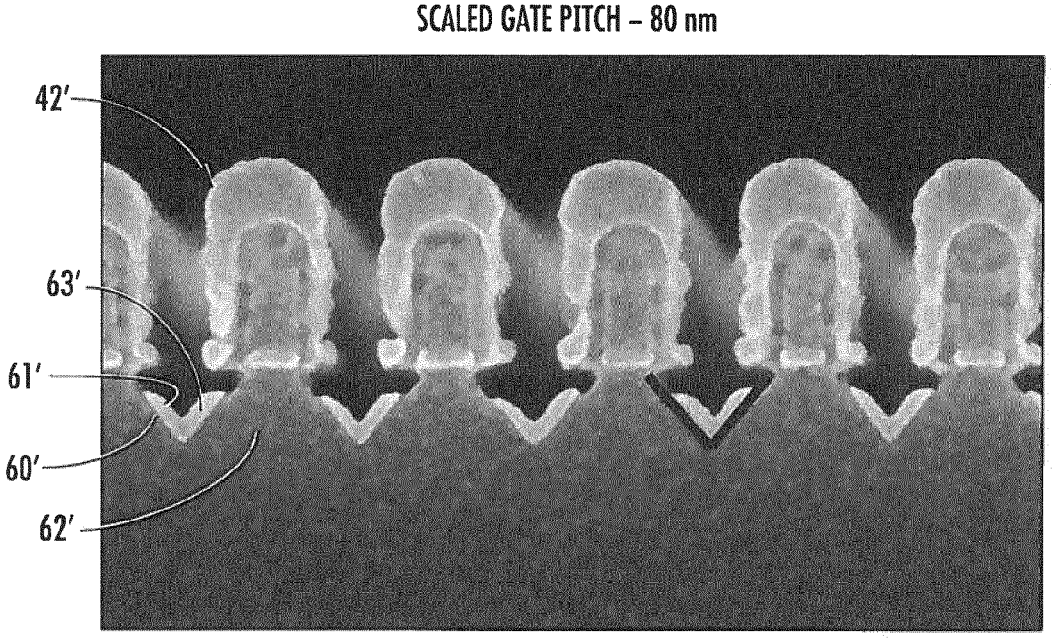
SCALED GATE PITCH – 80 nm
42′
63′
61′
60′
62′

FIG. 5

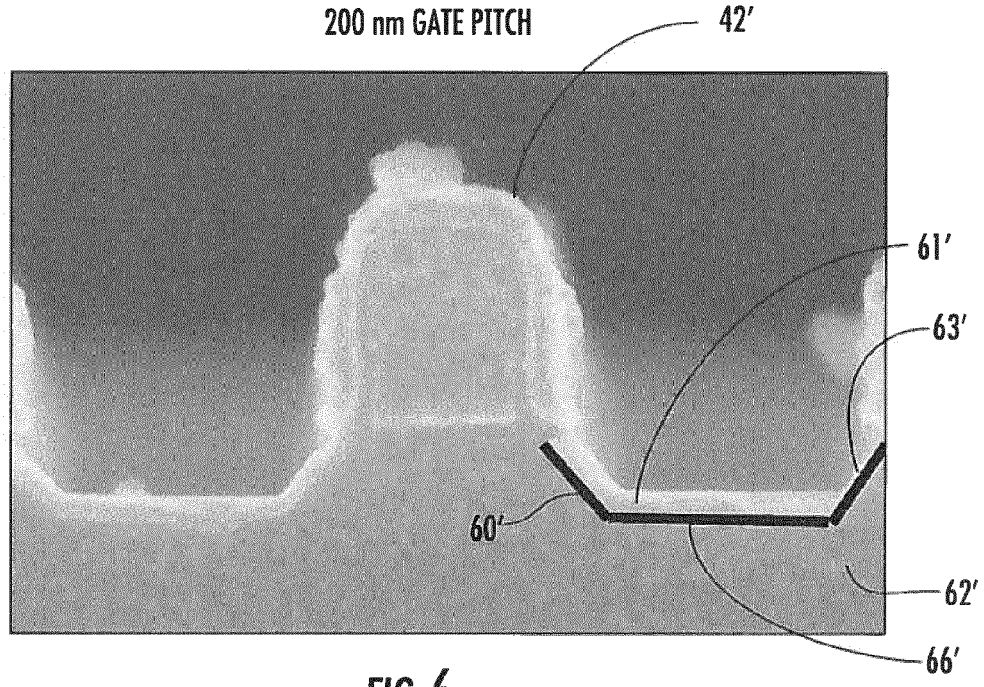
200 nm GATE PITCH
42′
61′
63′
60′
62′
66′

FIG. 6

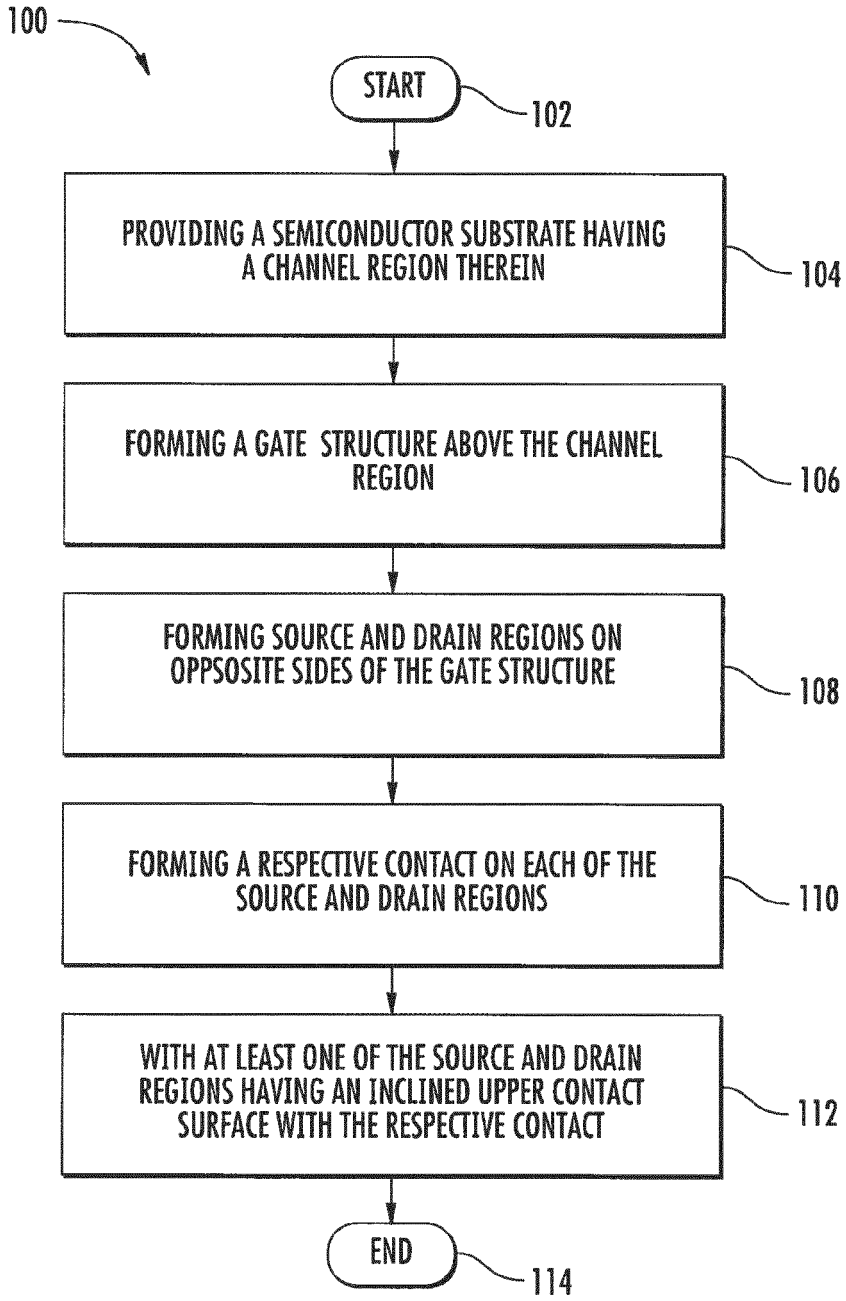
100
START
102
PROVIDING A SEMICONDUCTOR SUBSTRATE HAVING A CHANNEL REGION THEREIN
104
FORMING A GATE STRUCTURE ABOVE THE CHANNEL REGION
106
FORMING SOURCE AND DRAIN REGIONS ON OPPSOSITE SIDES OF THE GATE STRUCTURE
108
FORMING A RESPECTIVE CONTACT ON EACH OF THE SOURCE AND DRAIN REGIONS
110
WITH AT LEAST ONE OF THE SOURCE AND DRAIN REGIONS HAVING AN INCLINED UPPER CONTACT SURFACE WITH THE RESPECTIVE CONTACT
112
END
114

FIG. 7

## REFERENCES CITED IN THE DESCRIPTION

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### Patent documents cited in the description


- US 8101489 B **[0004]**
- US 8134208 B **[0005]**