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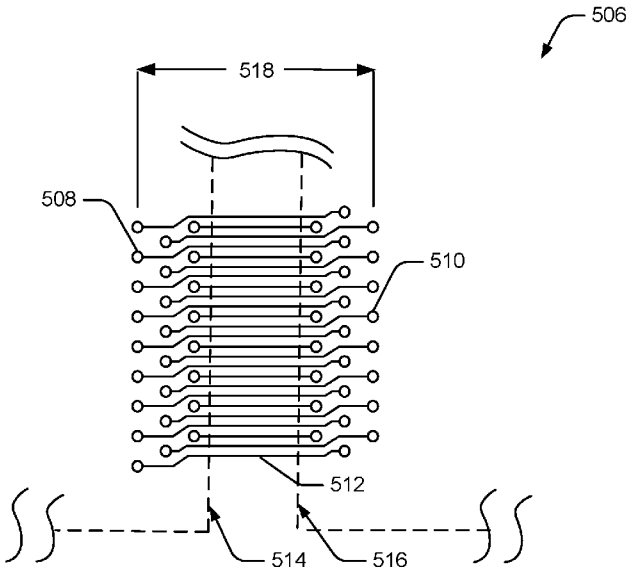

Fig. 5

(57) Abstract: This document describes apparatuses and techniques for integrated DRAM with low-voltage swing I/O. In some aspects, a dynamic random access memory (DRAM) die and application processor (AP) die are mounted to a system-in-package (SiP) die carrier that includes one or more redistribution layers. The DRAM die and AP die are located adjacent to each other on the die-carrier such that respective memory inputs/outputs of each die are proximate the other inputs/outputs.

WO 2018/136124 A1

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INTEGRATED DRAM WITH LOW-VOLTAGE SWING I/O

BACKGROUND

[0001] Computing devices include various types of memory to which data is written or from which data is read. Many types of conventional memory, however, are optimized for density efficiency (*e.g.*, raw capacity) instead of size, cost, power, or other aspects of memory performance. As such, these types of conventional memory are typically ill suited for use in mobile devices where cost, size, and power are often critical design or manufacturing constraints.

SUMMARY

[0002] This disclosure describes apparatuses and techniques for implementing integrated dynamic random access memory (DRAM) with low-voltage swing input/output (I/O). A dynamic random access memory (DRAM) die and application processor (AP) die are implemented on a system-in-package (SiP) die carrier that includes one or more redistribution layers. In some cases, the DRAM die and AP die are placed adjacent to each other on the die carrier such that respective data inputs/outputs of each die are proximate. This summary is provided to introduce simplified concepts concerning integrated DRAM

with low-voltage swing I/O, which is further described below in the Detailed Description. This summary is not intended to identify essential features of the claimed subject matter, nor is it intended for use in determining the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Embodiments of DRAM with low-voltage swing I/O are described with reference to the following drawings. The same numbers are used throughout the drawings to reference like features and components:

Fig. 1 illustrates an example environment that includes a computing device having an application processor and DRAM memory.

Fig. 2 illustrates an example configuration of the application processor and DRAM memory shown in Fig. 1.

Fig. 3 illustrates an example floor-plan of a DRAM die implemented in accordance with one or more aspects.

Fig. 4 illustrates an example floor-plan of an AP die implemented in accordance with one or more aspects.

Fig. 5 illustrates details of a die carrier to which an example DRAM die and an example AP are mounted.

Fig. 6 illustrates example performance diagrams of a system-in-package implemented in accordance with aspects described herein.

Fig. 7 illustrates an example method for mounting a DRAM die and an application processor die to a die carrier in accordance with one or more aspects.

Fig. 8 illustrates example, alternate configurations of a DRAM die and an AP die in a system-in-package.

Fig. 9 illustrates an example method for integrating a DRAM die with an application processor die.

Fig. 10 illustrates an example System-in-Package in which a DRAM die and AP die may be integrated in accordance with one or more aspects.

DETAILED DESCRIPTION

Overview

[0004] For most devices, particularly for high performance devices, inserting memory inline, such as cache memory, with an application processor (AP) can improve latency and bandwidth. When in the mobile space these and similar solutions, such as conventional techniques using embedded dynamic random access memory (eDRAM) or high bandwidth memory (HBM) with through silicon via (TSV) packaging technologies, are too costly.

[0005] The aspects described in this disclosure provide memory with latency, bandwidth, or cost improvements, which may be suitable for deployment in mobile spaces. In some cases, a dynamic random access memory (DRAM) die and application processor (AP) die are mounted onto a die carrier having redistribution layers (RDLs). The die

carrier, used in assembly of a System-in-Package (SiP) component, includes pads that position the DRAM die and AP die adjacent to each other such that respective data inputs/outputs of each die are proximate.

[0006] These are but a few examples of ways in which DRAM with low-voltage swing I/O can be implemented, which are described herein. The following discussion first describes an operating environment, followed by techniques that may be employed in this environment, and ends with example systems.

Operating Environment

[0007] Fig. 1 illustrates an example environment 100 that includes a computing device having an application processor and DRAM memory. Computing device 102 is illustrated with various non-limiting example devices, a smartphone 102-1, a tablet 102-2, and a laptop computer 102-3, though other devices may also be used, such as home automation and control systems, smart-watches, entertainment systems, wearable computers, Internet-of-Things devices, audio systems, other home appliances, security systems, netbooks, automobiles, smart-appliances, and e-readers. Note that the computing device 102 can be wearable, non-wearable but mobile, or relatively immobile (*e.g.*, desktops and appliances).

[0008] The computing device 102 includes one or more application processor die 104 and computer-readable media 106 (CRM 106), which includes memory media and storage media. Applications and/or an operating system (not shown) embodied as computer-readable instructions on computer-readable media 106 can be executed by

application processor die 104 to enable various functionalities of the computing device 102.

[0009] In some aspects, the application processor 104 and CRM 106, as dynamic random access memory (DRAM) 110 or other memory types, are implemented as an integrated system-in-package (SiP) component. For example, the application processor and DRAM can be dies, or chips, mounted onto a die carrier, of a system-in-package (SiP) component, via microbumps. In the case of the SiP, the application processor die and DRAM die may be connected via a redistribution layers (RDL) of the die carrier, where the RDL serves to connect integrated circuitry of the application processor die and the DRAM die.

[0010] The computing device 102 may also include one or more network interfaces 114 for communicating data over wired, wireless, or optical networks and a display 116. The network interface 114 may communicate data over a local-area-network (LAN), a wireless local-area-network (WLAN), a personal-area-network (PAN), a wide-area-network (WAN), an intranet, the Internet, a peer-to-peer network, point-to-point network, a mesh network, and the like. The display 116 can be integral with the computing device 102 or associated with it, such as with a gaming system or set-top box.

[0011] Fig. 2 illustrates an example configuration 200 of the application processor and DRAM memory shown in Fig. 1. In this example, an application processor (AP) die 202 and CRM, here shown as DRAM die 204, are implemented as a system-in-package (SiP) 206. Although shown as separate, the network interface 114 and/or a controller for

the display 116 may also be implemented in whole or part within the system-in-package 206 and/or with components thereof (*e.g.*, a baseband processor or graphics processor).

[0012] With respect to integrating the application processor die 202 and the DRAM die 204, any suitable type of data bus or configuration may be implemented. In some aspects, a high data rate of third generation low-power double data rate random access memory (LPDDR3) having wide data width supporting a Wide I/O2 (WIO2) compatible data bus are combined in a custom DRAM die (*e.g.*, 1Gb) to provide up to 68GB/s peak bandwidth. This design can be constructed for use where the DRAM die 204 and AP die 202 are placed side-by-side in the system-in-package (SiP) 206 and interface with Low Voltage Swing IOs (LVSIO). This may be effective to allow the full optimization of the 68GB/s while controlling power consumption of the DRAM die 204 and the AP die 202. Streamlined data flow, organized as compact bit slices, may also reduce parasitic capacitance and dynamic power. In some cases, this aids in attaining in 20mW/GBps in a seam-less read mode. The dual chip design may, in some instances, be implemented with an Integrated Fan-Out Wafer Level Packaging (InFOWLP) technique which results in low capacitance interconnections and efficiently distributed power delivery networks.

[0013] In some aspects, the DRAM die 204 is designed and constructed on a 30nm process technology for fabricating semiconductor wafers, with key features of the Wide I/O2 and LPDDR3 specifications or protocols. The process technology used to fabricate semiconductor wafers of the DRAM die 204 may not match the process technology used to fabricate wafers semiconductor wafers of a corresponding AP die of the SiP.

[0014] The DRAM die 204 may include four independent channels, each supporting an 8 byte wide data I/O and each with a separate power distribution network (PDN). The die floorplan can be bit-slice oriented to minimize on-chip Global data read/write (GDRW) routes to improve performance and power. In some cases, edge micro-bumps are used to facilitate low Re-Distribution Layer (RDL) interconnect capacitance between the DRAM die and AP. These micro-bumps may be implemented using any suitable process, size, and/or pitch, such as at pitches less than ~50 μm and/or with heights of ~40 μm. Alternately or additionally, the microbumps can be implemented with Copper (Cu) Pillar micro-bump or thermal compression with non-conductive paste (TCNCP) technologies. In order to reduce the interface power with high IO count, the Low Voltage Swing Input/Output (*e.g.*, JESD8-38) can be utilized to implement an interface between the DRAM die 204 and the AP die 202, or other components. The output stage logic power voltage (VCCQ) potential of the DRAM die 204 or AP die 202 can be driven by an applied load of approximately 0.3 volts and/or implemented without termination (*e.g.*, resistors or capacitors) between the two dies (or chips). In at least some aspects, the dies and die carrier are implemented directly, without interposer layers and/or through silicon vias, thereby enabling low capacitance interconnects and higher operating frequencies and/or transfer bandwidth.

[0015] The DRAM die 204 may also include other features, such as WIO2-like Data Bus Inversion (DBIac) to reduce simultaneous switching output (SSO) noise, Boundary Scan (BSCAN) for contactless testing of micro bumps, on-die reference voltage generation with trimming as proposed on LPDDR4X or other advanced memory specifications,

reduction of key row timings to address system random access cycle, and several test options to validate the high performance targets. Table 1 compares the features of this custom design with existing DRAM protocols.

Items	LPDDR3	WIO2	Custom
MAX DR	2133 Mbps	800 Mbps	2133 Mbps
DBI	no	yes - Dblac	yes - Dblac
BSCAN	no	yes - Dblac	yes - Dblac
VCCQ (V)	1.2	1.2	0.3
CHANNEL I/O	X32	X64	X64
CIO (pF)	5	1.4	0.3
CHANNELS	1	4	4
CHIP I/Os	32	256	256
2.5/3D PKG	no	yes (TSV)	yes (ubump)
VREF FOR CA	ext	ext	int
VRDEF FOR DQ	ext	ext	int
INPUT VSW	1.2	1.2	0.3
ON CHIP TEST	no	yes	yes

Table 1

[0016] In some cases, the 64Mb banks in each channel are configured as 4k row depth by 2kB page. Each access can provide an 8b pre-fetch for 64IOs controlled by column addresses (CA) <7:0.

[0017] Power dissipation of the DRAM 204 die can be optimized by using a ~300mV LVSIO design and/or minimizing the high speed data path routes. Alternately or additionally, the latter can be met by using a compressed, bit-slice data-path that keeps the GDRW lines to a minimum. By way of example, a 30nm design has a measured Idd4r2 in seam-less read mode of ~275mA/channel, or 20mW/GBps, approximately half the energy

per bit of standard LPDDR4 designs. An LVSIO design reduce power and improve performance, but the ~300mV un-terminated IO interface can results in a small data eye. To help reduce SSO eye degradation that may arise on a 512b wide IO bank, a DBIac algorithm can be implemented. This DBIac algorithm may be implemented similar to those of the WIO2 specification due to the un-terminated IO's or interface. In some cases, tight pitch of the bit lanes helps reduce wiring capacitance associated with calculating the DBIac. The 8-bit pre-fetch, however, may increase the calculation time for the DBIac algorithm when compared to WIO2. Mask Write command may also be added to provide an enablement of the dual function direct data bus (DMI) pin.

[0018] Fig. 3 illustrates an example floor-plan 300 of a DRAM die implemented in accordance with one or more aspects. The floor-plan 300 of a DRAM die, such as the DRAM die 204 of Fig. 2, supports a 4 channel chip architecture, each channel having one 64 Mb bank (302-1 through 302-4). The floor-plan 300 supports two identical dual-channels, 304-1 and 304-2, each fully autonomous for typical DRAM operations. The DRAM die may include Low Voltage Swing Input/Output (LVSIO) circuitry, inclusive of drivers, sense-amps, or the like, as necessary to access data and communicate data via inputs/outputs of the die. As illustrated, the floor-plan 300 illustrates fields of Low Voltage Swing Inputs/Outputs (LVSIOs) 306-1 and 306-2, respectively shared by dual-channels 304-1 and 304-2.

[0019] In this particular example, the respective shared fields of LVSIOs 306-1 and 306-2 are each are comprised of 128 microbumps, such as microbump 308, which support data I/O that is 16 bytes wide for each dual channel (effective to support a 32 byte wide

data bus from the DRAM die). The fields of LVSIOs 306-1 and 306-2 (*e.g.*, microbumps) are located at, or proximate, the edge 310 of the DRAM die. Locating the fields of LVSIOs 306-1 and 306-2 at, or proximate, the edge 310 of the DRAM die affords incorporating the DRAM die into a system-in-package (SiP) design that incorporates a data bus having reduced parasitics and that is optimized for performance.

[0020] The floor-plan 300 also includes fields of test pads and power microbumps, shared, respectively, by the dual channels 304-1 and 304-2. In this particular example, the respective shared fields 312-1 and 312-2 of test pads and power microbumps are each comprised of a plurality of test pads, such as test pad 314, and a plurality of power microbumps, such as microbump 316.

[0021] The plurality of test pads is configured to support testing of the DRAM die (via a semiconductor wafer probe pin or other electrical contact). The test pads may be metallic and enable test coverage for this design (*e.g.*, a custom memory design) in order to cover the standard array defects, validate the high speed paths and verify the feature set, while keeping test costs in line with other memory products. Test flow can be very critical for this design, and these test pads may enable the use of standard test fixtures, algorithms, or other procedures. Test data, collected via the test pads, may be used to aid in selection of a die during assembly

[0022] Wafer probing capabilities and DRAM circuitry functionality may influence arrangement of the test pads. For example, each 8-byte channel of the DRAM may have one byte of test data lines (DQs) with a single command/address (CA) pad set shared between a dual-channel. This may allow the testing to be completed on a single channel,

dual channel, or full chip with a reasonable probe count, thereby reducing quantity and/or location of test pads. The single test byte within a channel may be the broadcast to all 8 bytes in write mode and each of the 8 bytes can be serially sent compressed to the test byte in a read. As another example, DRAM circuitry supporting Built in Self-Test (BIST), data compression, and the like can reduce quantity of test pads required. Testing can exercise the entire data flow at maximum product speed at wafer test with the standard product circuit path, with the possible exception of the IB and Off Chip Driver (OCD).

[0023] The plurality of power microbumps is configured to connect to a power source supplying power to internal voltage generators and charge pumps of the DRAM die to support the array operations. Placement of the power microbumps, relative to the DRAM die floorplan, can be impact tFAW and tRDD timings and also help manage the high current demand regions by reducing, for example, current-resistance (IR) drops to key generators, pumps, and circuits.

[0024] Continuing with Fig. 3, the floor-plan 300 also includes other fields including microbumps that aid in mounting the DRAM die to a die carrier, such as fields of outrigger microbumps 316-1 through 316-6. Each outrigger microbump, such as outrigger microbump 318, may or may not provide additional electrical connectivity.

[0025] Fig. 4 illustrates an example floor-plan 400 of an AP die implemented in accordance with one or more aspects. The AP die may include Low Voltage Swing Input/Output (LVSIO) circuitry, inclusive of drivers, logic, or the like, as necessary to process data and communicate data via data inputs/outputs of the AP die. In the example, the floor-plan 400 of the AP die, such as the AP die 202 of Fig. 2, supports a processing

core 402 having Low Voltage Swing Input/Output (LVSIO) circuitry. The floor-plan 400 supports transmission and receipt of data via a field of LVSIOs 404 comprised of microbumps, such as microbump 406. In this particular example, the field of LVSIOs 404 includes 256 microbumps in order to support a data bus that is 256 bits wide. As illustrated by the floor-plan 400, the field of LVSIOs 404 (*e.g.*, microbumps) is located at, or proximate, the edge 408 of the AP die. Locating the field of LVSIOs 404 at, or proximate, the edge 408 of the AP die affords incorporating the AP die into a system-in-package (SiP) design that incorporates a data bus having reduced parasitics and that is optimized for performance.

[0026] The AP die also includes interconnect fields 408-1 through 408-3. The fields of interconnects 410-1 through 410-3 include microbumps, such as microbump 412, and serve as additional connections, either electrical or mechanical in nature, to the die carrier.

[0027] Fig. 5 illustrates details of a die carrier to which an example DRAM die and an example application processor die are mounted. In some aspects, the redistribution layer includes a plurality of un-terminated traces that provide a data bus between LVSIOs of the DRAM die and the application processor (AP) die.

[0028] Configuration 500 illustrates a side view exemplifying DRAM die 204 and AP die 202 of Fig. 2 mounted to an example die carrier 502. Die carrier 502 may be fabricated using fan-out wafer-level packaging (INFO-WLP) techniques that utilize multiple layers of RDL. At least one layer of the multiple layers of RDL, RDL 504, provides electrical connectivity, serving as an un-terminated interface, between the DRAM

die 204 and the AP die 202. DRAM die 204 and AP die 202 may be mounted to the die carrier, via pads defined by the RDL 504, using microbumps.

[0029] View 506 illustrates a magnified top view of a portion of RDL 504 (not to scale). The view includes a first plurality of pads, such as pad 508, a second plurality of pads, such as pad 510, and a plurality of traces, such as trace 512. Also illustrated is a boundary 514 for placement of DRAM die 204 (corresponding to edge 310 of Fig. 3) oriented adjacent to a boundary 516 for placement of AP die 202 (corresponding to edge 408 of Fig. 4). The first plurality of pads serves to mount, via microbumps, one or more fields of data I/O's of the DRAM die 204 (*e.g*, the fields of data I/O's 306-1 and fields 306-2 of Fig. 3) to the die carrier 502. The second plurality of pads serves to mount, via microbumps, a field of data I/O's of the AP die 202 (*e.g.*, the field of LVSIOs 404) to the die carrier 502.

[0030] The plurality of traces serves as an un-terminated interface that transmits signals between LVSIOs of DRAM die 204 and LVSIOs of AP die 202. In general, architectures of the DRAM die 204, AP die 202, and die carrier 502 are combined such that a distance 518 between RDL pads is optimized, resulting in trace lengths that are less than 530μm and effective to reduce parasitics of and optimize performance of a system in package (SiP) utilizing the combined architectures. Also, note that any individual I/O would, by definition, be contained within a proximity of less than 530μm from the die edge in order to avoid physical interferences of die when being mounted to the RDL pads. For example, it may be possible to have an individual I/O of a DRAM die be 100 μm from the

edge of the DRAM die, while a corresponding, individual I/O of an AP die is 400 μm from the edge of the AP die, but still maintain a trace length that is less than 530μm.

[0031] Die carrier 502 may also include additional, dedicated redistribution layers. For example, die carrier 502 may include an RDL (not illustrated) that is dedicated as a power plane, serving as a power connection for microbumps, such as microbump 318 of Fig. 3 or microbump 412 of Fig. 4. An additional redistribution layer dedicated as a power plane may support a more robust power distribution network (PDN) by strategic placement of power interconnects, effective to reduce the current-resistance (IR) drops to key generators, pumps, and circuits. Independent banks of a DRAM die, such as banks 302-1 through 302-4 as illustrated in the floor-plan 300 of the DRAM die illustrated in Fig.3, may each be powered by an associated power distribution network (PDN).

[0032] Fig. 6 illustrates example performance diagrams of a system-in-package implemented in accordance with aspects described herein. Performance diagram 600 may, for example, represent performance of the die carrier to which an example DRAM die and an example application processor die are mounted of Fig. 5. Fig. 6 illustrates a voltage vs. frequency shmoo plot measured from test pads in 4-channel operation mode. As shown at data point 602, stable operation is enabled at Vdd2=1.14V and 1067 MHz clock frequency. Additionally, the measurement results show tCK vs Vdd2 operating window and tRCD and tRP of 9.4 ns and 9.1 ns, respectively, at Vdd2=1.2V.

[0033] Performance diagram 604 compares a first continuous read data-eye 606 at 2133Mbps without DBIac enabled and a second continuous read data-eye 608 at 2133Mbps with DBIac. These silicon data eye waveforms from a continuous, seamless read cycle

highlight a 1.8X improvement (210mv/119mV) in eye height with DBIac enabled.

[0034] Table 2 summarizes the key array timings along with chip standby and active currents for critical operating modes.

1.2V/80C	CHANNEL SILICON (ns)	1.2V/85C	CHANNEL SILICON (mA)
tAA	10.8	Idd02	35.3
tRCD	9.4	Idd2P2	0.053
tRP(pb)	9.1	Idd4r2	275.2
tRAS	24.3	Idd4r2 w/dbi	279.3
tRCD	33.4	Idd4w2	145.1
tWR	6.1	Idd4w2 w/dbi	156.4
tRRD	2.6	Idd52	37.9
tFAW	11.6		

Table 2

[0035] Accordingly, a custom 1.2V 1Gb design may be developed in and/or using 30 nm technology. The design may operate as a thirty-two (32) byte wide IO chip with four (4) independent channels each supporting eight (8) bytes. Such a design has been verified to operate up to 1067MHz clock frequency at Vdd2 = 1.14V. An I/O power per bit of 2.5mW/Gbps can be attained with the optimized bit-slice architecture and LVSIO techniques as described herein. Edge to edge DRAM to AP placement on next level of assembly may also result in 68GBps data rate while using lower-cost packaging infrastructure.

[0036] Fig. 7 illustrates example, alternate configurations of a system-in-package containing a DRAM die and an AP die. Although floor-plan 300 of the DRAM die 204 and floor-plan 400 of the AP die 202 have been described in the context of mounting the DRAM die 204 and the AP die 202 to the die carrier 502, general architecture of the respective die floor-plans (*e.g.*, 300 and 400) lend themselves to additional, alternate configurations. Such configurations may offer, to an end user, an acceptable cost-versus-performance tradeoff when compared to configurations obtained via (TSV) packaging construction techniques.

[0037] In general, a DRAM die (such as DRAM die 204) and an AP die (such as AP die 202) may be fixed to either a coplanar surface or to parallel surfaces in a fashion that still maintains respective LVSIO field locations adjacent to one another. However, as opposed to electrically connecting respective I/O's of the LVSIO fields via an RDL, respective I/Os may be electrically connected via wirebonds or the like. Doing so may, in certain instances, result in a data bus having acceptable parasitic performance characteristics for a particular end use application of the system-in-package (SiP).

[0038] Example configuration 700 illustrates the DRAM die 204 and the AP die 202 fixed to a common planar surface via a common substrate 702 (note, that in contrast to configuration 500 of Fig. 5, DRAM die 204 and AP die 202 are oriented "face up" in configuration 700). The substrate 702 may be, in some instances, fabricated from silicon or a printed circuit board (PCB) containing one or more layers of circuitry. The DRAM die 204 and the AP die 202 may be fixed to the surface using taping or other semiconductor packaging techniques. The fields of LVSIOs (*e.g.*, 306-1, 306-2, and 404) are adjacent to

one another and are connected, in this instance, via wirebonds 704 (note the absence of RDL and microbumps).

[0039] Example configuration 706 illustrates a cross-section of the DRAM die 204 and the AP die 202 fixed to differing planar surfaces which are parallel to one another. In this example configuration, the DRAM die 204 and AP die 202 are stacked on top of a substrate 708, which again may be fabricated from silicon or a PCB containing one or more layers of circuitry. The order of stacking (DRAM die 204 on top of AP die 202, or vice versa) is variable, but "shingling" must occur in order to expose the respective fields of LVSIOs (*e.g.*, 306-1, 306-2, and 404) such that connection via wirebonds, such as wirebonds 710, may occur. Doing so may, in certain instances, result in a data bus having acceptable parasitic performance characteristics for a particular end use application of the system-in-package (SiP).

Example Method

[0040] Fig. 8 illustrates an example method for mounting a DRAM die and an application processor die to a die carrier. This method is shown as sets of blocks that specify operations performed but are not necessarily limited to the order or combinations shown for performing the operations by the respective blocks. For example, operations of different methods may be combined, in any order, to implement alternate methods without departing from the concepts described herein. In portions of the following discussion, the techniques may be described in reference to Figs. 2-5 though reference to which is made

for example only. The techniques are not limited to performance by one entity or multiple entities operating on one device, or those described in these figures.

[0041] At 802, a plurality of dynamic random access memory (DRAM) die are diced from a first semiconductor wafer. Each of the plurality of DRAM die is configured to communicate data via data inputs/outputs located at an edge of the DRAM die. The DRAM die may be the DRAM die 204 of Fig. 2 having a floor-plan corresponding to floor-plan 300 of Fig. 3. Dicing may be accomplished through a dicing process such as laser dicing, sawing, and the like.

[0042] At 804, a plurality of application processor (AP) die are diced from a second semiconductor wafer. Each of the plurality of AP die is configured to transmit and receive data via data inputs/outputs located near an edge of the AP die. The AP die may be the AP die 202 of Fig. 2 having a floor-plan corresponding to floor-plan 400 of Fig. 4. Dicing may be accomplished as noted above.

[0043] At 806, a DRAM die is selected from the plurality of DRAM Die and an AP die is selected from the plurality of AP die. The selection of DRAM die may be based, at least in part, on test data collected via test pads located on the DRAM die. The DRAM die, as well as the AP die, may also be selected based on identifiers associated with a semiconductor inking or marking process.

[0044] At 808, the selected DRAM die and selected AP die are mounted to pads of one or more RDLs of a die carrier fabricated from a silicon substrate. The die may be mounted to the pads via microbumps, comprised of microbumps such as 306, 308, 316, and 318 of Fig. 3 and microbumps 406 and 412 of Fig. 4. Mounting processes may rely

on, for example, thermal compression, reflow, or another semiconductor manufacturing process specific to a microbump material that results in the microbumps adhering to the pads of the one or more RDLs. Additionally, mounting processes may further result in edges of the selected DRAM die and edges of the selected AP die being mounted adjacent to one another, as illustrated in by the boundaries 514 and 516 shown in Fig. 5.

[0045] Fig. 9 illustrates an example method 900 for integrating a DRAM die with an application processor die. This method is shown as sets of blocks that specify operations performed but are not necessarily limited to the order or combinations shown for performing the operations by the respective blocks. For example, operations of different methods may be combined, in any order, to implement alternate methods without departing from the concepts described herein. In portions of the following discussion, the techniques may be described in reference to Figs. 3-5, though reference to which is made for example only. The techniques are not limited to performance by one entity or multiple entities operating on one device, or those described in these figures.

[0046] At 902, a die carrier is fabricated from a silicon substrate. The die carrier is fabricated to have one or more redistribution layers (RDLs), each layer of which includes respective traces. In some instances, the die carrier may be the die carrier 502 of Fig. 5 and the first RDL may be the RDL 504 of Fig. 5, including traces such as trace 512 and pads such as pad 508 and 510. As part of 902, a second RDL that is a power plane may also be fabricated. Furthermore, any RDL of the one or more RDL's may be fanned out.

[0047] At 904, an application processor (AP) die having low-voltage swing input/output (LVSIO) circuitry and having data inputs/outputs located at an edge of the AP

die is fabricated. In some cases, the AP die is the AP die 202 of Fig. 2 and has a floor-plan in accordance with floor-plan 400 Fig. 4.

[0048] At 906, a dynamic random access memory (DRAM) die having other LVSIO circuitry and other data inputs/outputs located at an edge of the DRAM die is fabricated. In some instances, the DRAM die is the DRAM die 204 of Fig. 2 and has a floor-plan in accordance with floor-plan 300 of Fig. 3.

[0049] At 908, the AP die and the DRAM die are mounted to the pads of the one or more RDLs of the die carrier. In some cases, the fields of microbumps may the fields of LVSIOs 404 and fields of interconnects 410-1 through 410-3 of Fig. 4 and the other fields of microbumps may be the fields of LVSIO's 306-1, 306-2, 312-1, 312-2, and 316-1 through 316-6 of Fig. 3. The microbump pads of the one or more RDLs may include, at least in part, pads 508 and 510 of Fig. 5.

Example System-in-Package

[0050] Fig. 10 illustrates various elements of an example system-in-package (SiP) 1000 that can be embodied in any type of client, server, and/or computing device as described with reference to the previous Figs. 1-8. The system-in-package 1000 includes a combination components of integrated circuitry in die or other form, including circuitry that may be integrated as part of a system-on-chip (SoC) die, to form the system-in-package 1000. Interconnects within the system-in-package 1000 may rely on combinations of package assembly technologies, including wirebonding to electrical pads, use of microbumps, and the like.

[0051] The components include communication interfaces 1002 that enables communication of system data 1004 (*e.g.*, received data, data that is being received, data scheduled for broadcast, data packets of the data, etc.). The communication interfaces may be implemented as controllers for any one or more of a serial and/or parallel interface, a wireless interface, any type of network interface, a modem, and as any other type of communication interface. System data 1004 or other system content can include configuration settings of the system, media content stored on the system, and/or information associated with a user of the system. Media content stored on the System-in-Package 1000 can include any type of audio, video, and/or image data. The system-in-package 1000 includes one or more data inputs 1006 via which any type of data, media content, and/or inputs can be received, such as messages, music, television media content, recorded video content, and any other type of audio, video, and/or image data received from any content and/or data source.

[0052] Also included are or more application processors 1008 (*e.g.*, any of microprocessors, controllers, and the like), which process various computer-executable instructions to control the operation of the system-in-package 1000. The system-in-package also includes DRAM 1010, which may be connected to respective ones of the application processors 1008 and/or placed adjacent to the application processors 1008 on a die carrier fabricated from silicon in accordance with methods described herein. Alternatively or in addition, the system-in-package 1000 can be implemented with any one or combination of hardware, firmware, or fixed logic circuitry that is implemented in connection with processing and control circuits, which are generally identified at 1012.

Although not shown, the system-in-package 1000 can include a system bus or data transfer system that couples the various components within the system. A system bus can include any one or combination of different bus structures, such as a memory bus or memory controller, a peripheral bus, a universal serial bus, and/or a processor or local bus that utilizes any of a variety of bus architectures.

[0053] The system-in-package 1000 also includes other components that may computer-readable media 1014, such as one or more memory devices that enable persistent and/or non-transitory data storage (i.e., in contrast to mere signal transmission), examples of which include non-volatile memory (*e.g.*, any one or more of a read-only memory (ROM), flash memory, EPROM, EEPROM, etc.) and the like. The System-in-Package 1000 may also interface with a disk storage device implemented as any type of magnetic or optical storage device, such as a hard disk drive, a recordable and/or rewriteable compact disc (CD), any type of a digital versatile disc (DVD), and the like.

[0054] The computer-readable media 1014 provides data storage mechanisms to store the system data 1004, as well as various system applications 1016 and any other types of information and/or data related to operational aspects of the System-in-Package 1000. For example, an operating system 1018 can be maintained as software or firmware with the computer-readable media 1014 and executed on the application processors 1008.

Conclusion

[0055] Although techniques and apparatuses for integrated DRAM with low-voltage swing I/O have been described in language specific to features and/or methods, it is to be

understood that the subject of the appended claims is not necessarily limited to the specific features or methods described. Rather, the specific features and methods are disclosed as example ways in which integrated DRAM with low-voltage swing I/O can be implemented.

[0056] In the following some exemplary embodiments are described

[0057] Example 1: A system-in-package comprising:

a die carrier, fabricated from silicon, having one or more redistribution layers (RDLs) of respective traces, the RDLs configured to connect at least two integrated circuit die;

an application processor (AP) die having Low-Voltage Swing Input/Output (LVSIO) circuitry, the AP die mounted, via microbumps, to pads of the one or more RDLs of the die carrier; and

a dynamic random access memory (DRAM) die having other LVSIO circuitry, the DRAM die mounted, via other microbumps, to other pads of the one or more RDLs of the die carrier, the respective traces of the one or more RDLs providing a data bus between the DRAM die and the AP die.

[0058] Example 2: The system-in-package as recited in example 1, wherein:

the respective traces of a first redistribution layer of the one or more RDLs are configured as a data bus; and

a second RDL of the one or more RDLs of the die carrier is configured as a power plane.

[0059] Example 3: The system-in-package as recited in example 1 or 2, wherein data inputs/outputs (I/Os) of the AP die are located at, or proximate, in particular between 100 and 1000 μm, in particular 530 μm, an edge of the AP die and other data I/Os of the DRAM die are located at, or proximate, in particular between 100 and 1000 μm, in particular 530 μm, an edge of the DRAM die.

[0060] Example 4: The system-in-package as recited in at least one of the preceding examples, wherein the other LVSIO circuitry is configured to operate with an output stage logic power voltage of 0.3 volts or less.

[0061] Example 5: The system-in-package as recited in at least one of the preceding examples, wherein the respective traces of the one or more RDLs that provide the data bus are un-terminated.

[0062] Example 6: The system-in-package as recited in at least one of the preceding claims , wherein the DRAM die further comprises metallic test pads.

[0063] Example 7: The system-in-package as recited in at least one of the preceding examples, wherein the respective traces of the one or more RDLs that provide the data bus are configured to support at least four channels of memory access.

[0064] Example 8: The system-in-package as recited in example 7, wherein each of the four channels of memory access is powered by a respective power distribution network.

[0065] Example 9: The system-in-package as recited in example 7 or 8, wherein each channel of the four channels of memory access supports an 8 byte wide data I/O.

[0066] Example 10: A method comprising:

dicing, from a first semiconductor wafer, a plurality of dynamic random access memory (DRAM) die, each DRAM die having Low Voltage Swing Input/Output (LVSIO) circuitry to communicate data via data inputs/outputs (I/Os), the data I/Os located at, or proximate, an edge of the DRAM die;

dicing, from a second semiconductor wafer, a plurality of application processor (AP) die, each AP die configured with other LVSIO circuitry to communicate data via other data I/Os, the other data I/Os located at, or proximate, an edge of the AP die;

selecting a DRAM die from the plurality of DRAM die and an AP die from the plurality of AP die; and

mounting, via microbumps, the selected DRAM die and the selected AP die to pads of one or more redistribution layers (RDLs) of a die carrier, the die carrier fabricated from a silicon substrate.

[0067] Example 11: The method as recited in example 10, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs electrically connects the data I/Os and the other data I/Os.

[0068] Example 12: The method as recited in example 10 or 11, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs electrically connects the DRAM die and the AP die to a power plane.

[0069] Example 13: The method as recited in at least one of examples 10 to 12, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs mounts the dies adjacent to one another.

[0070] Example 14: The method as recited in at least one of examples 10 to 13, wherein selecting the DRAM die from the plurality of DRAM die is based, at least in part, on test data collected via test pads located on the DRAM die.

[0071] Example 15: A system-in-package comprising:

an application processor (AP) die having Low Voltage Swing Input/Output (LVSIO) circuitry and having data inputs/outputs (I/O's) located at, or proximate, an edge of the AP die, the AP die fixed to a first planar surface;

a dynamic random access memory (DRAM) die having other LVSIO circuitry and having other data I/O's located at, or proximate, an edge of the DRAM die, the DRAM die fixed to a second planar surface that is parallel to the first planar surface and such that the other data I/O's located at, or proximate, the edge of the DRAM die are adjacent to the data I/O's located at, or proximate, the edge of the AP die; and

an electrical connection, the electrical connection connecting the data I/O's located at, or proximate, the edge of the AP die and the other data I/O's located at, or proximate, the edge of the DRAM die.

[0072] Example 16: The system-in-package as recited in example 15, wherein the first planar surface is a surface other than a surface of the DRAM die and the second planar surface is a surface of the AP die.

[0073] Example 17: The system-in-package as recited in example 15 or 16, wherein the first planar surface is a surface other than a surface of the AP die and second planar surface is a surface of the DRAM die.

[0074] Example 18: The system-in-package as recited in at least one of examples 15 to 17, wherein the electrical connection is a wirebond.

[0075] Example 19: The system-in-package as recited in at least one of examples 15 to 18, wherein the first planar surface and the second planar surface are a same surface.

[0076] Example 20: The system-in-package as recited in example 19, wherein the electrical connection is a wirebond.

CLAIMS

1. A system-in-package comprising:

a die carrier, fabricated from silicon, having one or more redistribution layers (RDLs) of respective traces, the RDLs configured to connect at least two integrated circuit die;

an application processor (AP) die having Low-Voltage Swing Input/Output (LVSIO) circuitry, the AP die mounted, via microbumps, to pads of the one or more RDLs of the die carrier; and

a dynamic random access memory (DRAM) die having other LVSIO circuitry, the DRAM die mounted, via other microbumps, to other pads of the one or more RDLs of the die carrier, the respective traces of the one or more RDLs providing a data bus between the DRAM die and the AP die.

2. The system-in-package as recited in claim 1, wherein:

the respective traces of a first redistribution layer of the one or more RDLs are configured as a data bus; and

a second RDL of the one or more RDLs of the die carrier is configured as a power plane.

3. The system-in-package as recited in claim 1 or 2, wherein data inputs/outputs (I/Os) of the AP die are located at, or proximate, in particular between 100 and 1000 μm, in particular 530 μm, an edge of the AP die and other data I/Os of the DRAM die are located at, or proximate, in particular between 100 and 1000 μm, in particular 530 μm, an edge of the DRAM die.

4. The system-in-package as recited in at least one of the preceding claims, wherein the other LVSIO circuitry is configured to operate with an output stage logic power voltage of 0.3 volts or less.

5. The system-in-package as recited in at least one of the preceding claims, wherein the respective traces of the one or more RDLs that provide the data bus are un-terminated.

6. The system-in-package as recited in at least one of the preceding claims, wherein the DRAM die further comprises metallic test pads.

7. The system-in-package as recited in at least one of the preceding claims, wherein the respective traces of the one or more RDLs that provide the data bus are configured to support at least four channels of memory access.

8. The system-in-package as recited in claim 7, wherein each of the four channels of memory access is powered by a respective power distribution network.

9. The system-in-package as recited in claim 7 or 8, wherein each channel of the four channels of memory access supports an 8 byte wide data I/O.

10. A method comprising:

dicing, from a first semiconductor wafer, a plurality of dynamic random access memory (DRAM) die, each DRAM die having Low Voltage Swing Input/Output (LVSIO) circuitry to communicate data via data inputs/outputs (I/Os), the data I/Os located at, or proximate, an edge of the DRAM die;

dicing, from a second semiconductor wafer, a plurality of application processor (AP) die, each AP die configured with other LVSIO circuitry to communicate data via other data I/Os, the other data I/Os located at, or proximate, an edge of the AP die;

selecting a DRAM die from the plurality of DRAM die and an AP die from the plurality of AP die; and

mounting, via microbumps, the selected DRAM die and the selected AP die to pads of one or more redistribution layers (RDLs) of a die carrier, the die carrier fabricated from a silicon substrate.

11. The method as recited in claim 10, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs electrically connects the data I/Os and the other data I/Os.

12. The method as recited in claim 10 or 11, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs electrically connects the DRAM die and the AP die to a power plane.

13. The method as recited in at least one of claims 10 to 12, wherein mounting the selected DRAM die and the selected AP die to the pads of the one or more RDLs mounts the dies adjacent to one another.

14. The method as recited in at least one of claims 10 to 13, wherein selecting the DRAM die from the plurality of DRAM die is based, at least in part, on test data collected via test pads located on the DRAM die.

15. A system-in-package comprising:

an application processor (AP) die having Low Voltage Swing Input/Output (LVSIO) circuitry and having data inputs/outputs (I/O's) located at, or proximate, an edge of the AP die, the AP die fixed to a first planar surface;

a dynamic random access memory (DRAM) die having other LVSIO circuitry and having other data I/O's located at, or proximate, an edge of the DRAM die, the DRAM die fixed to a second planar surface that is parallel to the first planar surface and such that the other data I/O's located at, or proximate, the edge of the DRAM die are adjacent to the data I/O's located at, or proximate, the edge of the AP die; and

an electrical connection, the electrical connection connecting the data I/O's located at, or proximate, the edge of the AP die and the other data I/O's located at, or proximate, the edge of the DRAM die.

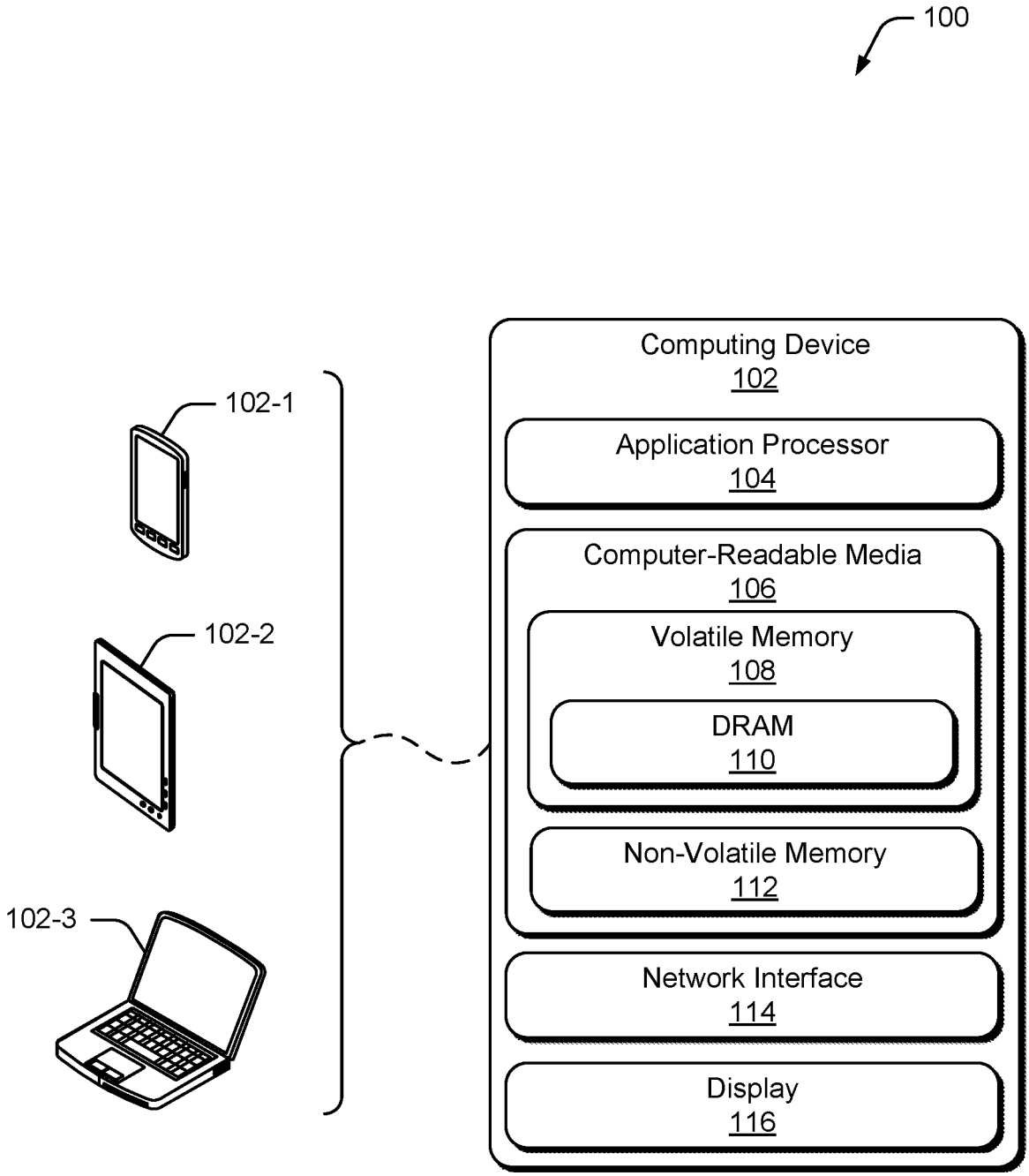
16. The system-in-package as recited in claim 15, wherein the first planar surface is a surface other than a surface of the DRAM die and the second planar surface is a surface of the AP die.

17. The system-in-package as recited in claim 15 or 16, wherein the first planar surface is a surface other than a surface of the AP die and second planar surface is a surface of the DRAM die.

18. The system-in-package as recited in at least one of claims 15 to 17, wherein the electrical connection is a wirebond.

19. The system-in-package as recited in at least one of claims 15 to 18, wherein the first planar surface and the second planar surface are a same surface.

20. The system-in-package as recited in claim 19, wherein the electrical connection is a wirebond.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102-1
102-2
102-3
Computing Device
102
Application Processor
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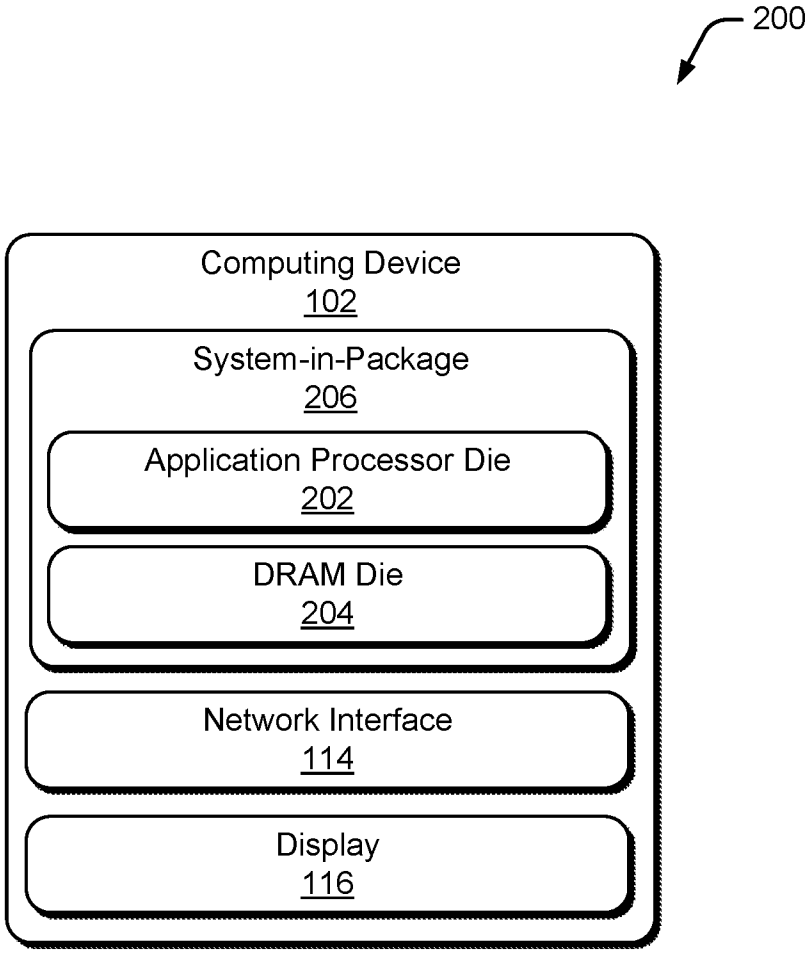
Computer-Readable Media
106
Volatile Memory
108
DRAM
110
Non-Volatile Memory
112
Network Interface
114
Display
116

Fig. 1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Application Processor Die
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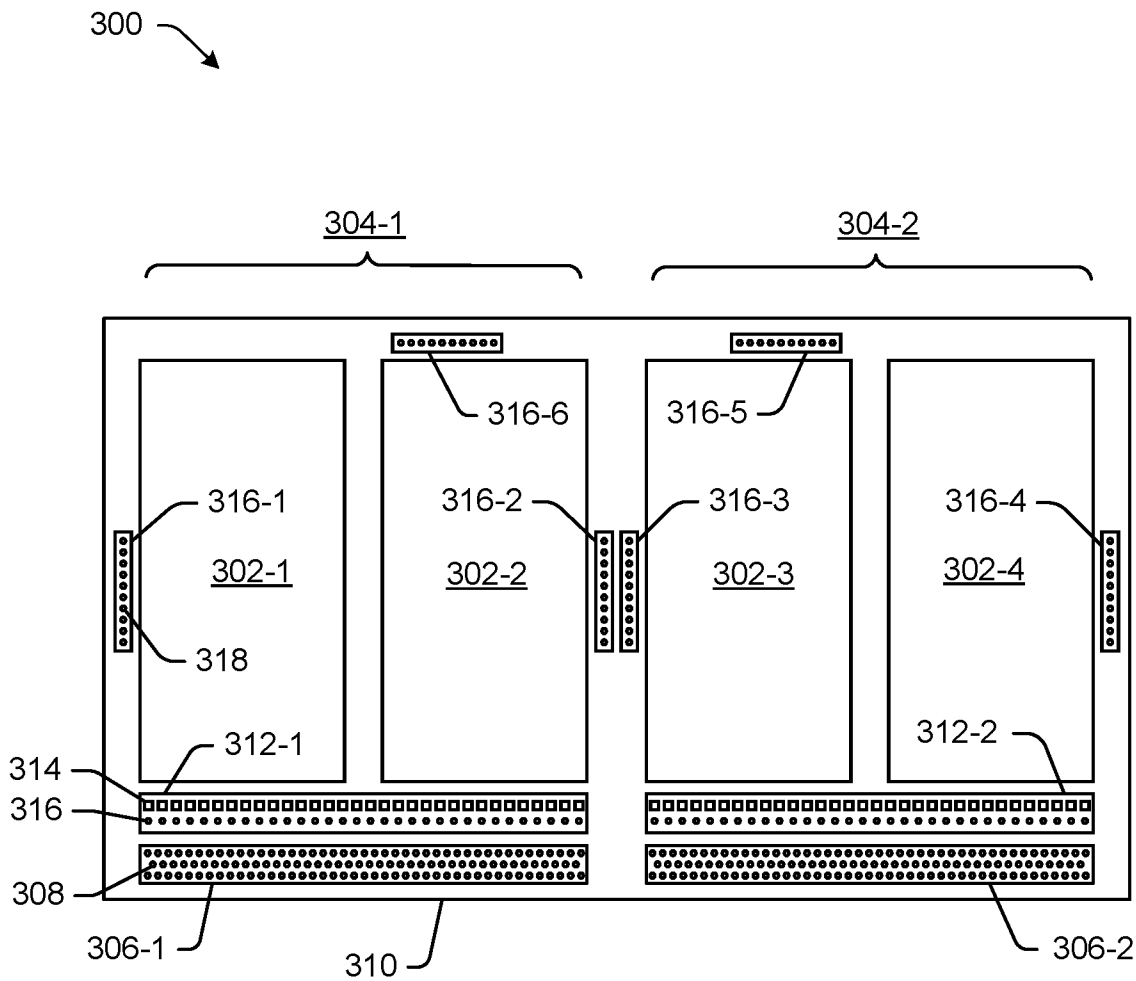
DRAM Die
204
Network Interface
114
Display
116

Fig. 2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304-2
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316-5
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316-2
316-3
316-4
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302-2
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302-4
318
312-1
312-2
314
316
308
306-1
310
306-2

Fig. 3

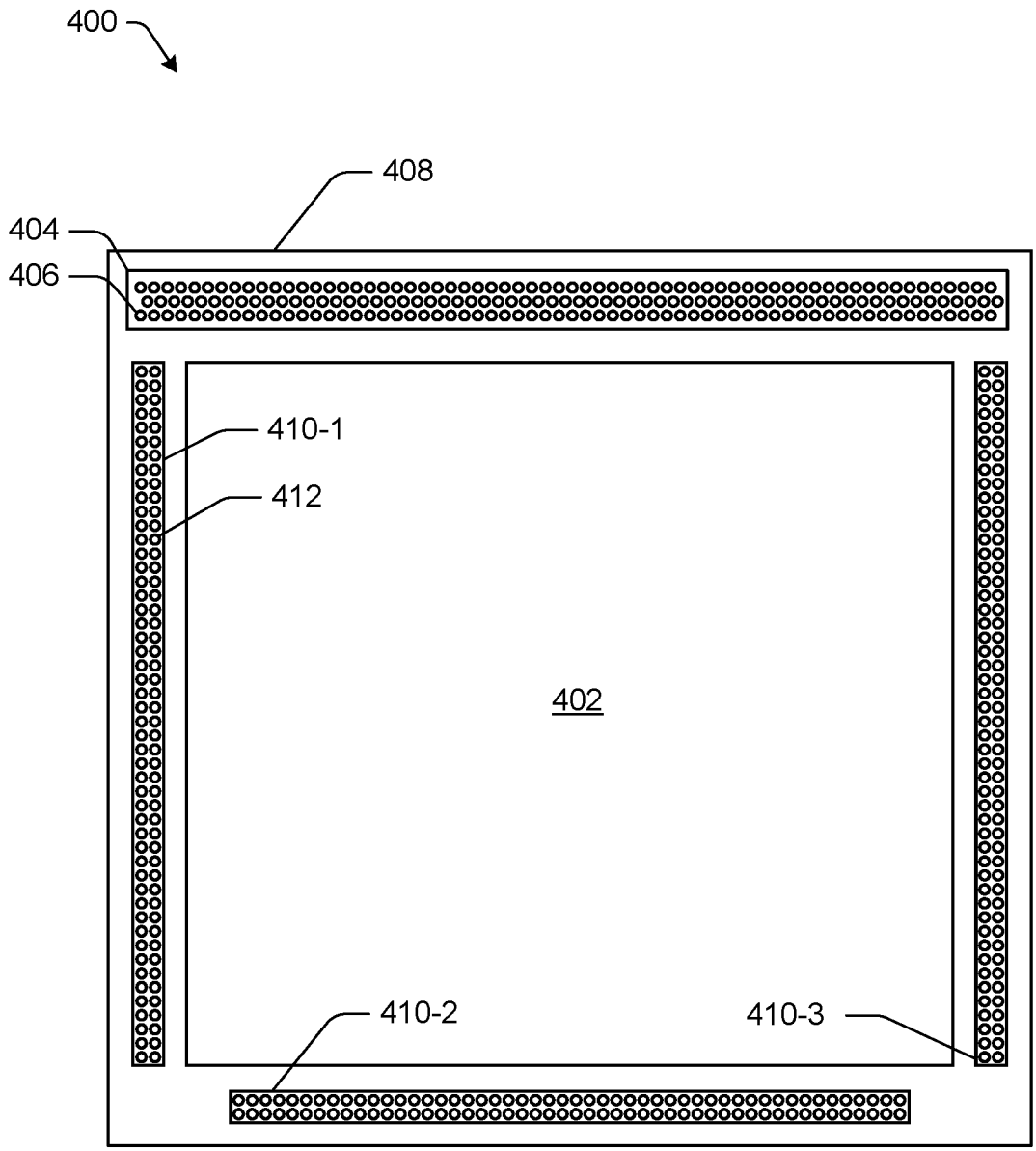
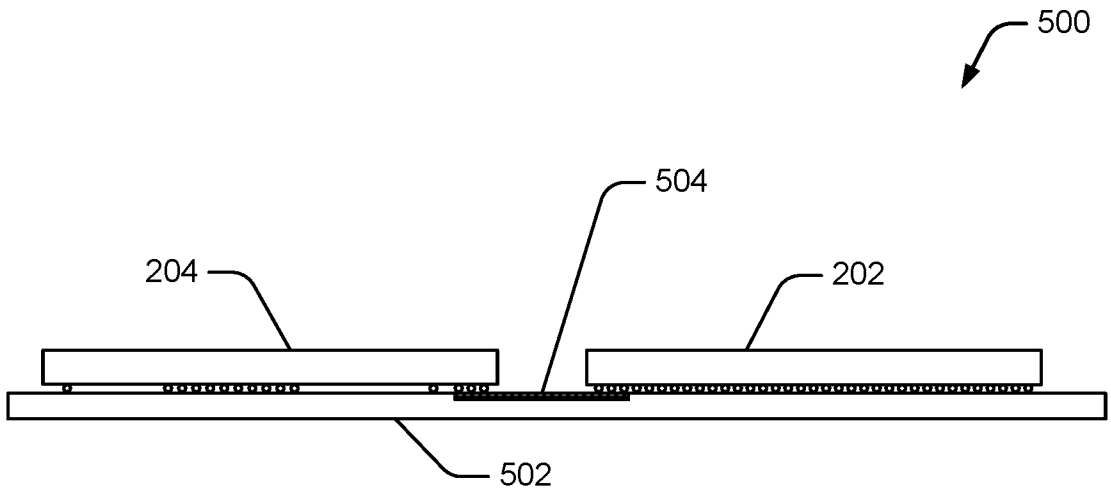


Fig. 4



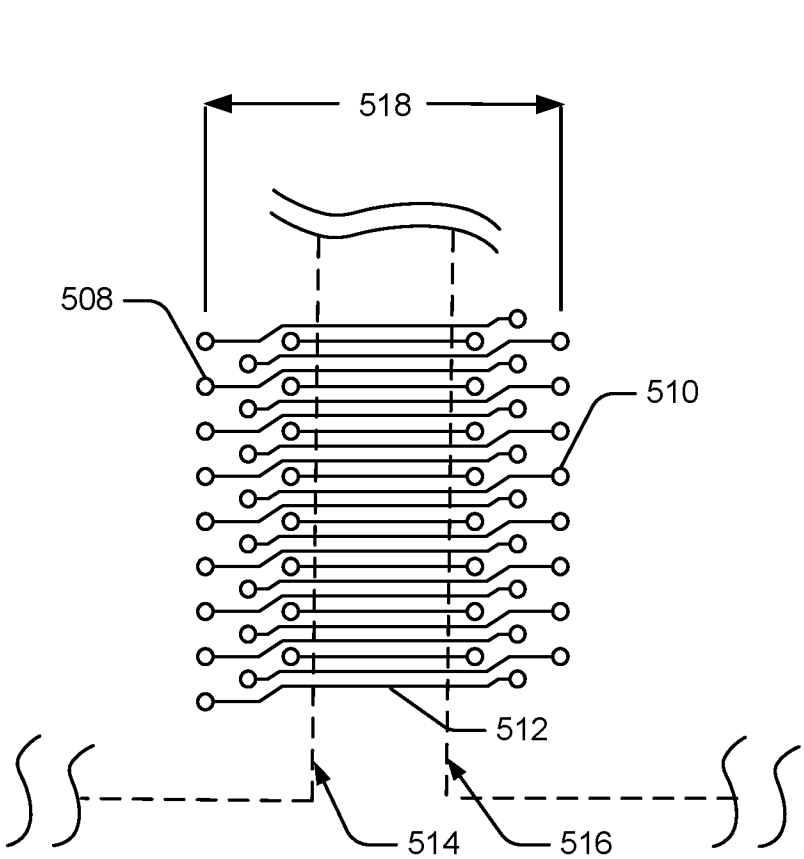
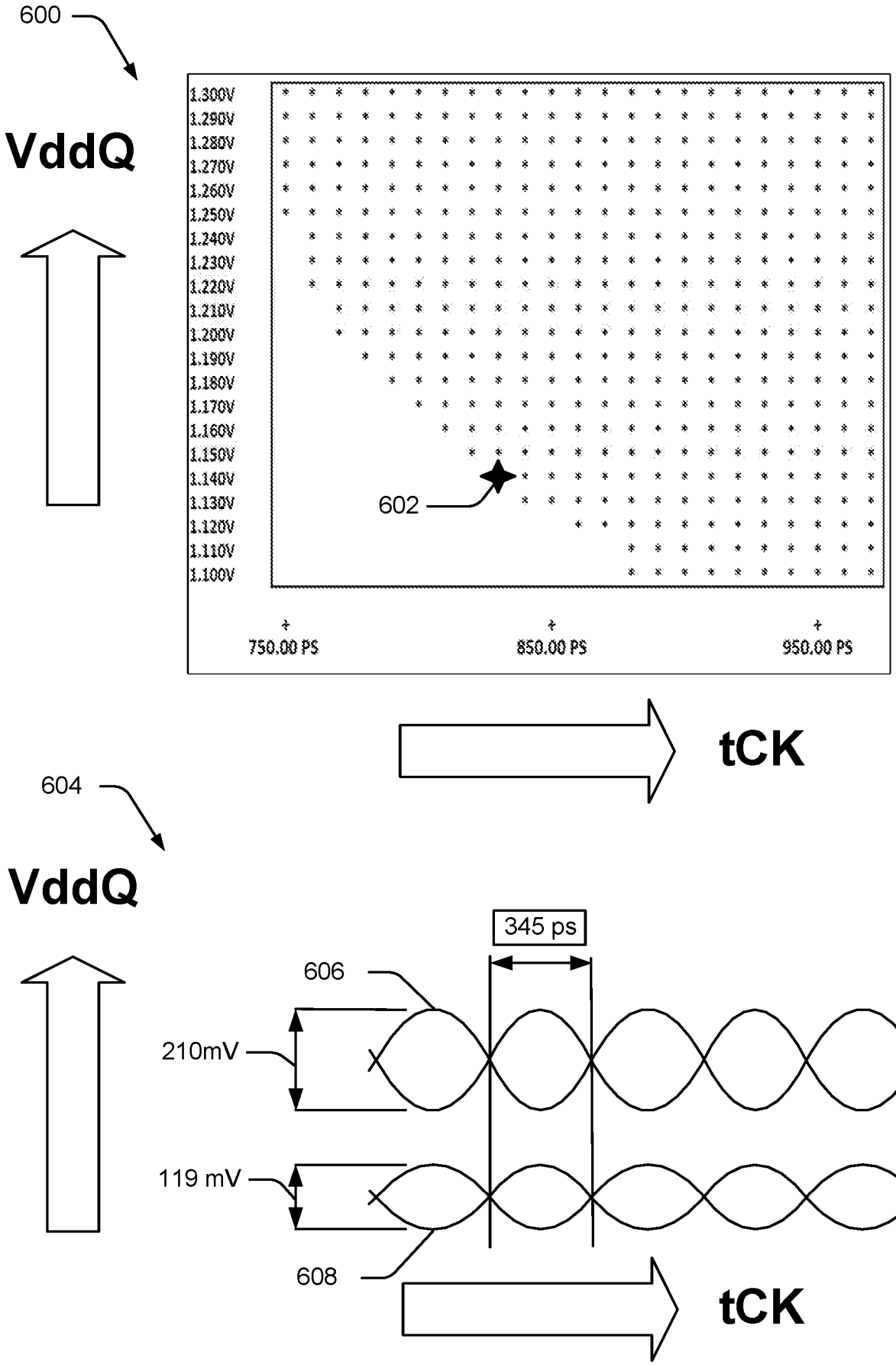


Fig. 5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VddQ
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1.280V
1.270V
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1.250V
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1.200V
1.190V
1.180V
1.170V
1.160V
1.150V
1.140V
1.130V
1.120V
1.110V
1.100V
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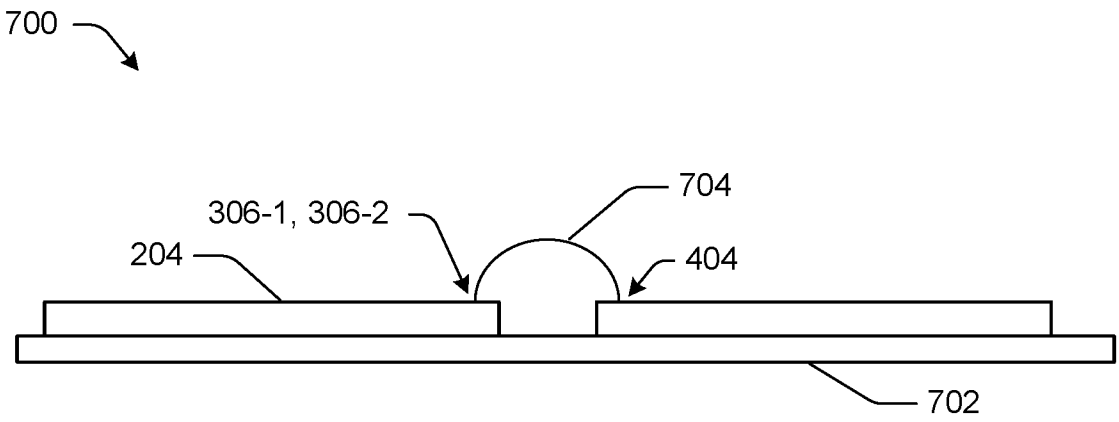
tCK
604
VddQ
345 ps
606
210mV
119 mV
608
tCK

Fig. 6



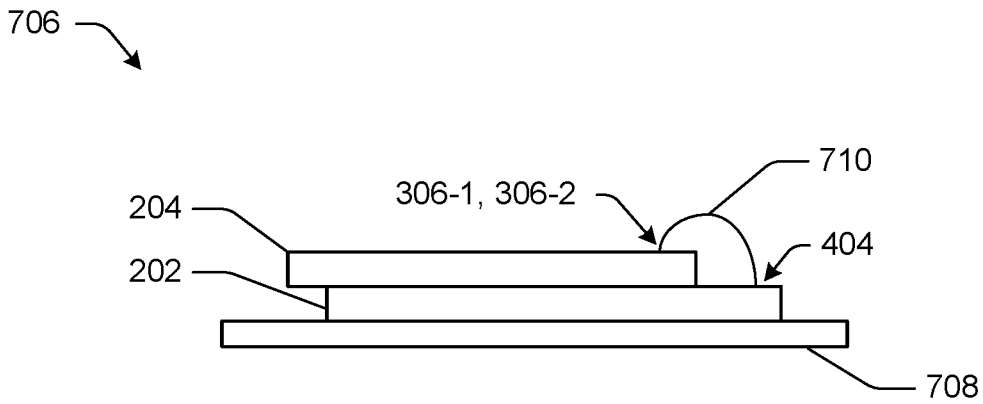


Fig. 7

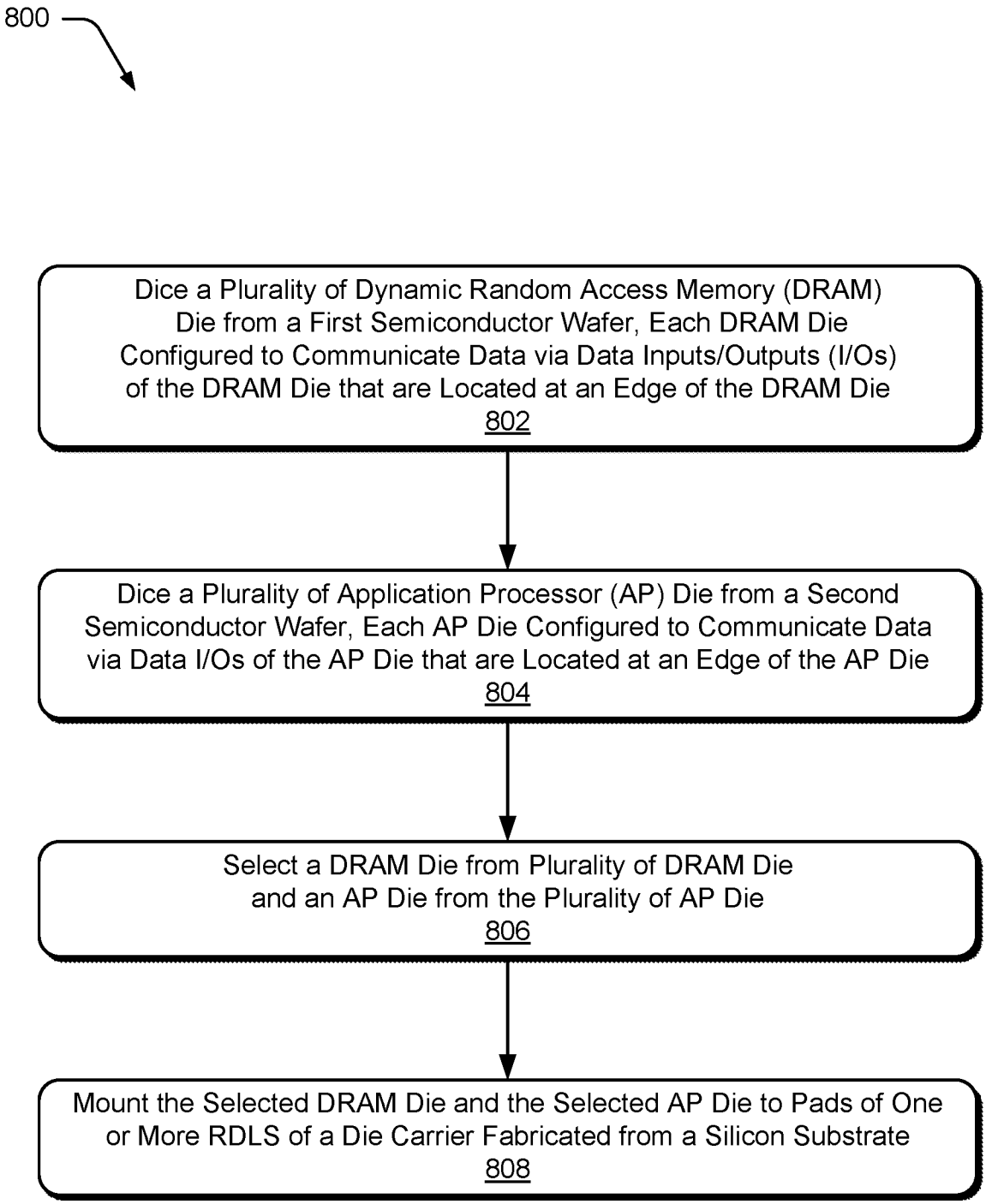

800
Dice a Plurality of Dynamic Random Access Memory (DRAM) Die from a First Semiconductor Wafer, Each DRAM Die Configured to Communicate Data via Data Inputs/Outputs (I/Os) of the DRAM Die that are Located at an Edge of the DRAM Die
802
Dice a Plurality of Application Processor (AP) Die from a Second Semiconductor Wafer, Each AP Die Configured to Communicate Data via Data I/Os of the AP Die that are Located at an Edge of the AP Die
804
Select a DRAM Die from Plurality of DRAM Die and an AP Die from the Plurality of AP Die
806
Mount the Selected DRAM Die and the Selected AP Die to Pads of One or More RDLS of a Die Carrier Fabricated from a Silicon Substrate
808

Fig. 8

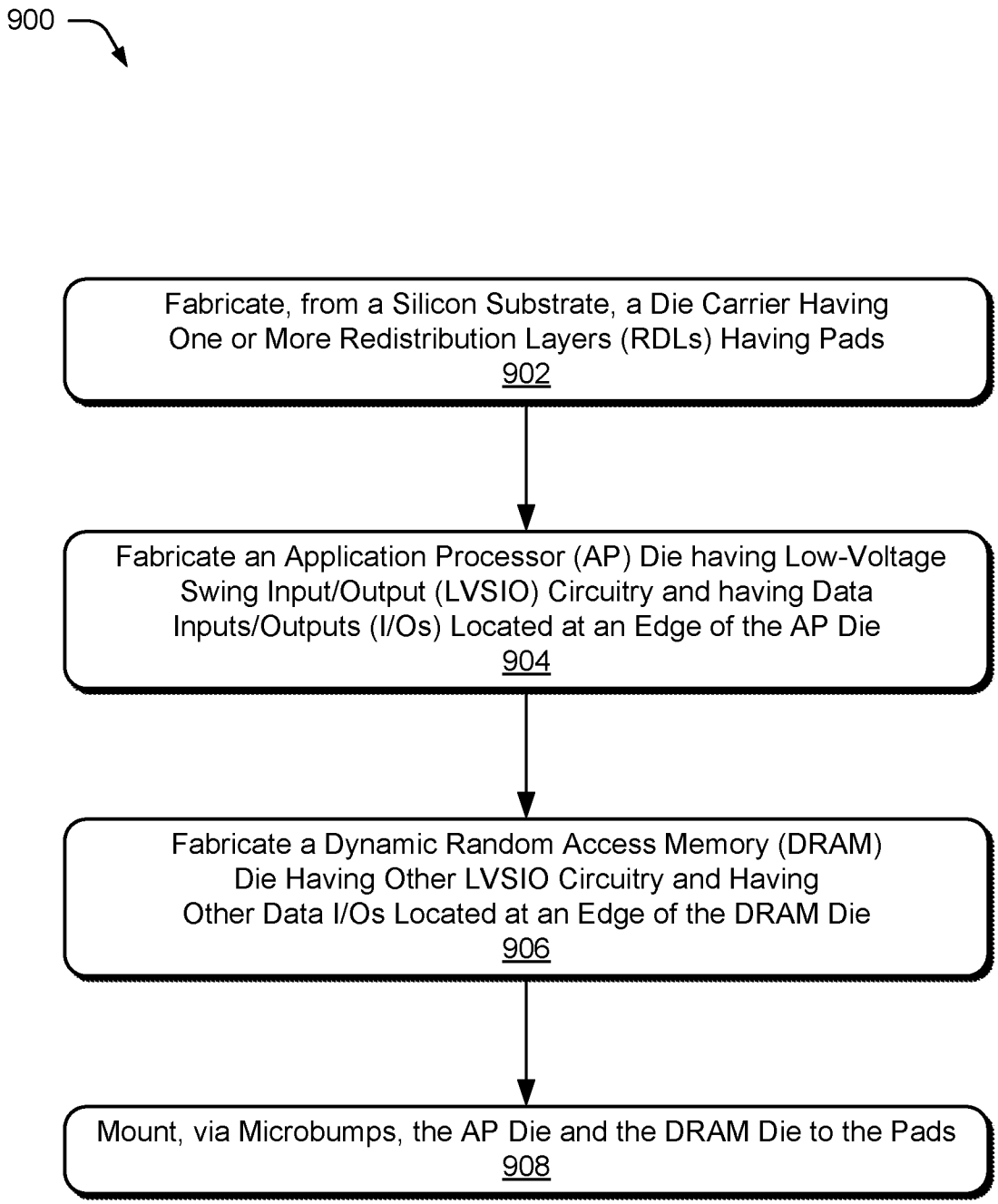
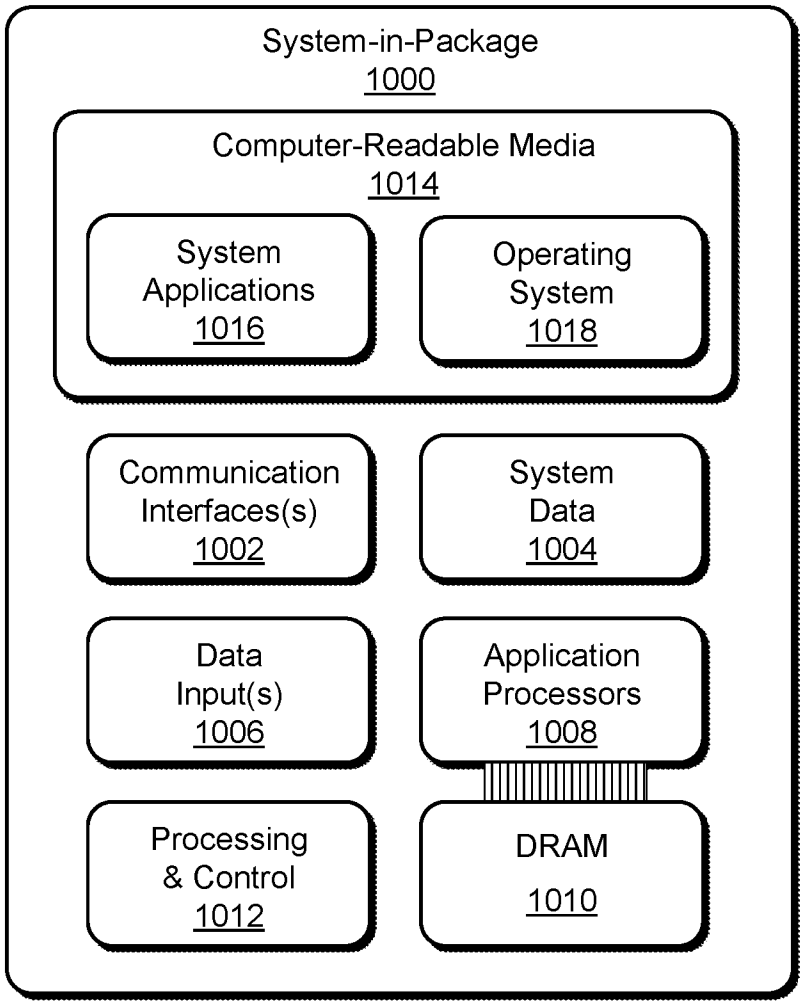

900
Fabricate, from a Silicon Substrate, a Die Carrier Having One or More Redistribution Layers (RDLs) Having Pads
902
Fabricate an Application Processor (AP) Die having Low-Voltage Swing Input/Output (LVSIO) Circuitry and having Data Inputs/Outputs (I/Os) Located at an Edge of the AP Die
904
Fabricate a Dynamic Random Access Memory (DRAM) Die Having Other LVSIO Circuitry and Having Other Data I/Os Located at an Edge of the DRAM Die
906
Mount, via Microbumps, the AP Die and the DRAM Die to the Pads
908

Fig. 9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Computer-Readable Media
1014
System Applications
1016
Operating System
1018
Communication Interfaces(s)
1002
System Data
1004
Data Input(s)
1006
Application Processors
1008
Processing & Control
1012
DRAM
1010

Fig. 10

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
20172600PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2017/058087	24 October 2017 (24-10-2017)	20 January 2017 (20-01-2017)
Applicant		
GOOGLE LLC		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 5
      [ ] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [X] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/058087

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C5/04 G11C5/06 G11C5/14 G11C29/48 H01L25/065
ADD. G11C7/10 G11C11/4093

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LIN MU-SHAN ET AL: "A 1 Tbit/s Bandwidth 1024 b PLL/DLL-Less eDRAM PHY Using 0.3 V 0.105 mW/Gbps Low-Swing IO for CoWoS Application", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 49, no. 4, 1 April 2014 (2014-04-01), pages 1063-1074, XP011544011, ISSN: 0018-9200, DOI: 10.1109/JSSC.2013.2297399 [retrieved on 2014-03-24] page 1063 - page 1069; figures 1,3b,5 -----	1-15,19
X	US 2012/326282 A1 (SUTARDJA SEHAT [US]) 27 December 2012 (2012-12-27) paragraph [0058] - paragraph [0060]; figures 2-13 ----- -/--	1,10, 15-20

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2018	24/01/2018

Name and mailing address of the ISA/	Authorized officer
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1

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2007/187814 A1 (CUSACK MICHAEL D [US] ET AL) 16 August 2007 (2007-08-16) figure 2	1-20

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