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(54) Title: METHODS AND APPARATUS FOR RESONANT ENERGY MINIMIZATION IN POWER CONVERTERS

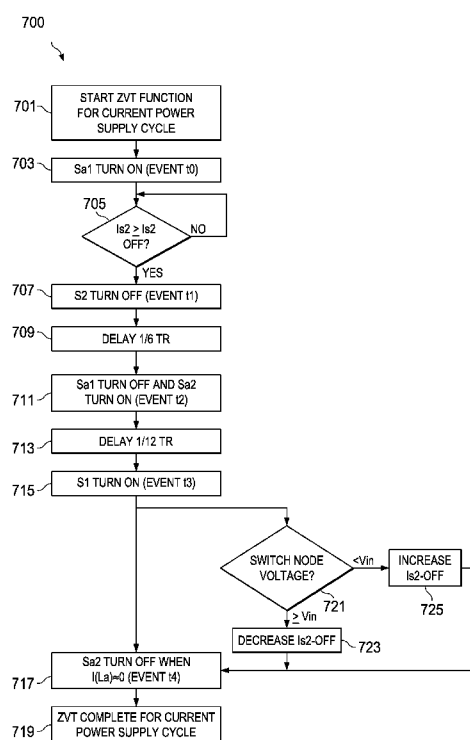


FIG. 7

(57) Abstract: In described examples, a zero voltage transition circuit includes an input node, an output node, a switch node, an output inductor coupling the switch node and output node, an output capacitor coupling the output node and ground, a first switch coupling the input node and switch node, a second switch coupling switch node and ground, a first auxiliary switch coupling the input node to an auxiliary node, a second auxiliary switch coupling the auxiliary node to ground, and an auxiliary inductor coupling the auxiliary node to the switch node. An example method (700) includes: closing the first auxiliary switch (703) to couple the input to the auxiliary node; subsequently, when a current is below a cutoff threshold (705), opening the second switch (707); after a first delay period (709), opening the first auxiliary switch (711) and closing the second auxiliary switch; and after a second delay period (713), closing the first switch (715).



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METHODS AND APPARATUS FOR RESONANT ENERGY MINIMIZATION IN POWER CONVERTERS

[0001] This relates generally to electronic circuitry, and more particularly to methods and circuitry for increased efficiency in switching power converters using zero voltage transition (ZVT) switching at the primary power switch or transistor sourcing power to a load.

BACKGROUND

[0002] Switching power supplies have existed for several decades and are currently heavily used in the electronics industry. Switching power supplies are commonly found in many types of electronic equipment, such as industrial machinery, automotive electronics, computers and servers, mobile consumer electronics (e.g., mobile phones and tablets), battery chargers for mobile electronics, and low cost/light weight items (e.g., wireless headsets and key chain flashlights). Many applications include switching power supplies for portable battery powered devices where an initial voltage is stepped down to a reduced voltage for part of the device, such as integrated circuits that operate at fairly low DC levels. Switching supplies are popular because they can be arranged to be light weight, low cost and highly efficient in the conversion of the voltage and current levels of electric power when compared to conventional approaches that use non-switching power supplies (such as linear power supplies).

[0003] High efficiency is achieved in switching power supplies by using high speed low loss switches (such as MOSFET transistors) to transfer energy from the input power source (such as a battery) to the electronic equipment being powered (the load) only when needed, so as to maintain the voltage and current levels required by the load.

[0004] Switching power supplies, which perform conversion from a direct current (DC) input (such as a battery) that supplies electric energy within a specific voltage and current range to a different DC voltage and current range required by the load, are known as “DC-DC” converters. Many conventional DC-DC converters are able to achieve efficiencies near or above 90% by employing zero voltage transition (ZVT) functionality. The ZVT technique was developed by Hua, et. al. and described in a paper published in 1994 (“Novel Zero-Voltage-Transition PWM Converters,” G. Hua, C.-S. Leu, Y. Jiang, and F. C. Lee, IEEE Trans. Power Electron., Vol. 9,

No. 2, pp. 213-219, Mar. 1994). The use of the ZVT function in conventional DC-DC converters reduces energy loss that would otherwise occur due to switching and has the additional benefit of reducing voltage stress on primary power switches of DC-DC converters. Reduction in voltage stress on a switch allows the switch to have a lower voltage tolerance rating, so potentially the switch can be made smaller and less costly.

[0005] The ZVT circuitry of conventional DC-DC converters introduces additional switches and corresponding additional energy loss and voltage stress on switching elements. However, the impact of energy loss and voltage stress of the ZVT function is much less significant than the overall performance improvements to switching converters that employ ZVT functionality. If energy loss and voltage stress of the ZVT function are reduced, then electronic equipment might be improved in multiple ways, such as increased battery life, lower cost of operation, and improved heat management.

[0006] To better illustrate shortcomings of conventional ZVT approaches, FIG. 1 shows a conventional ZVT DC-DC converter circuit 10 arranged in a circuit topology known as a buck converter. Buck DC-DC converters provide an output voltage at a lower voltage than an input voltage. Other types of DC-DC converters that can benefit from the use of ZVT switching include boost converters that increase voltage to the load to a voltage greater than the input voltage, and buck-boost DC-DC converters that dynamically transition between the buck and boost functions to adapt to various input voltage levels that could be either greater or less than the output voltage required by the load.

[0007] FIG. 1 illustrates a simplified circuit diagram of the switching elements, key passive components, and key parasitic elements of the circuit 10. For simplicity of explanation, FIG. 1 omits minor components, minor parasitic elements, the circuits for monitoring output voltage, and the control circuit for controlling the switch timing in conventional ZVT DC-DC buck power converters.

[0008] Circuit 10 of FIG. 1 contains two primary power switches, S1 and S2, that (in conjunction with the output inductor L_o and capacitor C_o) are used to perform a primary function of the buck converter of supplying energy to the load (represented as a resistive load, R_o) at an output voltage level V_o that is a reduced voltage from the DC input voltage, V_{in} . V_{in} represents both the external element that is the source of input voltage (such as a battery or another power supply) to the ZVT power converter and the voltage level across the positive and

negative terminals of the V_{in} input voltage source. Auxiliary switches $Sa1$ and $Sa2$ and the auxiliary inductor L_a are the extra components (added to conventional switching converter topology) that are used to accomplish the ZVT functionality. A primary parasitic inductance that contributes to voltage stress on switch $S2$ is represented in FIG. 1 by inductor L_{byp} . The source terminal of $S1$, the drain terminal of $S2$ and one terminal of each inductor L_a and L_o are coupled as illustrated in FIG. 1 to a common node, which is known as the switch node and labeled Switch Node in FIG. 1. The first auxiliary switch $Sa1$, the second auxiliary switch $Sa2$, and the auxiliary inductor L_a are coupled together at an auxiliary node labeled Aux Node. All four switches in the example buck converter 10 of FIG. 1 ($S1$, $S2$, $Sa1$ and $Sa2$) are enhancement mode n-channel MOSFETs. Drain to source parasitic capacitances of switches $S1$ and $S2$ are important to the circuit description and are illustrated in FIG. 1 as C_{ds1} and C_{ds2} respectively. The intrinsic body diode of MOSFET switches is also shown connected between source and drain for all switches ($S1$, $S2$, $Sa1$, and $Sa2$) of FIG. 1.

[0009] Enhancement mode n-channel MOSFETs are commonly used as switches in conventional DC-DC converters as shown in the example in FIG. 1, but other types of transistor switches (and diode switches in some cases) have been employed and can be used to form the buck converter 10 or other types of switching power converters.

[0010] Circuit 10 of FIG. 1 accomplishes the primary buck converter function of supplying a reduced voltage to the load (voltage across resistor R_o) by alternatively switching between two primary states. In one of the primary states (defined by switch $S1$ closed and switch $S2$ open, which means switch $S1$ is a transistor that is turned on, while switch $S2$ is a transistor that is turned off), the input voltage source (V_{in}) supplies energy to the load, and energy to maintain or increase magnetic energy is also stored in inductor L_o . In the other primary state (defined by switch $S1$ open and switch $S2$ closed, which means that switch $S1$ is a transistor that is turned off, while switch $S2$ is a transistor that is turned on), current flow from the input (V_{in}) is blocked, and the magnetic energy stored in inductor L_o is converted to electric energy and supplies energy to the load (resistor R_o). The voltage across the load R_o is maintained in a predefined range by varying the relative amount of time the circuit spends in each primary state. Converters that alternate between the two states described hereinabove are sometimes described as pulse width modulated (PWM) switching converters, because the output V_o is proportional to the input voltage V_{in} , multiplied by the duty cycle of switch $S1$ (a ratio of the on time of switch

S1 to the total cycle period). Typically, conventional buck converters cycle between these states rapidly (often at hundreds of KHz to 1 MHz and above). In addition to the two primary states, brief dead times occur during the transitions between the two primary states. During the dead times, switches S1 and S2 are simultaneously open, so the transistors implementing switches S1 and S2 are simultaneously turned off. Dead times ensure that a high current path does not exist across the input voltage source (V_{in}) directly to ground, which could occur when both S1 and S2 are closed. Conventional PWM switching power supplies employ two dead times during each cycle of operation: a first dead time occurs when switch S1 opens and ends when switch S2 closes; and a second dead time occurs when switch S2 opens and ends when switch S1 closes. The ZVT function operates in a small amount of time that begins before the beginning of the second dead time with S2 opening, and the ZVT function ends a small amount of time after the second dead time ends with switch S1 closing. The ZVT function does not operate in the first dead time of the buck converter cycle described hereinabove (the time between switch S1 opening and S2 closing).

[0011] FIG. 2 is a timing diagram of the sequence of switch transition events to operate ZVT functionality for conventional ZVT DC-DC buck converters. In FIG. 2 the switching events are labeled t_0 , t_1 , t_3 , and t_4 . For increasing simplicity of explanation, no event is labeled t_2 in FIG. 2. The dead time described hereinabove during the time interval between switch S2 opening and switch S1 closing begins at event t_1 and ends at event t_3 illustrated in FIG. 2.

[0012] The open and closed states of each of the four switches (S1, S2, Sa1 and Sa2) illustrated in FIG. 1 are represented in FIG. 2 by the voltage applied to the switch gates (V_{g1} , V_{g2} , V_{ga1} , and V_{ga2} respectively) and shown in four graphs, graph 201 illustrates the voltage on the gate of switch S1, graph 202 illustrates the voltage on the gate of switch S2, graph 203 illustrates the voltage on the gate of switch S3, and graph 204 illustrates the voltage on the gate of switch S4. A voltage annotated as V_{on} applied to a switch gate indicates the switch is closed, and a voltage annotated as V_{off} indicates the switch is open. The purpose of FIG. 2 is to illustrate of the sequence of switching events, and does not illustrate specific voltage levels, waveform shapes, and time increments.

[0013] ZVT functionality for conventional approaches begins at event labeled t_0 in FIG. 2 with switch Sa1 turning on as shown in graph 203. In the time leading up to event t_0 switch S2 has been closed and switches S1 and Sa2 have been open for a significant portion of the current buck

converter cycle. Time progresses to event t1 illustrated in FIG. 2 when switch S2 opens as shown in graph 202. At the next event, t3, switches S1 and Sa2 close as shown in both graphs 201, 204. Switch Sa1 opens at time t3, as shown in graph 203, and after a short delay to provide the dead time, Sa2 closes just after event t3 as shown in graph 204. At event t4, Sa2 opens as shown in graph 204 to complete ZVT functionality for the current cycle of the buck converter.

[0014] The conventional ZVT buck converter circuit 10 of FIG. 1 accomplishes ZVT when the primary power switch S1 transitions from open to closed (S1 turn on as shown in graph 201) at event labeled t3 illustrated in FIG. 2 with zero or near zero volts across it. For the circuit 10 to reach a condition with zero or near zero volts across switch S1 before S1 turning on or closing, an L-C resonant circuit is used to increase the voltage at the source terminal of switch S1 (coupled to the node “switch node” in FIG. 1) until approximately equivalent to the voltage at the drain terminal of S1, which is coupled to and approximately equivalent to the input voltage, V_{in} . The above L-C resonant circuit includes the inductor L_a and the parallel combination of capacitances C_{ds1} and C_{ds2} (the drain to source parasitic capacitances of the switches S1 and S2 respectively) and is referenced herein as the “ZVT resonant circuit.” The ZVT resonant circuit is a portion of circuit 10. For conventional approaches, the ZVT resonant circuit resonates only when switch Sa1 is closed and switches S1, S2, and Sa2 are open, which is the time span between events t1 and t3 in FIG. 2. The time span between events t1 and t3 for conventional approaches is equivalent to one-quarter cycle of the natural resonant frequency of the ZVT resonant circuit.

[0015] Conventional DC-DC converters incorporating the ZVT function typically have lower energy loss and lower voltage stress on transistor switches when compared to conventional DC-DC converters formed without the ZVT function, but the ZVT function itself introduces energy loss and voltage stress.

[0016] Energy loss of conventional ZVT functions is caused by at least two key contributors. First, energy is lost when auxiliary switch Sa1 turns off when conducting peak current as it transitions through the MOSFET linear region. Second, energy is lost during the ZVT operation by the sum of conduction losses through switches Sa1, Sa2 and S1 and inductor L_a .

[0017] The most significant impact of voltage stress resulting from the ZVT function is on the voltage tolerance required for switch S2 and, therefore, this impacts S2 transistor size and potential cost. The voltage stress on switch S2 is the result of switch Sa1 turning off with peak

current flowing through it, causing a voltage spike across switch S2 induced by the parasitic inductance, L_{byp} . Also, a voltage spike occurs across Sa1 when it turns off with current flowing through it, due to ringing with parasitic inductances. However, sizing Sa1 for higher voltage tolerance is not a significant impact to potential converter cost, because Sa1 is already a small transistor when compared to the primary power transistors, S1 and S2.

[0018] Accordingly, improvements are desirable in performance and efficiency of ZVT converters, such as improvements to reduce the power losses of the ZVT converter over conventional approaches and to reduce voltage stress, enabling the use of smaller and lower cost components in the ZVT converter.

SUMMARY

[0019] In described examples, a zero voltage transition circuit includes an input node, an output node, a switch node, an output inductor coupling the switch node and output node, an output capacitor coupling the output node and ground, a first switch coupling the input node and switch node, a second switch coupling switch node and ground, a first auxiliary switch coupling the input node to an auxiliary node, a second auxiliary switch coupling the auxiliary node to ground, and an auxiliary inductor coupling the auxiliary node to the switch node.

[0020] An example method includes: closing the first auxiliary switch to couple the input to the auxiliary node; subsequently, when a current is below a cutoff threshold, opening the second switch; after a first delay period, opening the first auxiliary switch and closing the second auxiliary switch; and after a second delay period, closing the first switch.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 depicts a simplified circuit diagram illustrating the switching elements, key passive components, and key parasitic elements of a typical ZVT DC-DC buck power converter applicable to example embodiments.

[0022] FIG. 2 depicts a group of timing diagrams illustrating switch transition events and sequencing to operate ZVT functionality for conventional approaches.

[0023] FIG. 3 depicts a group of timing diagrams illustrating switch transition events and sequencing to operate ZVT functionality for example embodiments.

[0024] FIG. 4 depicts a group of waveform plots comparing current flow in a key element of example embodiments to current flow in conventional approaches.

[0025] FIG. 5 depicts an ideal equivalent circuit diagram of the ZVT resonant circuit of

example embodiments.

[0026] FIG. 6 depicts an ideal equivalent circuit diagram of the ZVT resonant circuit in an alternative embodiment.

[0027] FIG. 7 depicts a flow chart illustrating a sequence of switch transitions in a method of example embodiments.

[0028] FIG. 8 depicts a block diagram illustrating the modified switch sequencing and timing control of example embodiments.

[0029] FIG. 9 depicts in another circuit block diagram of an integrated circuit incorporating example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0030] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are not necessarily drawn to scale.

[0031] In this description, the term “coupled” includes “directly connected” and connections made with intervening elements. Additional elements and various connections may be used between any elements that are described as “coupled.”

[0032] Multiple comparisons of example embodiments and conventional approaches are provided below. In all cases, these comparisons are based on operating conditions, voltage source characteristics, and load characteristics being approximately identical for example embodiments and conventional approaches. Further, the comparisons are based on approximately equivalent circuit operations of example embodiments and conventional approaches, except where an aspect of the arrangement or circuit operation is different as described below. The comparisons below of example embodiments and conventional approaches are not limited to a specific circuit, operating condition, voltage source characteristic, or load characteristic. Example embodiments can be incorporated in and provide benefit to a broad range of switching power converters employing ZVT technology.

[0033] As discussed above, FIG. 1 illustrates a simplified circuit diagram 10 of the switching elements, key passive components, and key parasitic elements of a ZVT DC-DC buck power converter, where example embodiments can be incorporated and the advantages achieved can be accrued. For the purposes of diagram simplification, FIG. 1 omits minor components, minor parasitic elements, and the circuits for monitoring output voltage and controlling the switch timing, which exist in conventional approaches and example embodiments. Example

embodiments modify sequencing and timing of transitions for the switches of circuit 10. Accordingly, circuit 10 is referenced herein for convenience of describing switching events of example embodiments. By modifying the switch transition sequencing and timing, example embodiments achieve improved power efficiency and improved ZVT power converters with reduced semiconductor die area for switch implementation as described herein.

[0034] The modified switch transition sequencing and timing of example embodiments occurs during the operation of the ZVT function and does not significantly impact the operation of circuit 10 during a remainder of the power supply cycle. Accordingly, this description does not include a description of the full power supply cycle.

[0035] FIG. 3 illustrates a timing diagram of switch transition events to operate ZVT functionality for an example embodiment. In FIG. 3, the switching events are labeled t_0 , t_1 , t_2 , t_3 , and t_4 .

[0036] The open and closed states of each of the four switches (S_1 , S_2 , S_{a1} , and S_{a2}) illustrated in FIG. 1 are represented in FIG. 3 by the voltage applied to the switch gates (V_{g1} , V_{g2} , V_{ga1} , and V_{ga2} respectively). Graph 301 illustrates the voltage V_{g1} at the gate terminal of switch S_1 ; graph 302 illustrates the voltage V_{g2} at the gate terminal of switch S_2 ; graph 303 illustrates the voltage at the gate terminal of the switch S_{a1} ; and graph 304 illustrates the voltage at the gate terminal of switch S_{a2} . A voltage annotated as V_{on} applied to a switch gate indicates the switch is closed because a transistor is on, and a voltage annotated as V_{off} indicates the switch is open because a transistor is off. The purpose of the graphs 301, 302, 303 and 304 in FIG. 3 is to illustrate the sequence of switching events, and FIG. 3 does not illustrate specific voltage levels, waveform shapes, and time increments. For example embodiments and conventional approaches, a brief dead time occurs between switch S_{a1} turn off and switch S_{a2} turn on. This dead time ensures that a high current path does not exist from across the input voltage source V_{in} . The dead time between switch S_{a1} turn off and switch S_{a2} turn on does not significantly impact circuit 10 functionality. Accordingly, switch S_{a1} turn off, the intervening dead time, and switch S_{a2} turn on are illustrated as occurring in a single event (at time t_2) in FIG. 3 for further simplicity of explanation.

[0037] ZVT functionality for example embodiments begins with the event labeled t_0 in FIG. 3, with switch S_{a1} turning on, as shown in graph 303, while switch S_2 remains closed and switches S_1 and S_{a2} remain open. In FIG. 3 time progresses to event t_1 when switch S_2 opens as shown

in graph 302. At the next event, t_2 , as shown in FIG. 3, switch Sa1 opens as illustrated in graph 303, and after a short delay that fulfills the dead time requirement, switch Sa2 closes as shown in graph 304. Unlike example embodiments, conventional ZVT circuits do not employ a switching event at time t_2 . As shown in FIG. 3, at event t_3 for example embodiments, switch S1 is closing as illustrated in graph 301 at time t_3 . At event t_4 , switch Sa2 opens as shown in graph 304 to complete ZVT functionality for the current cycle of the buck converter.

[0038] Also, the waveform and timing diagrams provided herein are not annotated with voltage and current values and time increments, because specific values depend on a how a specific example is made. When waveforms are compared herein, the same relative voltage, current, and time scales are used.

[0039] For each successive span of time between the above stated switching events, this description includes: a description of the ZVT functionality and the modified switch transition sequencing and timing of example embodiments within the respective time span; a comparison to conventional approaches; and a description of the circuit functionality to control the modified switch sequencing and timing.

[0040] The first time span during the operation of the ZVT function is between events t_0 and t_1 as shown in FIG. 3. The ZVT function starts during each buck converter cycle at event t_0 . In the time leading up to t_0 , an example embodiment operates similarly to a conventional approach and has a state with switch S1 open and switch S2 closed and switches Sa1 and Sa2 open. At event t_0 switch Sa1 closes, allowing current to flow through the auxiliary inductor L_a , which ramps from zero amperes until the current flowing in inductor L_a is approximately equivalent to the current flowing through inductor L_o . Simultaneously, the current flowing in the closed switch S2 ramps to zero or near zero. As stated above, the behavior of circuit 10 for example embodiments and for conventional approaches is similar for the time interval starting at event t_0 and ending at event t_1 , with an exception being that the time at which t_1 occurs after event t_0 is adjusted by the control circuit of example embodiments, as further described below.

[0041] The adjustment to the time at which event t_1 occurs can be performed to modify the resonant trajectory of the ZVT resonant circuit, such that the switch node voltage will be equal or nearly equal to the input voltage, V_{in} , at event t_3 (ZVT functionality for subsequent events is described below). Adjusting the resonant trajectory on an on-going basis allows the ZVT function to adapt to dynamic changes in load and other operating conditions. The adjustment to

the time at which t_1 (following the events at t_0) occurs is accomplished indirectly by monitoring and adjusting the current I_{S2} flowing through switch S_2 when it is turned off at event t_1 . To accomplish the adjustment of the S_2 turn off current, the switch node voltage is measured at event t_3 . If the switch node voltage is equal to or greater than V_{in} at time t_3 , the target value (the current through S_2 when turned off, or I_{S2-off}) for the S_2 turn off current is incrementally reduced. If the switch node voltage is less than V_{in} , I_{S2-off} is incrementally increased. During the operation of the ZVT function of the immediately following buck converter cycle, the current in switch S_2 is monitored between events t_0 and t_1 and compared to I_{S2-off} (set in the previous cycle). In example embodiments, the switch S_2 is turned off when the current I_{S2} is equal to or less than I_{S2-off} .

[0042] The second time span during the operation of the ZVT function as shown in FIG. 3 is between events t_1 and t_2 . For example embodiments and conventional approaches, switch S_2 opens at event t_1 with zero or near zero current flowing through it, as shown in graph 302. Switches S_1 and S_{a2} remain open at t_1 . With only switch S_{a1} closed, the inductor L_a resonates with the parallel combination of the parasitic drain to source capacitances, C_{ds1} and C_{ds2} , of switches S_1 and S_2 respectively (the ZVT resonant circuit). In example embodiments, event t_2 occurs at a time that is $1/6 t_r$ after event t_1 , when the switch node reaches a voltage greater than $\frac{1}{2} V_{in}$, at which time S_{a1} is opened and S_{a2} is closed (after a short dead time delay) as shown in FIG. 3 in graphs 303, 304 at time t_2 and just after time t_2 . The natural resonant period of the ZVT resonant circuit is referenced herein as time “ t_r .”

[0043] Unlike example embodiments, in conventional ZVT converters, the event t_2 does not occur. In at least some conventional converters, the ZVT resonant circuit continues resonating on the same trajectory until the switch node (and, therefore, the source terminal of switch S_1) is equivalent or nearly equivalent to the input voltage, V_{in} , at event t_3 , when S_1 is then closed with zero or nearly zero volts across it, and resonance is then halted by opening switch S_{a1} and closing switch S_{a2} .

[0044] FIG. 4 illustrates: (a) graphs of the current in L_a , labeled $I(L_a)$, for example embodiments; and (b) graphs comparing the current obtained to the corresponding current obtained in conventional ZVT converters. The switching events t_0 , t_1 , t_2 , t_3 , and t_4 shown in FIG. 4 are duplicated from FIG. 3 for clarity of illustration. The time scales of FIG. 4 for $I(L_a)$ waveforms are the same for example embodiments and a conventional approach.

[0045] Graphs 401, 402, 403, and 404 of FIG. 4 correspond to the graphs 301, 302, 303 and 304 of FIG. 3 and depict the gate voltages on the switches S1, S2, Sa1, and Sa2 for the buck converter circuit 10 in FIG. 1, such as using a sequencing arrangement of example embodiments at the events t0, t1, t2, t3 and t4.

[0046] In FIG. 4, the current flowing in the inductor La is shown on separate graphs 411 (for example embodiments), 413 (for a conventional approach), and graph 415 which shows the current in inductor La for example embodiments and that of a conventional approach overlaid on the same set of axes. Graph 415 illustrates that example embodiments operate at lower inductor La current for a shorter time period during the time span between events t2 and t4. For the overlaid waveform diagram 415, a dashed line is used to illustrate current $I(L_o)$ for example embodiments and for conventional approaches where the waveforms differ significantly. In graphs 411, 413 and 415 of FIG. 4, the current through Lo is represented by fixed grid line labeled $I(L_o)$. In practice, $I(L_o)$ is not a fixed value and is load dependent. For simplicity of explanation, $I(L_o)$ is shown as a fixed value.

[0047] In example embodiments, another difference (compared to conventional approaches) is that a voltage spike occurs when switch Sa1 opens at event t2 with current flowing through it, due to ringing with parasitic inductances. In conventional buck converters, this voltage spike appears only across switch S2, because it is open and switch S1 is closed when the spike occurs. In contrast, example embodiments operate by opening switch Sa1 with both S1 and S2 open and before the drain to source capacitance of S1 (C_{ds1}) is fully discharged, distributing the voltage spike across both switches S1 and S2 in series. Specifically, in the operations of example embodiments, the series combination of the parasitic drain-source capacitances C_{ds1} and C_{ds1} of switches S1 and S2 respectively form a capacitive divider across which the voltage spike occurs. Dividing the voltage spike across both S1 and S2 advantageously reduces the voltage tolerance requirement of switch S2 when compared to the voltage tolerance requirement for the same switch in conventional approaches. In example embodiments, the voltage tolerance requirement of the switch S1 is not increased, because the spike across S1 when Sa1 opens is less than the voltage across S1 at other times during the operation of the buck converter.

[0048] In at least one example embodiment, the switch Sa1 can require a higher voltage tolerance than in a conventional ZVT buck converter. However, in other example embodiments, the voltage tolerance and the size of this transistor Sa1 can be the same as in a conventional ZVT

buck converter. In the ZVT buck converters, switch Sa1 is a significantly smaller transistor than the high power switches S1 and S2. Accordingly, even if (in certain cases) the size of Sa1 is increased, example embodiments result in a relatively small die area increase for the entire buck converter, and this potential die area increase can also easily be offset by a reduced die area for the most larger transistor that forms switch S2.

[0049] Yet another contrast (between example embodiments and conventional ZVT converters) is the possibility of switching Sa1 off more rapidly, which results from the modified approach of opening switch Sa1 before the time that the switch S1 source terminal voltage becomes approximately equal to the input voltage, V_{in} . In some example embodiments, the transistor Sa1 can be switched off more rapidly than in a conventional approach. In other arrangements, the turn off time can be retained as before. A more rapid turn off of switch Sa1 with current flowing through it will further reduce energy losses, because the amount of time the Sa1 transistor is conducting in the linear (resistive) region is reduced by the rapid turn off. A more rapid turn off of Sa1 also increases ringing with parasitic inductances, consequently increasing the voltage tolerance requirement of Sa1 and therefore requires a larger die area. However, for example embodiments, the potential exists to completely off-set any die area increase due to the increased size of the relatively small transistor Sa1 with the further reduced die area requirement of the much larger transistor S2 that can be achieved due to the new lower voltage tolerance requirement of S2, as described hereinabove.

[0050] The third time span during the operation of the ZVT function for example embodiments is between events t2 and t3. As stated above in the description of FIG. 3, event t2 of example embodiments occurs when the transition of switch Sa1 from closed to open occurs, and switch Sa2 transitions from open to closed shortly afterwards, with switches S1 and S2 remaining open. When switch Sa1 opens and switch Sa2 closes, the ZVT resonant circuit configuration is changed and the voltage across inductor La reverses. Current flow through inductor La will continue in the same direction, and resonance will continue on a different trajectory with the current in La resonating towards zero, resulting in the switch node continuing to charge. The energy stored in La at event t2 is sufficient to continue charging the switch node until it becomes approximately equivalent to the input voltage, V_{in} , provided the event at time t2 occurs with the switch node voltage still sufficiently above $\frac{1}{2}$ the V_{in} voltage level. For an ideal circuit, if t2 were to occur when the switch node is exactly $\frac{1}{2} V_{in}$, then sufficient energy should be stored in

inductor L_a for the switch node voltage to reach V_{in} . However, in example embodiments, t_2 should occur with the switch node at a voltage greater than $\frac{1}{2} V_{in}$, so as to accommodate component parameter variance and non-ideal circuit characteristics. The switch node voltage becomes approximately equivalent to V_{in} at a time that is $1/12 t_r$ after the event t_2 , at which time event t_3 occurs, with S_1 closing. This sequence is shown in graphs 401, 402, 403, and 404 at time t_3 .

[0051] FIG. 5 illustrates a simplified circuit diagram of an equivalent ideal ZVT resonant circuit of example embodiments in the configuration during the span of time from event t_1 to t_2 described hereinabove (circuit 50). FIG. 6 illustrates another simplified circuit diagram of the equivalent ideal ZVT resonant circuit for example embodiments in the configuration for the span of time from event t_2 to t_3 described hereinabove (circuit 60). Both circuits 50 and 60 illustrate a portion of circuit 10 of FIG. 1 with switches S_1 , S_2 , S_{a1} , and S_{a2} in the states described hereinabove for the respective time spans. For simplicity, in the diagrams for circuits 50 and 60, the switches S_{a1} and S_{a2} are treated as ideal and shown as interconnect conductors when closed and are simply not shown when open.

[0052] As described hereinabove, during the time period between events t_2 and t_3 for example embodiments, stored energy in inductor L_a is used to charge the switch node from a level greater than $\frac{1}{2} V_{in}$ to V_{in} . Unlike example embodiments, conventional ZVT converters use energy from the power converter input voltage source, V_{in} , to charge the switch node to be approximately equivalent to the input voltage, V_{in} . Consequently, more energy is stored in L_a and current is higher in L_a when switch S_1 closes at t_3 during operation of conventional approaches than for example embodiments. Greater stored energy in L_a and higher current through L_a result in greater energy losses for conventional approaches.

[0053] As stated above, the event t_2 of example embodiments is not part of the operation of conventional converters. Therefore, conventional ZVT resonant circuits continue resonance on the same trajectory for the full time span from t_1 to t_3 . In contrast, for example embodiments, the resonant trajectory is modified at event t_2 as described hereinabove.

[0054] As illustrated in FIG. 4, compared to conventional approaches, current through switch S_{a1} is lower when S_{a1} turns off during operation of example embodiments, due to ramping the switch node voltage to a level greater than $\frac{1}{2} V_{in}$. The turn off of switch S_{a1} is performed early when compared to conventional approaches, instead of waiting for the switch node voltage to be

approximately equivalent to V_{in} . As a result, energy lost by switch Sa1 while it is conducting in the transistor linear region during the transition from on to off for the transistor Sa1 is much lower for example embodiments.

[0055] The fourth and final time span during the operation of the ZVT function is between events t3 and t4. During the period of time between events t3 and t4, operation of example embodiments and conventional approaches is similar in that switch S1 turns on at event t3, and current in inductor La ramps down to zero, at which time Sa2 is turned off at event t4, ending the operation of the ZVT function for the current buck converter cycle. After switch S1 closes, the portion of the current in La that exceeds the current in Lo is returned to the source and the remainder of the current in La flows into Lo to supply the load.

[0056] In the time period between events t3 and t4, at least three differences exist between a conventional approach and example embodiments. The first difference is that switch Sa1 opens and switch Sa2 closes at t3 in conventional approaches; but, for example embodiments, Sa1 opens and Sa2 closes before the event t3 (at t2) as described hereinabove. The second difference is that a smaller fraction of the energy stored in inductor La is returned to the source than in conventional approaches, reducing energy losses for example embodiments. The third difference is that the inductor La current reaches its peak at t3 for conventional approaches; but, for example embodiments, the peak current through La is lower and the peak current is achieved earlier in time (at event t2), resulting in the time period from t3 to t4 being significantly shorter for example embodiments. Also, the time from t2 to t4 for example embodiments is shorter than the time from t3 to t4 for conventional approaches.

[0057] Compared to conventional approaches, the operation of example embodiments results in switches Sa1, Sa2, and S1 and inductor La each conducting for shorter amounts of time with lower RMS current levels, resulting in significantly lower energy loss. Advantages of example embodiments include: RMS current through Sa1, Sa2, S1, and La are lower for example embodiments, because Sa1 turns off before the switch node voltage reaching V_{in} , resulting in lower peak current in La, Sa1, and Sa2. Conduction time for switch Sa1 is reduced because it turns off earlier than in conventional approaches, turning off before the switch node voltage reaching V_{in} . Because the peak current in La is lower for example embodiments, the current in La ramps to zero in less time, resulting in lower RMS current in switch S1. Also, because the current in La ramps to zero more rapidly, the conduction times for Sa2, S1, and La are also

reduced.

[0058] FIG. 7 illustrates a flow chart of a method for operating the following modified switch sequencing and timing for the ZVT converter of example embodiments. At step 701, the zero voltage transition function of the buck converter begins. At step 703, the event described hereinabove at t_0 occurs, and the auxiliary switch Sa1 is turned on. At step 705, a decision loop begins. Current flowing through switch S2 is monitored and when it reaches a target current, indicating a time for switch S2 to turn off, the method transitions to step 707.

[0059] At step 707, the switch S2 is turned off, and example embodiments are implemented in the method. At step 709, a delay following the switch S2 turn off of $1/6$ the resonant period t_r is allowed to expire, then the method 700 transitions to step 711. At step 711, the auxiliary switch Sa1 is turned off, and the auxiliary switch Sa2 is then turned on, the event t_2 described hereinabove. The method then transitions to step 713 where another delay is allowed to expire, this one of $1/12$ the resonant time t_r . At step 715, event t_3 is performed, and main switch S1 is turned on. At this point in the method, steps 721, 723 and 725 are performed, and the voltage at the switch node is measured at step 721, and based on this measurement, the target current for switch S2, I_{s2} , used at step 705 above, is adjusted so that it will more closely match the ideal behavior in the next ZVT cycle. At step 723, if the voltage at the switch node is greater than V_{in} at the time S1 is turned on, at event t_3 , then the current target is decreased. At step 725, in contrast, if the switch node voltage at event t_3 is less than V_{in} , the target current is increased.

[0060] At step 711 the second auxiliary switch Sa2 is turned off when the current in inductor L_a is approximately equal to zero, at event t_4 as described hereinabove, which ends the ZVT portion of the power supply cycle, at step 719.

[0061] FIG. 8 illustrates a block diagram 800 of switch sequencing and timing control blocks in at least one example embodiment. As described hereinabove, the switch node voltage is monitored at the event t_3 in each buck converter cycle, this is shown in FIG. 8 in block 801. The target value (I_{s2-off}) for the current flowing through switch S2 when it is turned off in the subsequent buck converter cycle is set in block 803, as illustrated in FIG. 8. The current through S2 in each buck converter cycle is monitored by block 805, and this value is compared by comparator 807 to the I_{s2-off} target value set in the previous buck converter cycle, and when the two values are approximately equivalent, S2 is turned off (event t_1). As described hereinabove and illustrated in FIG. 7, the switch S2 turn off is followed by a fixed delay of $1/6 t_r$,

implemented in block 809, after which event t2 occurs turning off Sa1, and then turning on Sa2 after a short deadtime delay. Event t2 is followed by a fixed delay of $1/12 t_r$ implemented in block 811, after which S1 is turned on at event t3.

[0062] Both FIG. 7 and FIG. 8 are illustrating only the modified aspects of switch sequencing and timing control for the ZVT part of the power converter cycle and do not illustrate the sequencing and timing control for the entire ZVT function or for the remaining operations of the converter.

[0063] FIG. 9 depicts in another block diagram an integrated circuit 900 that provides a ZVT power converter in a buck circuit topology that incorporates example embodiments. In the integrated circuit 900, the conventional buck converter of FIG. 1 is again shown, with an input voltage V_{in} , a pair of primary switches S1, S2, which with the output inductor L_o , capacitor C_o , and resistance R_o , provide a voltage V_{out} to a load (not shown) coupled to the output. To provide the zero voltage transition function for the converter, auxiliary switches Sa1 and Sa2, and inductor L_a , are used to control the voltage at the source terminal of switch S1 and to allow it to be turned on when the source-drain voltage is approximately zero.

[0064] In FIG. 9, a controller 901 provides the gate control voltages V_{g1} , V_{g2} to the primary switches S1, S2 and also the gate voltages V_{ga1} , V_{ga2} , to the auxiliary switches Sa1, Sa2. Controller 901 implements the switching sequences needed to operate the buck converter on integrated circuit 900 including the delayed turn off of the auxiliary switch Sa1, and the delayed turn on of switch S1 after that event, that are used in example embodiments to improve the performance of the ZVT converter. Controller 901 also controls the gate voltages for other portions of the converter operating cycle to regulate the output voltage. The inputs to controller 901 include the output voltage, V_o , the switch node voltage, V_{SN} , and the current I_{s2} (or a voltage equivalent) provided by current monitor 911.

[0065] Controller 901 can be implemented in a variety of ways, such as circuits including a microcontroller, microprocessor, CPU, DSP, or other programmable logic, as a dedicated logic function such as a state machine, and can include fixed or user programmable instructions. Further, in an alternative embodiment, controller 901 can be implemented on a separate integrated circuit, with the switches S1, S2, Sa1, Sa2, and the remaining passive analog components, implemented on a stand-alone integrated circuit. Controller 901 can be implemented as an application specific integrated circuit (ASIC), such as using field

programmable gate arrays (FPGAs) or complex programmable logic devices (CPLDs). The sequencing and timing control of example embodiments can be implemented as software, firmware or hardcoded instructions. Delay lines and counters can be used to determine the needed delays $1/6 t_r$, $1/12 t_r$, as determined by a particular hardware designer. Because example embodiments are implemented as changes in the sequence of gate signals applied to the transistors of a converter, example embodiments are useful in existing converter circuits by modifying software and some sensing hardware, so example embodiments are useful to improve the performance of conventional systems without the need for entire replacements of the converter hardware.

[0066] Accordingly, example embodiments reduce energy lost during operation of the ZVT DC-DC converter function due to the auxiliary switch transitions and conduction losses in the auxiliary switches, reduce losses in the primary switch, and reduce losses in the auxiliary inductor. Also, example embodiments address an undesirable voltage spike across the secondary switch, allowing a smaller and less costly secondary switch transistor to be used.

[0067] In described examples, a zero voltage transition circuit includes an input node receiving an input voltage, an output node outputting an output voltage, a switch node, an output inductor coupled in series between the switch node and the output node, an output capacitor coupled between the output node and a ground potential, a first switch for coupling the input node to the switch node, a second switch for coupling the switch node to the ground potential, a first auxiliary switch for coupling the input node to an auxiliary node, a second auxiliary switch for coupling the auxiliary node to the ground potential, and an auxiliary inductor coupled between the auxiliary node and the switch node. An example method includes: operating the zero voltage transition circuit so that the first switch is open, the second switch is closed, the first auxiliary switch is open, and the second auxiliary switch is open; closing the first auxiliary switch to couple the input voltage to the auxiliary node and to the auxiliary inductor; subsequently, monitoring the current flowing through the second switch and when a current is below a current cutoff threshold, opening the second switch; after a first delay period, opening the first auxiliary switch and subsequently closing the second auxiliary switch; and after a second delay period, closing the first switch.

[0068] In a further example, a resonant period time t_r is determined by values of the auxiliary inductor, and by parasitic capacitances in the first switch and the second switch. In still another

example, the first delay period is approximately one-sixth t_r . In still another example, the second delay period is approximately one-twelfth t_r .

[0069] In yet another example, the first auxiliary switch is opened when the voltage at the switch node is equal to or greater than one half the voltage at the input node. In still another example, when the first switch is closed, a voltage across the first switch is approximately zero. In still another example, the cutoff current for the second switch corresponds to a current flowing in the second switch that will result in the voltage at the switch node being greater than or equal to a voltage of one-half the input voltage when the first auxiliary switch is opened.

[0070] In yet another example, the method further includes: comparing the voltage at the switch node to the voltage at the input node when the first switch is closed; and responsive to the comparing, adjusting the cutoff current threshold for the second switch.

[0071] In still another example, the method further includes: iteratively performing operating the zero voltage transition circuit so that the first switch is open, the second switch is closed, the first auxiliary switch is open, and the second auxiliary switch is open closing the first auxiliary switch to couple the input voltage to the auxiliary node and to the auxiliary inductor; subsequently monitoring the current flowing through the second switch and when the current is below a threshold, opening the second switch; after a first delay period, opening the first auxiliary switch and subsequently closing the second auxiliary switch; and after a second delay period, closing the first switch.

[0072] In still another example, providing the zero voltage transition circuit further includes providing transistors that implement a buck converter. In yet another example, providing the zero voltage transition circuit further includes providing MOS transistors implementing the first switch, the second switch, the first auxiliary switch, and the second auxiliary switch.

[0073] In another example, circuitry for a zero voltage transition switching converter includes: a first switch coupled between an input node for receiving an input voltage and a switch node; a second switch coupled between the switch node and a ground node for coupling to a ground potential; an output node for outputting a voltage to a load; an output inductor coupled between the switch node and the output node; an output capacitor coupled between the switch node and the ground node; an auxiliary circuit for enabling a zero voltage transition in turning on the first switch, including a first auxiliary switch coupled between the input node and an auxiliary node, a second auxiliary switch coupled between the auxiliary node and the ground node, an auxiliary

inductor coupled between the auxiliary node and the switch node; and a controller coupled to each of the first switch, the second switch, the first auxiliary switch, and the second auxiliary switch. The controller is configured to operate the zero voltage transition switching converter, such that: the first switch is open and the second switch is closed, subsequently, closing the first auxiliary switch, subsequently identifying when a current in the second switch falls below a cutoff current threshold; turning off the second switch, after a first delay period, opening the first auxiliary switch and then closing second auxiliary switch, and after a second delay period, closing the first switch.

[0074] In yet another example, the controller is further configured to monitor the voltage at the switch node when the first switch is turned off, and to adjust the cutoff current threshold for the second switch responsive to the monitoring.

[0075] In still a further example, a resonant time period t_r is determined by values of the auxiliary inductor, and parasitic capacitances in the first switch and the second switch.

[0076] In yet a further example, the first delay period is a time that is approximately one sixth of t_r . In another example, the second delay period is a time that is approximately one twelfth of t_r . In yet a further example, when the first auxiliary switch is turned off, the voltage at the switch node is greater than or equal to one half of the voltage at the input node. In another alternative example, the first switch, the second switch, the first auxiliary switch and the second auxiliary switch each comprise MOS transistors.

[0077] In yet another example, an integrated circuit zero voltage transition converter includes: a semiconductor substrate; a zero voltage transition converter on the semiconductor substrate further including a first switch coupled between an input node for receiving an input voltage and a switch node, a second switch coupled between the switch node and a ground node for coupling a ground potential, an output node for outputting a voltage to a load; an output inductor coupled between the switch node and the output node; and an output capacitor coupled between the switch node and the ground node; an auxiliary circuit on the semiconductor substrate configured to enable a zero voltage transition in closing the first switch, including a first auxiliary switch coupled between the input node and an auxiliary node, a second auxiliary switch coupled between the auxiliary node and the ground node, and an auxiliary inductor coupled between the auxiliary node and the switch node; and a controller on the semiconductor substrate coupled to each of the first switch, the second switch, the first auxiliary switch, and the second auxiliary

switch, configured to operate the zero voltage transition switching converter such that the first switch is open and the second switch is closed, subsequently closing the first auxiliary switch, subsequently identifying when a current in the second switch falls below a cutoff current threshold; then opening the second switch, after a first delay period, opening the first auxiliary switch and then closing second auxiliary switch, and after a second delay period, closing the first switch.

[0078] In still another example, each of the first switch, the second switch, the first auxiliary switch and the second auxiliary switch further includes a MOS transistor.

[0079] Example embodiments include zero voltage transition power converters that have reduced resonant energy losses due to improved switching sequences and timing control in the auxiliary and primary switch devices, reducing current flow in linear regions of switch operation, and reducing voltage tolerance requirements on certain ones of the switches, improving the circuit area required and increasing circuit performance.

[0080] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of operating a zero voltage transition circuit, the method comprising:
providing a zero voltage transition circuit, comprising an input node receiving an input voltage, an output node outputting an output voltage, a switch node, an output inductor coupled in series between the switch node and the output node, an output capacitor coupled between the output node and a ground potential, a first switch for coupling the input node to the switch node, a second switch for coupling the switch node to the ground potential, a first auxiliary switch for coupling the input node to an auxiliary node, a second auxiliary switch for coupling the auxiliary node to the ground potential, and an auxiliary inductor coupled between the auxiliary node and the switch node;
operating the zero voltage transition circuit so that the first switch is open, the second switch is closed, the first auxiliary switch is open, and the second auxiliary switch is open;
closing the first auxiliary switch to couple the input voltage to the auxiliary node and to the auxiliary inductor;
subsequently, monitoring the current flowing through the second switch and when a current is below a current cutoff threshold, opening the second switch;
after a first delay period, opening the first auxiliary switch and subsequently closing the second auxiliary switch; and
after a second delay period, closing the first switch.
2. The method of claim 1, wherein a resonant period time t_r is determined by values of the auxiliary inductor, and parasitic capacitances in the first switch and the second switch.
3. The method of claim 2, wherein the first delay period is approximately one-sixth t_r .
4. The method of claim 2, wherein the second delay period is approximately one-twelfth t_r .
5. The method of claim 1, wherein the first auxiliary switch is opened when the voltage at the switch node is equal to or greater than one half the voltage at the input node.
6. The method of claim 1, wherein when the first switch is closed, a voltage across the first switch is approximately zero.
7. The method of claim 1, wherein the cutoff current for the second switch corresponds to a current flowing in the second switch that will result in the voltage at the switch node being greater than or equal to a voltage of one-half the input voltage when the first auxiliary switch is

opened.

8. The method of claim 7, further comprising:

comparing the voltage at the switch node to the voltage at the input node when the first switch is closed; and

responsive to the comparing, adjusting the cutoff current threshold for the second switch.

9. The method of claim 8, further comprising iteratively performing steps of:

operating the zero voltage transition circuit so that the first switch is open, the second switch is closed, the first auxiliary switch is open, and the second auxiliary switch is open;

closing the first auxiliary switch to couple the input voltage to the auxiliary node and to the auxiliary inductor;

subsequently monitoring the current flowing through the second switch and when the current is below a threshold, opening the second switch;

after a first delay period, opening the first auxiliary switch and subsequently closing the second auxiliary switch; and

after a second delay period, closing the first switch.

10. The method of claim 1, wherein providing the zero voltage transition circuit further comprises providing transistors that implement a buck converter.

11. The method of claim 1, wherein providing the zero voltage transition circuit further comprises providing MOS transistors implementing the first switch, the second switch, the first auxiliary switch, and the second auxiliary switch.

12. Circuitry for a zero voltage transition switching converter, comprising:

a first switch coupled between an input node for receiving an input voltage and a switch node;

a second switch coupled between the switch node and a ground node for coupling to a ground potential;

an output node for outputting a voltage to a load;

an output inductor coupled between the switch node and the output node;

an output capacitor coupled between the switch node and the ground node;

an auxiliary circuit for enabling a zero voltage transition in turning on the first switch, comprising a first auxiliary switch coupled between the input node and an auxiliary node, a second auxiliary switch coupled between the auxiliary node and the ground node, an auxiliary

inductor coupled between the auxiliary node and the switch node; and

a controller coupled to each of the first switch, the second switch, the first auxiliary switch, and the second auxiliary switch, the controller configured to operate the zero voltage transition switching converter such that the first switch is open and the second switch is closed, subsequently, closing the first auxiliary switch, subsequently identifying when a current in the second switch falls below a cutoff current threshold; turning off the second switch, after a first delay period, opening the first auxiliary switch and then closing second auxiliary switch, and after a second delay period, closing the first switch.

13. The zero voltage transition converter of claim 12, wherein the controller is further configured to monitor the voltage at the switch node when the first switch is turned off, and to adjust the cutoff current threshold for the second switch responsive to the monitoring.

14. The zero voltage transition converter of claim 12 wherein a resonant time period t_r is determined by values of auxiliary inductor, and parasitic capacitances in the first switch and the second switch.

15. The zero voltage transition converter of claim 13, wherein the first delay period is a time that is approximately one sixth of t_r .

16. The zero voltage transition converter of claim 15, wherein the second delay period is a time that is approximately one twelfth of t_r .

17. The zero voltage transition converter of claim 12, wherein when the first auxiliary switch is turned off, the voltage at the switch node is greater than or equal to one half of the voltage at the input node.

18. The zero voltage transition converter of claim 12, wherein the first switch, the second switch, the first auxiliary switch and the second auxiliary switch each comprise MOS transistors.

19. An integrated circuit zero voltage transition converter, comprising:

a semiconductor substrate;

a zero voltage transition converter on the semiconductor substrate further comprising a first switch coupled between an input node for receiving an input voltage and a switch node, a second switch coupled between the switch node and a ground node for coupling a ground potential, an output node for outputting a voltage to a load; an output inductor coupled between the switch node and the output node; and an output capacitor coupled between the switch node and the ground node;

an auxiliary circuit on the semiconductor substrate configured to enable a zero voltage transition in closing the first switch, comprising a first auxiliary switch coupled between the input node and an auxiliary node, a second auxiliary switch coupled between the auxiliary node and the ground node, and an auxiliary inductor coupled between the auxiliary node and the switch node; and

a controller on the semiconductor substrate coupled to each of the first switch, the second switch, the first auxiliary switch, and the second auxiliary switch, configured to operate the zero voltage transition switching converter such that the first switch is open and the second switch is closed, subsequently closing the first auxiliary switch, subsequently identifying when a current in the second switch falls below a cutoff current threshold; then opening the second switch, after a first delay period, opening the first auxiliary switch and then closing second auxiliary switch, and after a second delay period, closing the first switch.

20. The integrated circuit of claim 19, wherein each of the first switch, the second switch, the first auxiliary switch and the second auxiliary switch further comprises a MOS transistor.

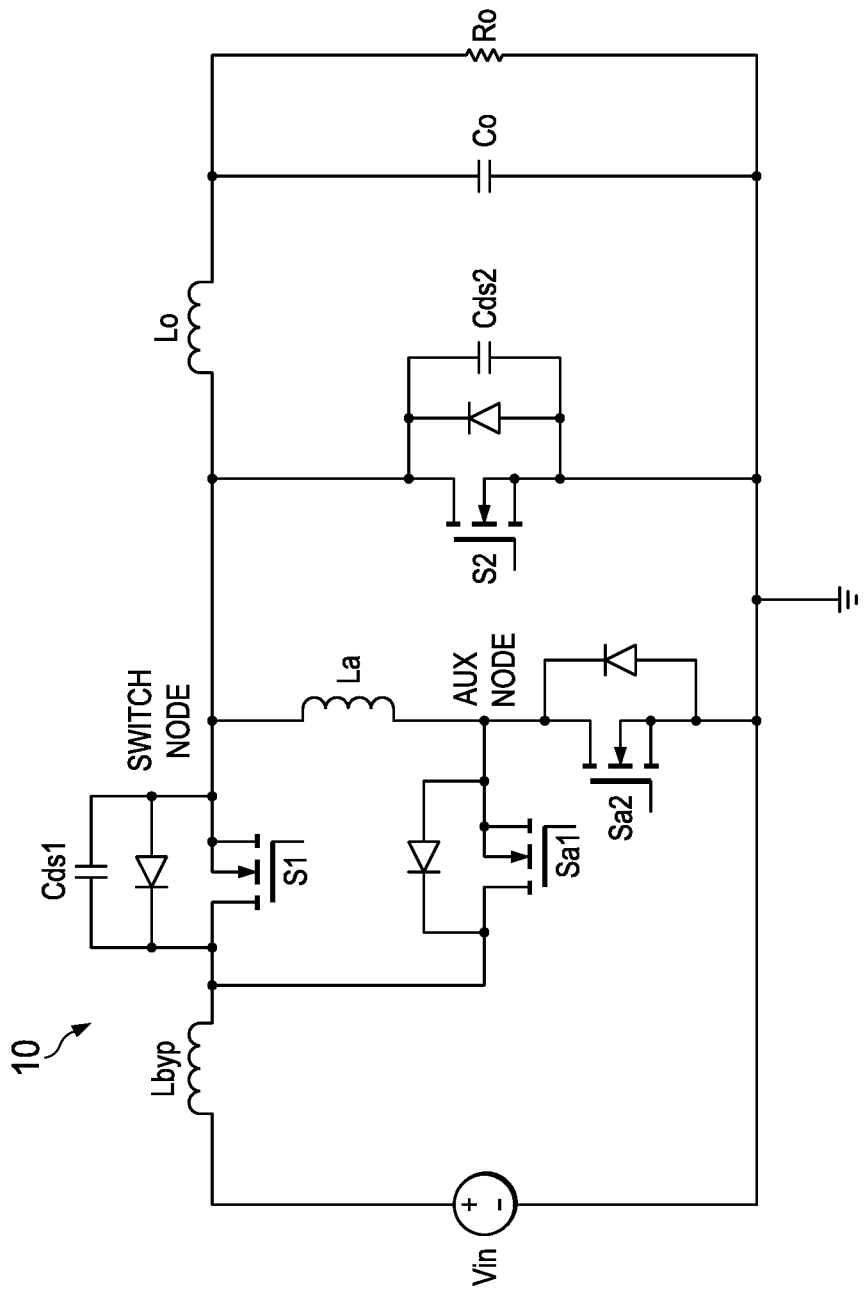


FIG. 1

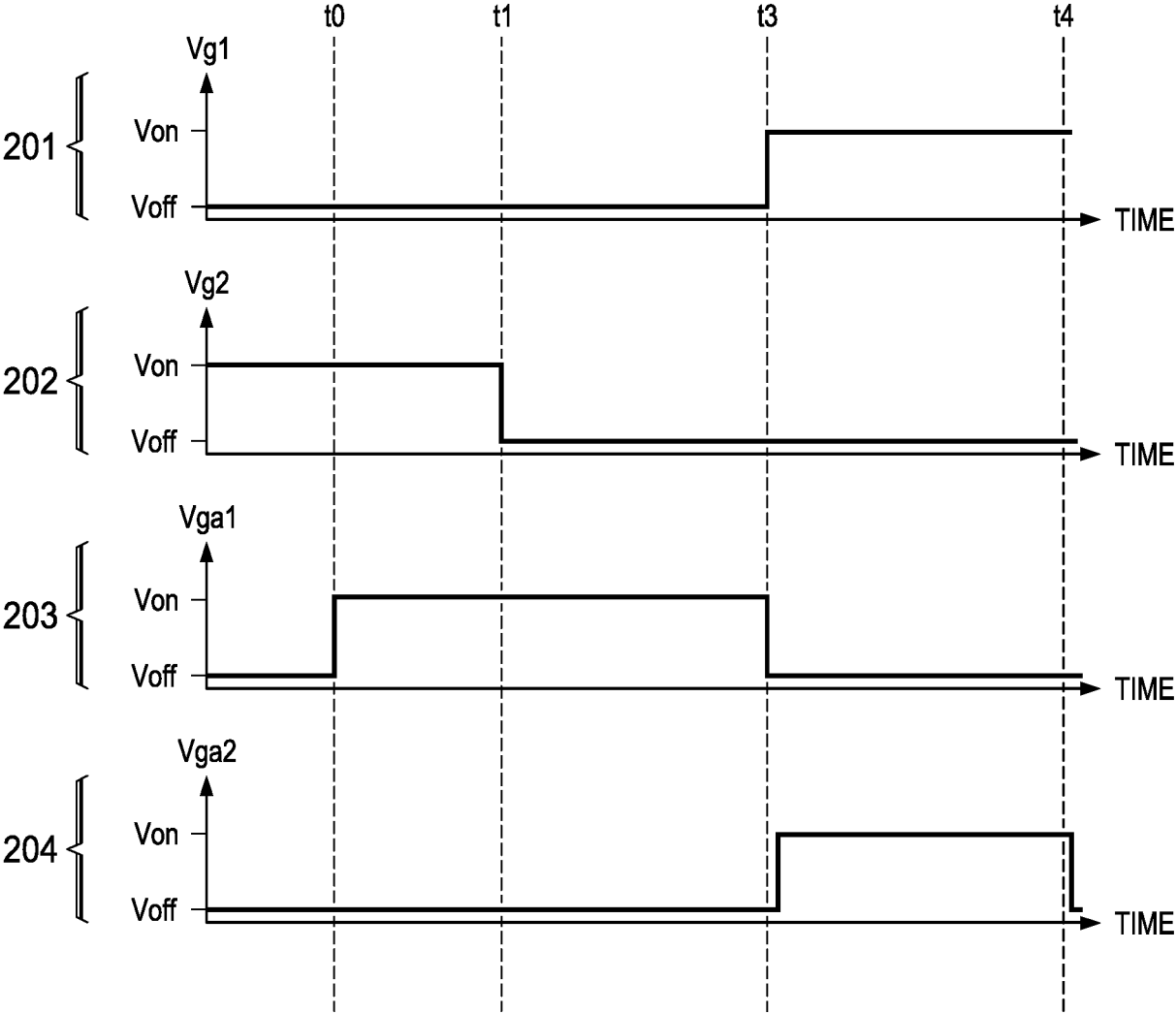


FIG. 2

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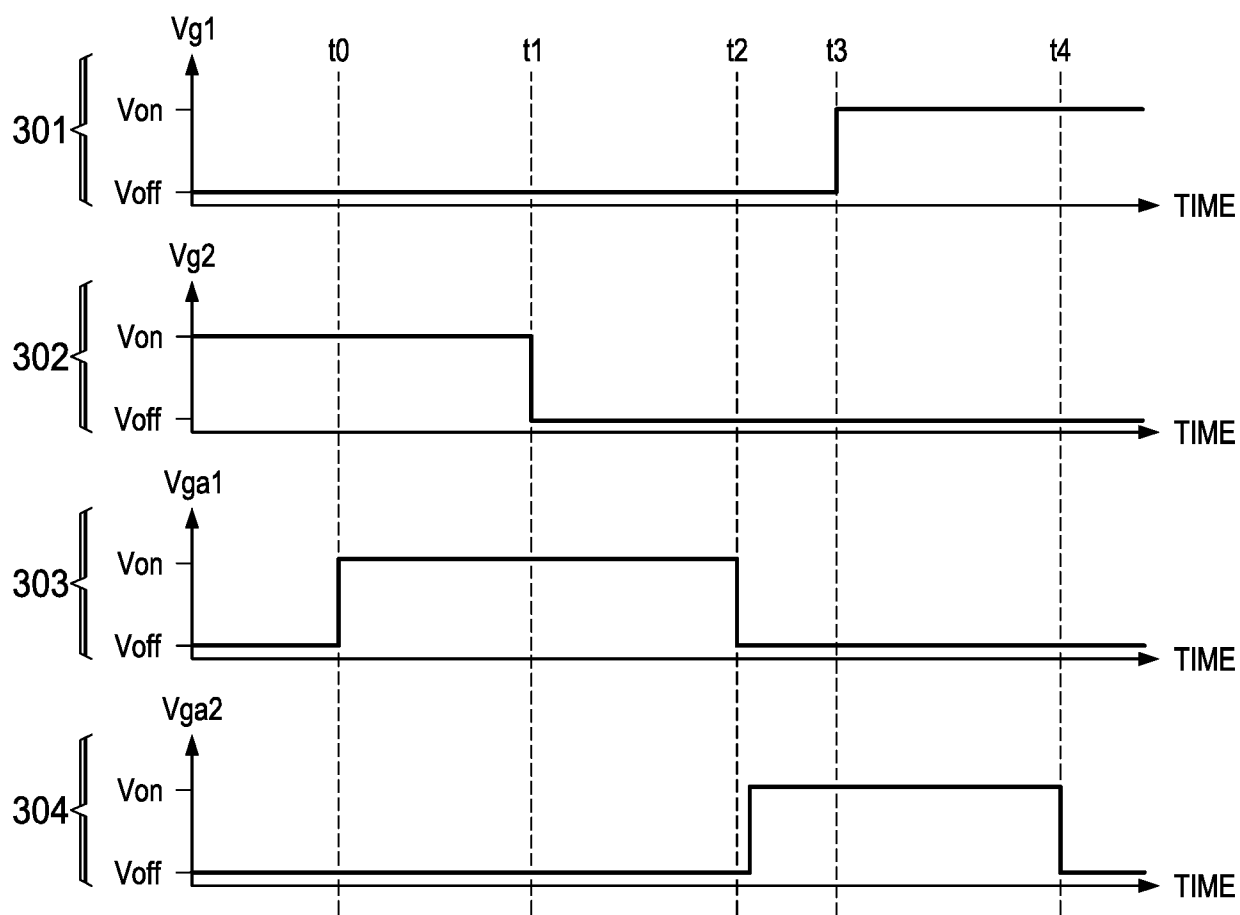


FIG. 3

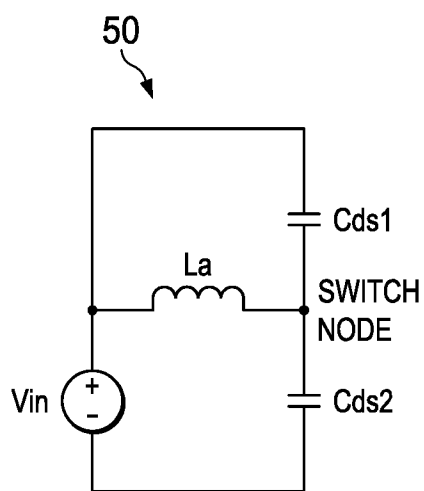


FIG. 5

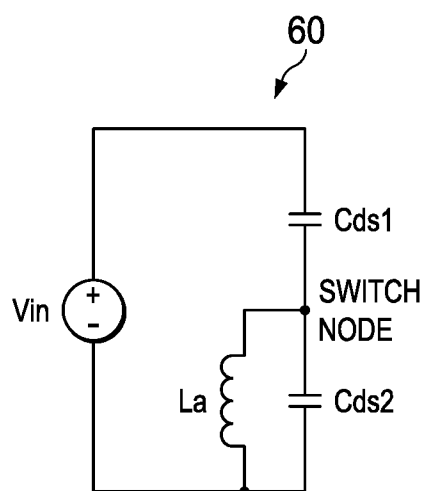
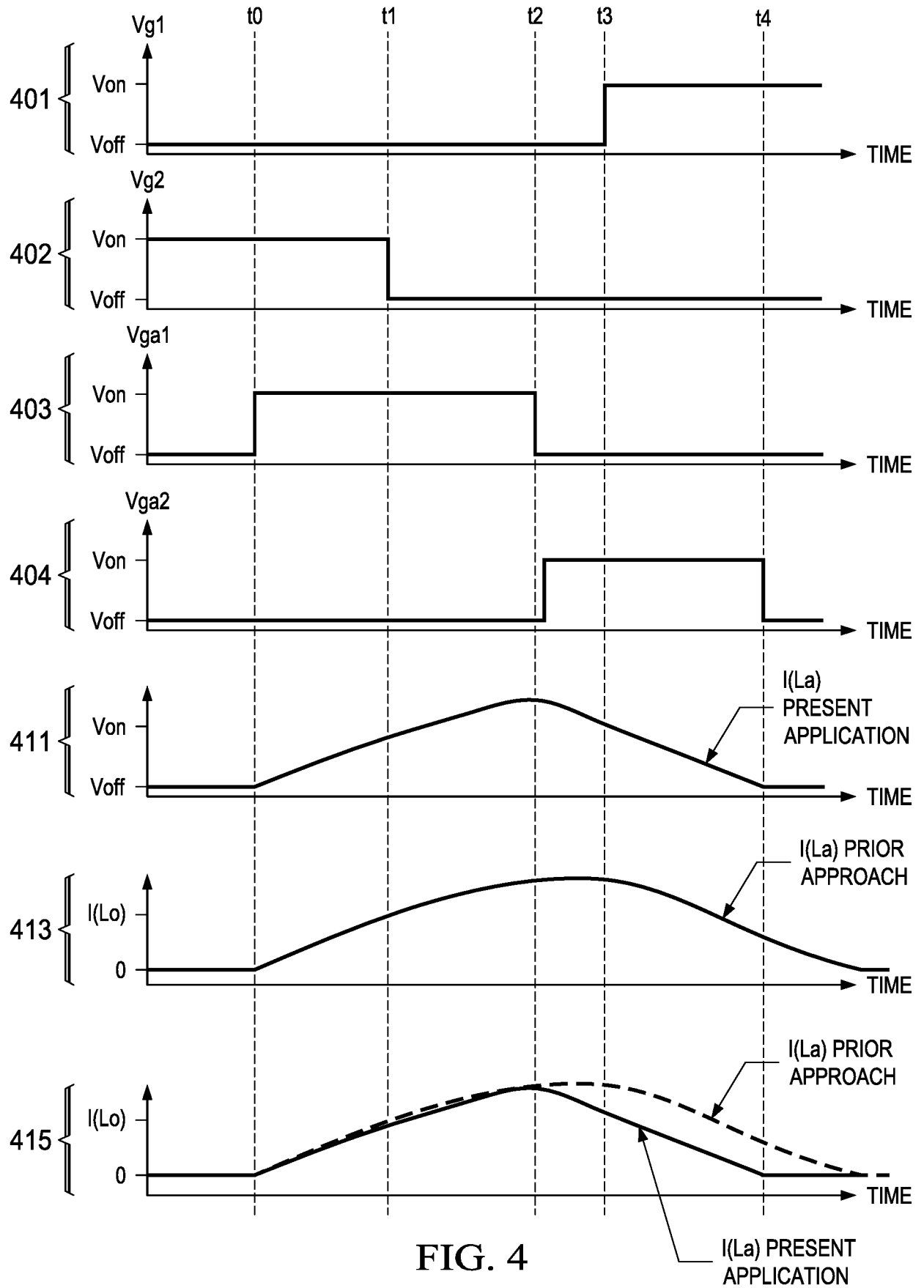


FIG. 6

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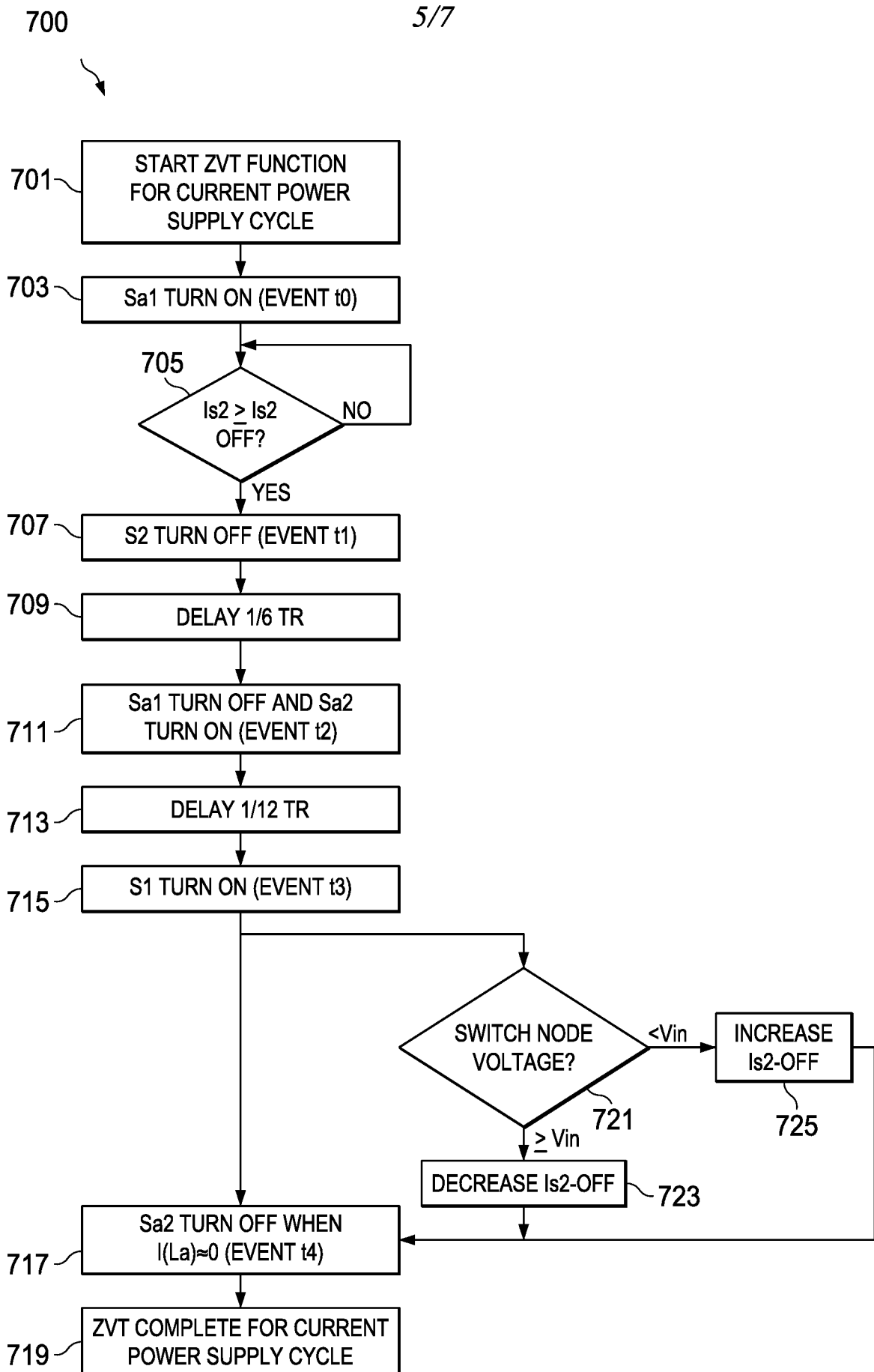


FIG. 7

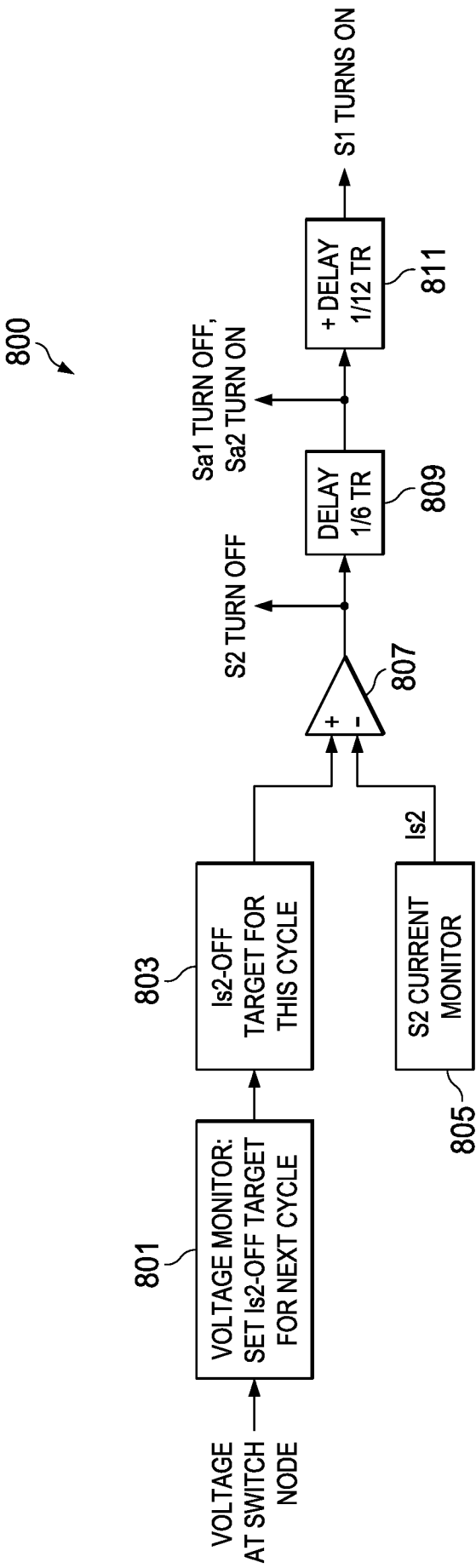


FIG. 8

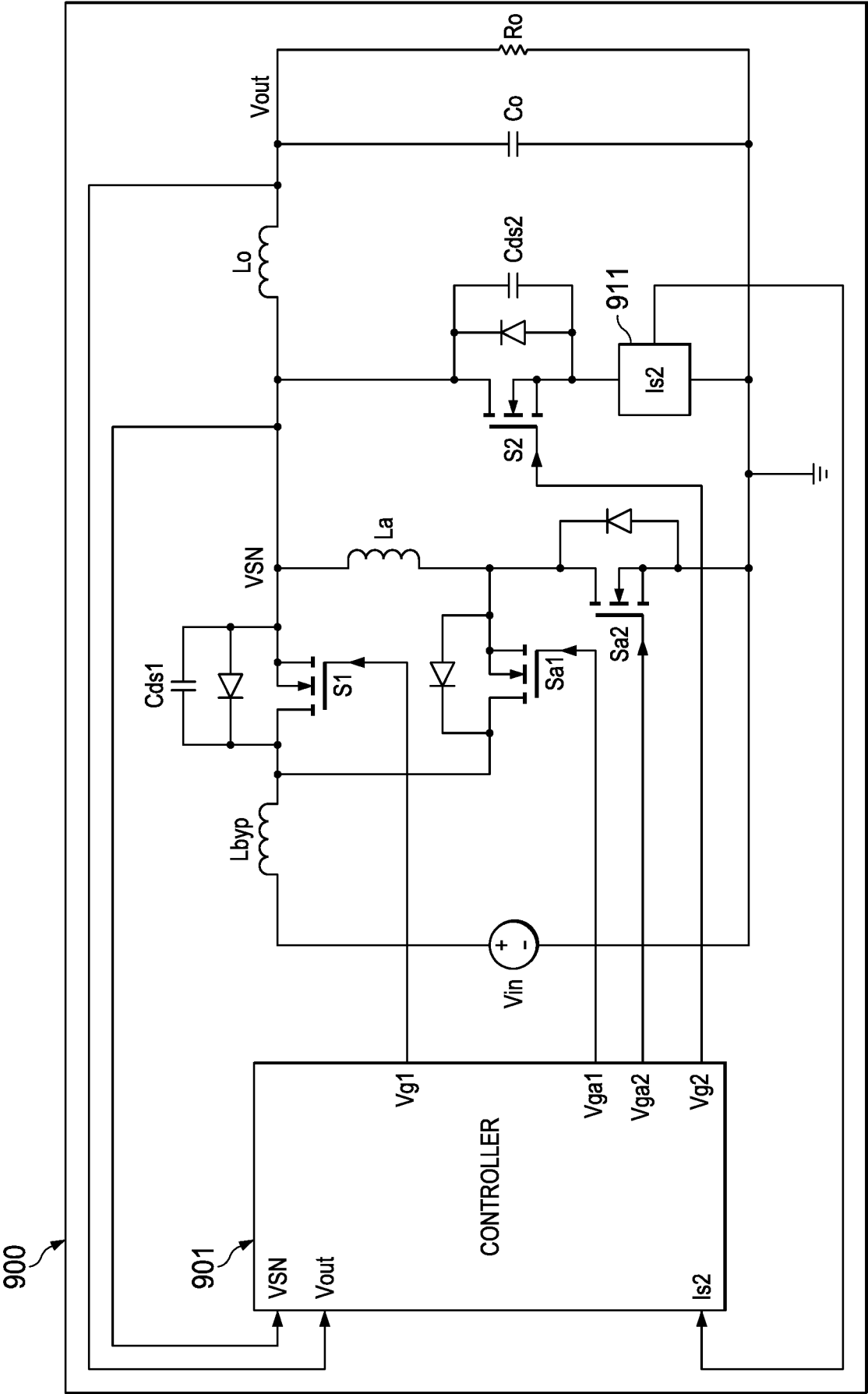


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/069149

A. CLASSIFICATION OF SUBJECT MATTER

H02M 3/156 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 3/145-3/156

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 104201884 A (BEIJING HANTIAN XINFENG MECHANICAL EQUIPMENT CO LTD) 10.12.2014	1-20
A	JPH 7123707 A (SUN EH ELECTRIC CO) 12.05.1995	1-20
A	US 6462963 B1 (TECHNICAL WITTS, INC) 08.10.2002	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

18 May 2017 (18.05.2017)

Date of mailing of the international search report

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