May 10, 1966 N. A. BOLTON ETAL 3,251,030

TRAFFIC SIGNAL CONTROLLER

Filed May 24, 1963 3 Sheets-Sheet 1

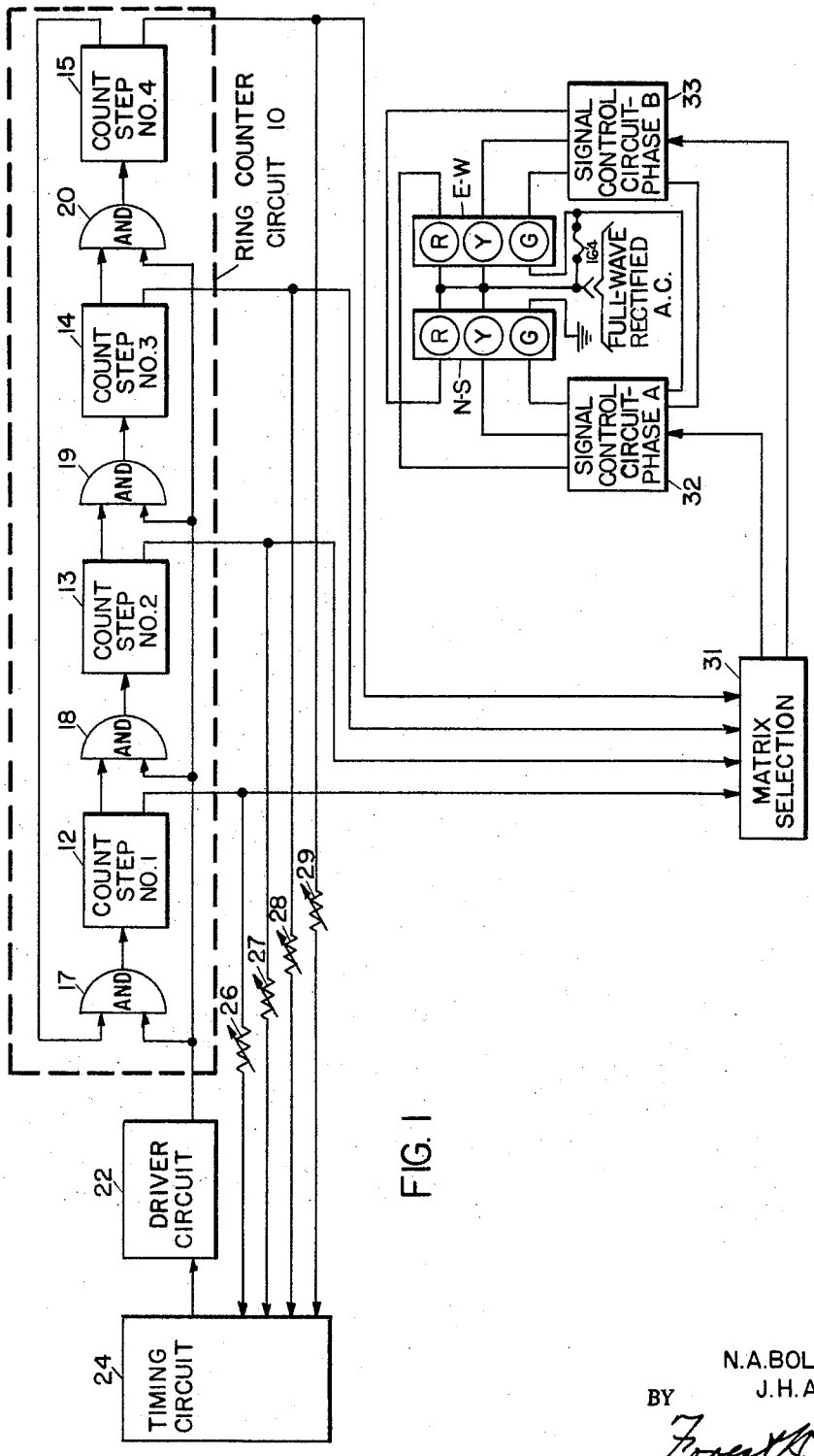


FIG. 1

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3 Sheets-Sheet 2

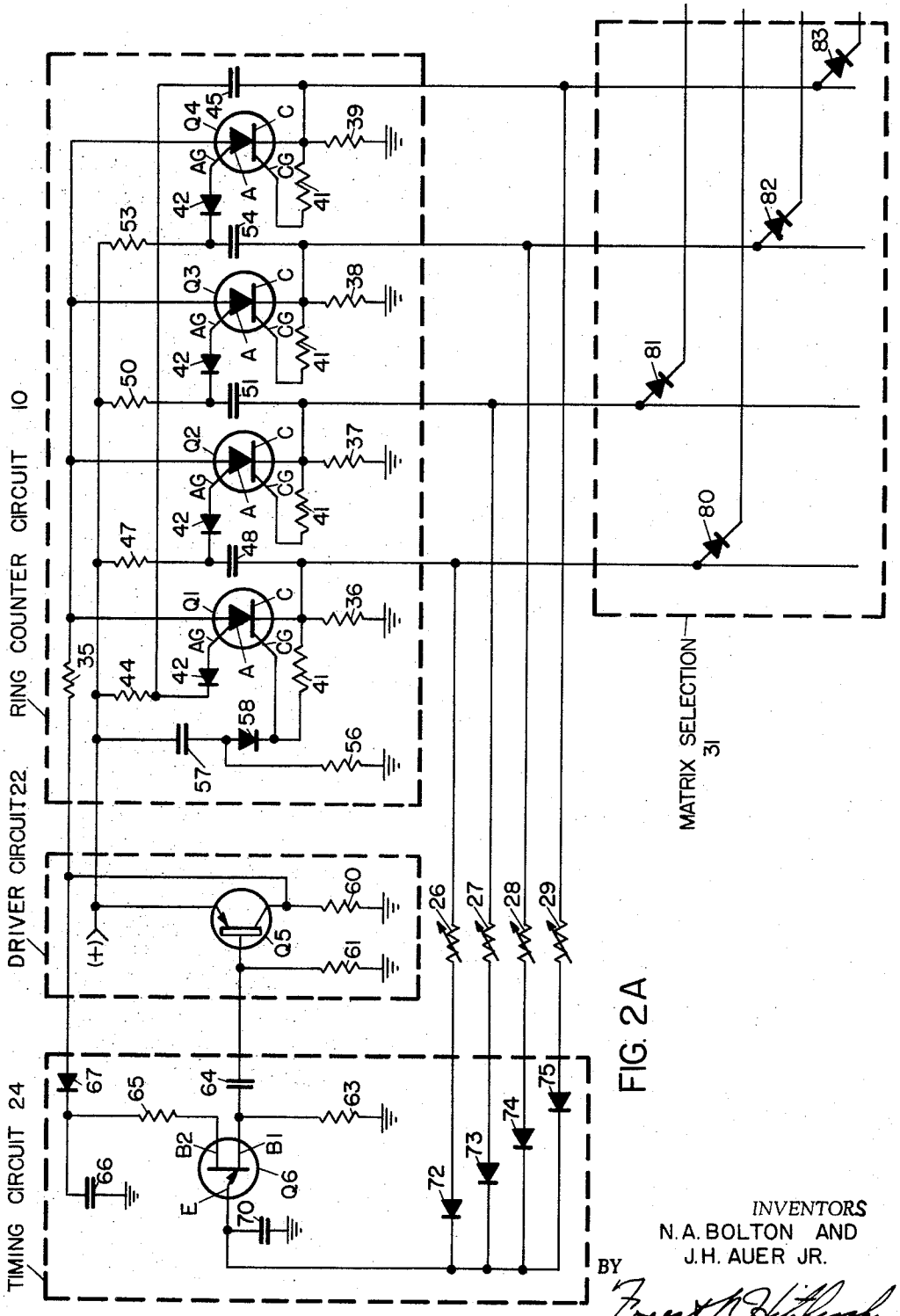


FIG. 2A

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TRAFFIC SIGNAL CONTROLLER

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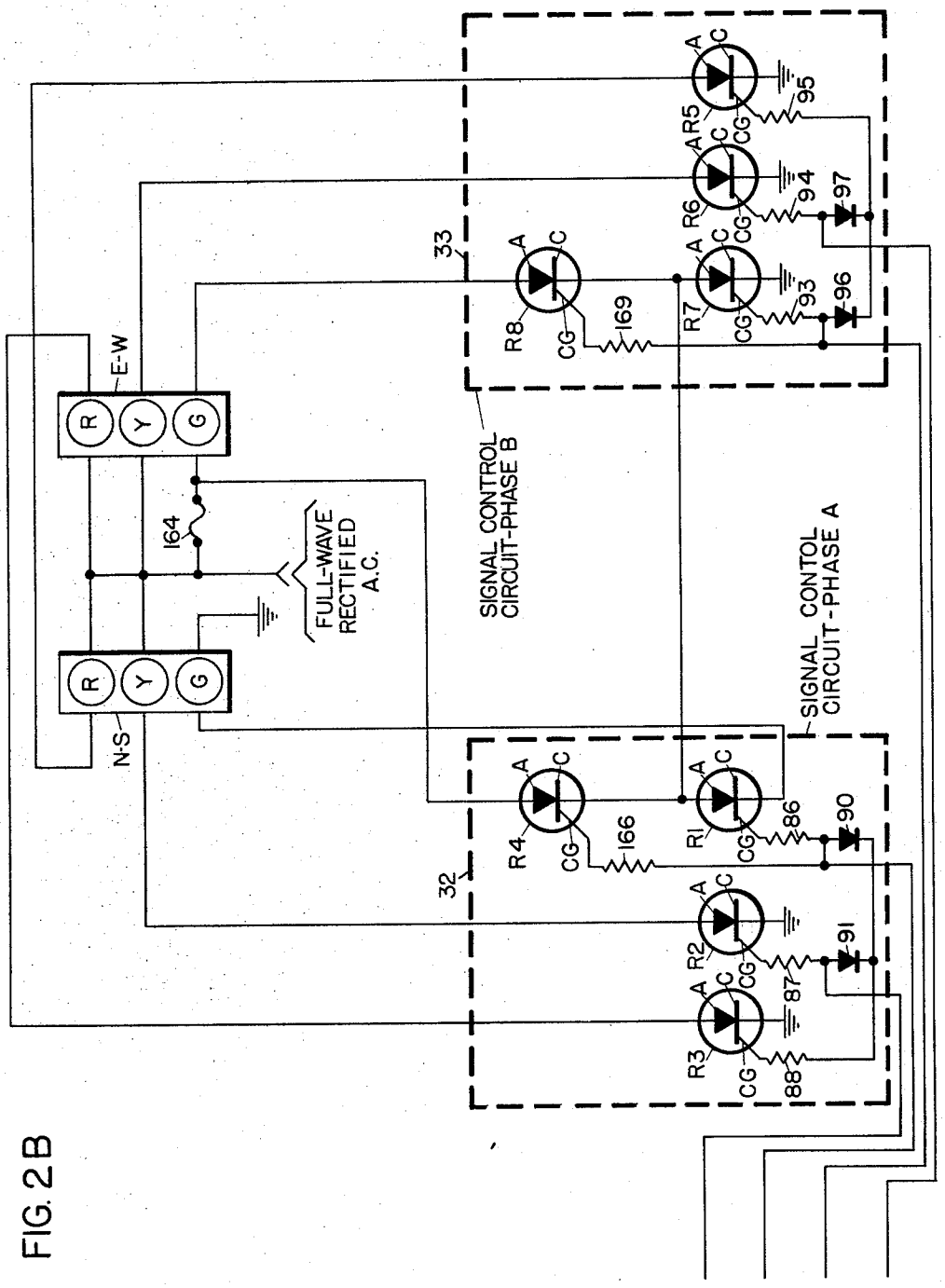


FIG. 2B

United States Patent Office 3,251,030 Patented May 10, 1966

3,251,030

TRAFFIC SIGNAL CONTROLLER

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Filed May 24, 1963, Ser. No. 283,105
9 Claims. (Cl. 340—41)

This invention relates to a highway traffic signal controller, and, more particularly, pertains to an electronic controller in which the operating characteristics can be readily varied electronically for the diverse operating conditions encountered in regulation of highway traffic.

In the cyclic operation of conventional traffic signals at an intersection, it is common practice to have a plurality of toothed disks or cams rotated simultaneously for operation of contacts for controlling the traffic signals. If it is desired to change the cycle length or the different time periods thereof, actual rearrangement of the disks or cams is required and in some cases new disks or cams must be supplied. In any event, the moving parts may become worn or misplaced over protracted periods of time. Also, mechanical failure may occur due to frost, rust, dirt or lack of lubrication.

It is contemplated by the present invention to provide an all-electronic traffic signal controller which is effective to overcome the limitations mentioned above. More specifically, it is proposed to provide selective electronic timing for each of the different time periods of an operating cycle. In addition, the cycle length may be varied by the adjustment of one or more time periods for respective traffic signals for conflicting routes at an intersection to meet the requirements of a given operating condition. Conversely, the cycle length can be maintained although the different time periods may be so varied to meet the particular operating conditions.

In the proposed embodiment, the cycle length timing means includes electronic stepping means which is operated through successive steps, each of which may have its duration selected by a timing circuit including a variable resistor operable to different resistance values. At the termination of a step period, the timing circuit becomes effective to advance said stepping means to its next step wherein a different variable resistor is used in its timing circuit.

The traffic signals at the intersection are controlled by electronic devices which are rendered effective for intervals demarcated by the electronic stepping means. Thus, throughout each interval, the green or amber signal for one phase of traffic movement and the red signal for an opposite phase of traffic movement are energized. The electronic devices employed with the green signal for the different phases of traffic movement are so organized that a malfunction of any of these devices renders the green signals for all phases of traffic movement ineffective.

For illustrative purposes, it will be assumed that a conventional lamp-type traffic signal having standard red, amber and green aspects which, when energized, respectively display STOP, SIGNAL CHANGE and GO instructions to traffic, is operated at a two-phase intersection; that is, at an intersection of two streets or highways. The traffic signals at the intersection are controlled by electronic devices rendered effective for intervals controlled by the electronic stepping means. Thus, throughout each interval, the green or amber signal for one phase of traffic movement and the red signal for the opposite phase of traffic movement are energized. The electronic devices employed with the green signal for each phase of traffic movement are so organized that a malfunction of any of these devices associated with a given phase of traffic movement renders the green signal for at least that phase of traffic movement ineffective.

Thus, one object of this invention is to provide a traffic signal controller wherein the aspect interval for each phase of traffic movement at an intersection is independently variable electronically.

Another object of this invention is to provide a traffic signal controller in which the cycle length for all phases of traffic movement at an intersection is adjustable to meet the requirements of a plurality of diverse operating conditions.

Another object of this invention is to provide a traffic signal controller including electronic means operable stepwise through a plurality of conditions where the duration of each condition is electronically variable.

Another object is to provide a traffic signal controller operable through a plurality of steps demarcated by a ring counter for each of a corresponding plurality of conditions wherein the duration of each step is independently controlled by a common timing capacitor.

Another object of this invention is to provide an electronic traffic signal controller which is readily varied electronically for each of a plurality of diverse operating conditions without the use of moving parts.

Other objects, purposes and characteristic features of this invention will be in part obvious from the accompanying drawings and will in part be pointed out as the description of the invention progresses.

To simplify the illustration, the various parts and circuits constituting the embodiment of the invention are shown diagrammatically and in block form. The symbol (+) and the symbol for a ground indicate connections made to the positive and negative terminals respectively of a source of suitable voltage such as a battery of rectified A.C. for the operation of the various electronic devices employed herein. Where rectified A.C. is required, a legend designates such a source.

In describing the invention in detail, reference will be made to the accompanying drawings in which like reference characters indicate corresponding parts in the several views, and in which:

FIG. 1 illustrates in block diagram form one embodiment of this invention; and

FIGS. 2A and 2B illustrate diagrammatically one possible circuit for this invention.

Referring now to FIG. 1, conventional green, red and amber signals indicated respectively as G, R, and Y are shown for each of a north-south direction and an east-west direction as may be employed at a given intersection. The north-south direction may be referred to as phase A, while the east-west direction may be referred to as phase B.

In the present invention, it is contemplated that the intersection at which the traffic signals are employed may be any one of a plurality of intersections subject to diverse operating conditions of the traffic signals. Irrespective of the different time periods desired for the traffic signals of phase A and phase B, the apparatus comprising the present invention may be readily adjusted electronically to fulfill the desired operating conditions of such traffic signals.

The traffic signals for both phase A and phase B are controlled during a traffic cycle period according to the outputs derived from electronic steppings means, such as a ring counter circuit **10**. More specifically, circuit **10** includes count step stages Nos. 1, 2, 3 and 4 designated respectively **12**, **13**, **14** and **15**. The count step stages **12–15** are operated in sequence to each provide an output which is employed for operating given traffic signals for phase A and phase B. In the present embodiment, the output from step stage **12** functions to operate the green signal for phase A, while the output from count step stage **13** operates the amber signal also for phase

A, both outputs from stages 12 and 13 in sequence being operative to control the red signal of phase B. Similarly, the output from step stage 14 operates the green signal of phase B, while the output from count step stage 15 operates the amber signal of phase B, both outputs from stages 14 and 15 in sequence functioning to operate the red signal of phase A.

Each of the count step stages 12–15 has included therewith an AND gate respectively designated 17, 18, 19 and 20 which functions individually to initiate the stepping between adjacent counting stages. One of the two inputs to each of the AND gates 17–20 is supplied by the previous count step stage such as, for example, the input supplied to AND gate 18 from count step stage 12. The second of the two inputs to each of the AND gates 17–20 is supplied thereto from a driver circuit 22. The driver circuit 22 is operated to provide an output which is applied to each of the AND gates 17–20 at a specific time as governed by the operation of a timing circuit 24. The absence of an output from driver circuit 22 prevents any of the AND gates 17–20 from having its two inputs fulfilled; therefore, the ring counter circuit 10 remains with its last-operated stage in the active condition. However, when driver circuit 22 receives an input from timing circuit 24, a pulse is supplied to each of the AND gates 17–20 simultaneously. The particular one of these AND gates that is then receiving an input from the then-operated stage of the ring counter, will have both its inputs fulfilled so that an output will be derived from such AND gate that will operate the succeeding stage of the ring counter to its active condition, at the same time restoring the previous stage to its normal or inactive state.

Timing circuit 24 functions to provide output signals at spaced intervals selected by a control circuit including variable resistors 26, 27, 28 and 29.

Each of the variable resistors 26–29 is connected to the output of one of the count step stages 12–15 and is effective in the control circuit only when the count step stage with which it is associated is then operating. The variable resistors 26–29 control the variation in time duration between outputs of driver circuit 24 as will be described more fully hereinafter. The variable resistors 26 and 28 are associated respectively with count step stages 12 and 14 which are alloted to the green signals for phase A and phase B respectively (see FIGS. 2A and 2B) and may, for example, permit control of the intervals between outputs from circuit 24 over a range of two to sixty seconds. Similarly, the resistors 27 and 29 are associated respectively with count step stages 13 and 15 which are allotted to the amber signals of phase A and phase B respectively (see FIGS. 2A and 2B) and may permit control of the intervals between outputs from circuit 24 over a range of two to eight seconds.

The outputs from count step stages 12–15 are supplied to the matrix selection circuit 31 from which outputs are supplied to a signal control circuit 32 for phase A and a signal control circuit 33 for phase B. The outputs of circuits 32 and 33 operate the traffic signals in the manner generally described above.

Referring now to FIG. 2A, it is seen that the ring counter circuit 10 includes in each of AND gates 17–20 a solid state device generally referred to as a silicon controlled switch, such switches being designated respectively as Q1, Q2, Q3 and Q4. Each of the switches Q1–Q4 includes an anode A, a cathode C, an anode gate AG and a cathode gate CG. The anodes A for the switches Q1–Q4 are connected to (+) through a resistor 35 and the collector-to-emitter circuit of a PNP type transistor Q5. The cathodes C of the switches Q1–Q4 are connected to ground through respective resistors 36, 37, 38 and 39. The cathode C of each of the switches Q1–Q4 is further connected to its cathode gate CG through a resistor 41, each of which is provided for operating stability purposes.

The anode gate AG for each of the switches Q1–Q4 is connected through a diode 42 to its associated count step stage, these stages being designated in FIG. 1 as 12–15. Each such count step stage 12–15 includes a resistor and capacitor. Count step stage 12 includes resistor 44 and capacitor 45. Count step stage 13 includes resistor 47 and capacitor 48. Count step stage 14 includes resistor 50 and capacitor 51. Count step stage 15 includes resistor 53 and capacitor 54.

The cathode gate CG of switch Q1 is connected to a circuit including resistor 56, capacitor 57 and diode 58 which together function to apply a positive pulse to the cathode gate CG of switch Q1 upon application of energy to the circuit, causing switch Q1 to initially conduct.

Driver circuit 22 comprises a transistor Q5 having collector and base biasing resistors 60 and 61 respectively. Transistor Q5 is so biased that it is normally conducting. The function of transistor Q5 when conducting is to supply (+) energy through the transistor in series with resistor 35 to the anodes A of switches Q1–Q4. When nonconducting, transistor Q5 functions to remove the (+) energy from the anodes A of switches Q1–Q4, removing (+) energy from one input to each of AND gates 17–20.

Timing circuit 24 is comprised of a unijunction type transistor Q6 having an emitter E and bases B1 and B2. Base B1 is connected through resistor 63 to ground, and through a capacitor 64 to the base of transistor Q5 included with driver circuit 22. Base B2 is connected to a biasing circuit including resistor 65 and capacitor 66 in series. Capacitor 66 is charged through diode 67 from (+) appearing at the collector of transistor Q5 in circuit 22 whenever transistor Q5 is conducting. The diode prevents capacitor 66 from discharging to the anodes of switches Q1–Q4 whenever transistor Q5 is nonconductive.

Emitter E of transistor Q6 is connected to ground through capacitor 70 and to the cathode C of the switches Q1–Q4 respectively through variable resistors 26–29. Diodes 72, 73, 74 and 75 are serially connected with respective variable resistors 26–29 to prevent energy feedaround from capacitor 70 to ground through cathode resistors 36, 37, 38 and 39. Each circuit including one of the resistors 26–29 functions to charge the capacitor 70 at a rate depending upon the value of resistance in order to raise the potential on emitter E of transistor Q6 to a firing level for causing an output to be supplied by timing circuit 24.

Those skilled in the art will immediately recognize the value of requiring but a single capacitor for timing each separate step of the controller. Thus, capacitor 70, which for accurate and precise timing must be of a very low leakage variety, provides overall cycle length timing as well as timing of each individual step thereof, by its use in combination separately with each of resistors 26–29. Furthermore, the economy achieved by use of a single low leakage capacitor common to each step or stage of the entire circuit, instead of one for each step, is obvious.

Matrix selection 31 is a conventional diode matrix for applying the outputs supplied from circuit 10 to the proper signal control circuit 32 or 33. The diodes, designated 80, 81, 82 and 83, are respectively associated with switches Q1–Q4. It is contemplated in the present invention that other sets of traffic signals for other nearby intersections may be operated by the outputs from circuit 10 with connections being made thereto by matrix selection 31.

Referring now to FIG. 2B, signal control circuit 32 for phase A or the north-south direction of traffic movement is seen to include silicon controlled rectifiers R1, R2, R3 and R4, while signal control circuit 33 for phase B or the east-west direction of traffic movement includes silicon controlled rectifiers R5, R6, R7 and R8. Hereinafter, these silicon controlled rectifiers R1–R8 will be

referred to as rectifiers R1–R8. Each of the rectifiers R1–R8 includes an anode A, a cathode C and a cathode gate CG.

The anodes A of rectifiers R2 and R3 for circuit 32 are connected respectively through the filament of traffic signal Y for phase A and traffic signal R for phase B to full-wave rectified A.C. energy. The cathode C of each of the rectifiers R2 and R3 is connected to ground. The cathode gate CG of rectifier R2 is connected to the cathode C of switch Q2 in circuit 10 through resistor 87 and diode 81. The cathode gate CG of rectifier R3 is connected to the cathodes C of switches Q1 and Q2 through the resistor 88 and respective diodes 90 and 91 included with circuit 32 and the diodes 80 and 81 included with matrix selection circuit 31.

The anode A of rectifier R4 is connected to full-wave rectified A.C. energy through a fuse 164. The cathode C of rectifier R1 is connected through the lamp filament of traffic signal G for phase A of the north-south direction of traffic movement to ground. The cathode gates CG of rectifiers R1 and R4 are connected through respective resistors 86 and 166 to the cathode C of switch Q1 included with circuit 10. An electrical connection is made between the common connection of the anode A of rectifier R1 and cathode C of rectifier R4 and the common connection of the anode A of rectifier R7 in circuit 33 and cathode C of rectifier R8 in circuit 33.

In circuit 33, the anodes A of rectifiers R5 and R6 are connected respectively through the filaments of the traffic signal R for phase A and the traffic signal Y for phase B to full-wave rectified A.C. energy. The cathodes C of rectifiers R5, R6 and R7 are connected respectively to ground. The cathode gate CG of rectifier R6 is connected to cathode C of switch Q4 in circuit 10 through a resistor 94 and diode 83 included with circuit 31. The cathode gate CG of rectifier R5 is connected to the cathodes C of switches Q3 and Q4 through resistor 95 and respective diodes 96 and 97 included with circuit 33 and respective diodes 82 and 83 included with circuit 31.

The anode A of rectifier R8 is connected to full-wave rectified A.C. energy through the filament of the traffic signal G for phase B or the east-west direction of traffic movement and fuse 164. The cathode gates CG of rectifiers R7 and R8 are connected respectively through resistors 93 and 169 in parallel to the cathode C of switch Q3.

It is believed that the nature of the invention, its advantages and characteristic features can be best understood with further description being set forth from the standpoint of operation.

It is to be understood herein that each of the variable resistors 26–29 may be calibrated so that specific adjustments only are required for establishing a desired cycle length while also providing the durations of each portion or step thereof before energy is applied to the respective circuits. However, it is contemplated that the resistance values of one or more of the resistors 26–29 may be changed, if desired, even after energy is applied to the circuit. In any event, it will become apparent from the following description that capacitor 70 comprises a timing capacitor which is common to each stage of the ring counter.

In the following typical example of operation, let it be assumed that resistor 26 is adjusted such that it takes forty seconds for the charge on capacitor 70 to reach the firing level of transistor Q6; resistor 27 is adjusted so that it takes five seconds for the charge on capacitor 70 to reach the firing level of transistor Q6; resistor 28 is adjusted such that it takes twenty seconds for the charge on capacitor 70 to reach the firing level of transistor Q6; and resistor 29 is adjusted also that it takes three seconds for the charge on capacitor 70 to reach the firing level of transistor Q6. Each of these intervals thus delineates a separate step of the controller, as will be apparent infra.

Upon applying energy to the circuits of FIGS. 2A and 2B, capacitors 45, 48, 51 and 54 are charged by obvious circuits while the respective switches Q1–Q4 are nonconductive, but are discharged separately when the respective switch is rendered conductive. At this time, capacitor 57 begins to charge through resistor 56 eventually causing a sufficiently large positive signal to be applied through diode 58 to the cathode gate of switch Q1, driving the switch into conduction. The anode A (+) energy supply for switch Q1 is supplied through transistor Q5 which is biased to conduction.

A charging circuit is completed for capacitor 66 through diode 67 and to (+) energy through transistor Q5. The charge on capacitor 66 thus biases base B2 of transistor Q6 through resistor 65. With base B2 thus biased, application of the firing level of energy on emitter E of transistor Q6 drives the transistor into conduction, reducing the level of impedance between its emitter E and base B1.

As switch Q1 conducts, a positive-going signal is taken from the cathode C thereof and applied to capacitor 70 through resistor 26 and diode 72 for charging capacitor 70. According to the above assumption, the level of charge on capacitor 70 for firing transistor Q6 is reached approximately forty seconds after switch Q1 is rendered conductive. In addition, capacitor 48, which previously acquired a charge through resistors 47 and 36 in series, is discharged through a series circuit comprising switch Q1, resistor 35, transistor Q5 and resistor 47.

When transistor Q6 fires, capacitor 70 is discharged through transistor Q6 from emitter E to base B1, through resistor 63, to ground. The resulting voltage drop appearing across resistor 63 is coupled through capacior 64, which is initially uncharged, to the base of transistor Q5. The base of transistor Q5 is thus driven positive, cutting off the transistor for an interval determined by the time required to charge capacitor 64 to a voltage level which lowers the base voltage on transistor Q5 to the level which permits transistor Q5 to resume conduction. When transistor Q6 subsequently ceases conduction, due to the lowered voltage across capacitor 70, the charge stored on capacitor 64 leaks off through resistors 61 and 63 in series.

When transistor Q5 is driven into cutoff, positive energy for anode A of switch Q1 is interrupted, cutting off switch Q1 and thereby returning cathode C of switch Q1 to substantially ground potential. Capacitor 48 thus begins to acquire a charge, and the capacitor charging current which flows through resistor 47 drives the cathode of diode 42 in a negative direction, thus driving anode gate AG of switch Q2 negative with respect to anode A of switch Q2. Transistor Q5 resumes conduction while capacitor 48 is still being charged, due to the short RC time constant of resistor 61 and capacitor 64, and switch Q2 is accordingly driven into conduction. However, switch Q1 remains non-conductive, since capacitor 45 remains fully charged, preventing anode gate AG of switch Q1 from being driven negative with respect to anode A of switch Q1.

During the time interval of approximately forty seconds that switch Q1 is conducting, the positive voltage appearing on cathode C of switch Q1 is applied through diode 80 in circuit 31 to the cathode gates CG of rectifiers R1 and R4 through respective resistors 86 and 166, causing such rectifiers R1 and R4 to conduct. The green signal G for phase A, being connected in the cathode circuit of rectifier R1, is thus energized. Moreover, the positive voltage appearing on cathode C of switch Q1 is also supplied through diode 80 to the cathode gate CG of rectifier R3 through diode 90 and resistor 88, causing rectifier R3 to conduct. The red signal R for phase B, being connected, in the anode circuit of rectifier R3, is thus energized.

Rectifiers R1 and R4 continue to conduct as long as positive voltage is applied to the respective cathode gates CG. However, after a slight delay on the order of less than a millisecond following removal of the positive volt-

age, the rectifiers R1 and R4 are cut off in response to the removal of positive energy from the anode circuits thereof. This slight delay is caused by charging current flowing through capacitor 48. It will be noted that the full-wave rectified A.C. energy appears as a series of positive half-cycles where each half-cycle starts at a zero voltage level, rises to a maximum positive voltage level, and returns to a zero voltage level. It is when the zero voltage level is applied to the anode circuits in the absence of positive voltage signal which is applied to the cathode gates CG thereof that the rectifiers R1 and R4 are cut off. It is to be understood that the other rectifiers described herein operate in a similar manner.

Upon conduction of switch Q2, a positive voltage is supplied from cathode C of switch Q2 to the cathode gate CG of rectifier R2 through diode 81 and resistor 87 in series, which causes conduction of rectifier R2. This signal is applied for a time period of approximately five seconds, as determined by the setting of resistor 27. While conducting, rectifier R2 energizes signal Y for phase A, causing an amber indication to be displayed.

During the total time period of forty-five seconds, rectifier R3 remains in conduction as a consequence of positive voltages being applied to the cathode gate CG of rectifier R3 through diodes 90 and 91 in sequence. The red signal R for phase B or the east-west direction of traffic movement is thus energized during the period that the green signal G and amber signal Y for phase A are sequentially energized.

When the level of charge on capacitor 70, supplied through resistor 27, reaches the voltage sufficient to fire transistor Q6 at the end of the five second time interval, transistor Q6 is fired, again causing transistor Q5 to be cut off for a predetermined time interval. The positive energy for anode A of switch Q2 is removed, thereby cutting off switch Q2. Capacitor 51 thus begins to acquire a charge through resistor 50, driving anode gate AG of switch Q3 negative with respect to the anode of switch Q3.

Transistor Q5 resumes conduction while capacitor 51 is still being charged, due to the short RC time constant of resistor 61 and capacitor 64, and switch Q3 is accordingly rendered conductive, causing a positive voltage to appear at its cathode C. This voltage is applied to the cathode gates CG of rectifiers R7 and R8 through diode 82 of circuit 31 and respective resistors 93 and 169 for the time period of approximately twenty seconds during which switch Q3 is conductive, as determined by the setting of resistor 28. During this time period of twenty seconds, the green signal G for phase B is energized through a circuit including the rectifiers R7 and R8 in series. In addition, the positive voltage appearing on cathode C of switch Q3 is also applied through diode 82 to the cathode gate CG of rectifier R5 through diode 96 and resistor 95 in series, to cause conduction of rectifier R5. The red signal R for phase A or the north-south direction of traffic movement is energized thereby.

While switch Q3 is in conduction, capacitor 70 in timing circuit 24 acquires a charge from cathode C of switch Q3 through resistor 28 and diode 74 in series. After approximately twenty seconds from the instant switch Q3 is driven into conduction, the voltage on capacitor 70 reaches a level sufficient to fire transistor Q6, again cutting off transistor Q5 for a predetermined interval and thereby interrupting the anode voltage of switch Q3, rendering the switch non-conductive. After a brief delay, during which capacitor 54 acquires a charge, cathode C of switch Q3 returns to substantially ground potential. As capacitor 54 charges, anode gate AG of switch Q4 is driven negative with respect to the anode of switch Q4. When transistor Q5 resumes conduction, capacitor 54 is still being charged, due to the short RC time constant of resistor 61 and capacitor 64, and therefore switch Q4 is rendered conductive. Moreover, when cathode C of switch Q3 returns to substantially ground potential, the positive voltage on cathode gates CG of rectifiers R7 and R8 in circuit 33 is removed, permitting rectifiers R7 and R8 to become non-conductive by the action of the full-wave rectified A.C. energy, as previously described. The green signal G for phase B is consequently deenergized.

Upon conduction of switch Q4, a positive voltage is supplied from cathode C thereof to cathode gate CG of rectifier R6 through diode 83 in series with resistor 94, and to cathode gate CG of rectifier R5 through a series circuit comprising diodes 83 and 97 and resistor 95. Rectifiers R6 and R5 are thus rendered conductive for a period of approximately three seconds, which is the time required for the charge on capacitor 70, supplied through resistor 29, to reach the firing potential of transistor Q6. During the conducting period of rectifier R6, the phase B amber signal Y is energized, while the phase A red signal R is simultaneously energized due to conduction of rectifier R5.

Through the latter two successive intervals, which endure for a total of twenty-three seconds, rectifier R5 remains conductive, since positive voltages are supplied from the cathodes of switches Q3 and Q4 through the circuits described above to the cathode gate CG of rectifier R5. The red signal R for phase A or the north-south direction of traffic movement is thus energized throughout this interval, since its lamp filament is included in the anode circuit of rectifier R5.

The level of charge on capacitor 70 reaches the level of firing voltage for transistor Q6 in approximately three seconds from the instant at which switch Q4 begins conduction, at which time transistor Q5 is cut off for a predetermined interval in the manner described above. Positive anode voltage for switch Q4 is interrupted while transistor Q5 is cut off, causing switch Q4 to be cut off. Capacitor 45 then begins to acquire a charge through resistor 44, driving the anode gate AG of switch Q1 negative with respect to the anode of switch Q1. When transistor Q5 subsequently resumes conduction, capacitor 45 is still being charged, due to short RC time constant of resistor 61 and capacitor 64, and therefore switch Q1 is rendered conductive. Thus, upon transfer of conduction from switch Q4 to switch Q1, one cycle of controller operation is completed, while a second cycle of operation is initiated. That is, the green signal G for phase A is again energized while the red signal R for phase B is also energized.

In the energizing circuit for the phase A green signal G, there exists a possibility that either rectifier R1 or rectifier R4 may become short-circuited or open-circuited due to a malfunction. For a similar reason, in the energizing circuit for the phase B green signal G, either rectifier R7 or rectifier R8 may become short-circuited or open-circuited. The circuit arrangement shown in FIG. 2B, however, prevents any unsafe traffic condition from resulting from such malfunction, by insuring that at least one of the red signals R for phase A and phase B is energized at all times, depending upon the counting position of circuit 10. Hence, if either one of rectifiers R4 or R7 becomes short-circuited, a short circuit is completed from fuse 164 through both rectifiers in series, to ground, when the remaining rectifier is rendered conductive, blowing the fuse and thereby disconnecting the full-wave rectified A.C. energy from the green signal circuits. On the other hand, if either one of rectifiers R1 or R8 is short-circuited, the energizing circuits for both the phase A and phase B green signals G are completed when the remaining rectifier is rendered conductive by an input signal; however, the increased resistance resulting from the added lamp filament in series reduces the energizing current for the green signals G to a low value, substantially preventing illumination thereof.

If either rectifier R1 or R4 should become open-circuited, the energizing circuit for the green signal G for phase A remains disconnected even when an input signal from switch Q1 is applied to the cathode gates CG of

rectifiers R1 and R4. If either rectifier R7 or R8 opens, the energizing circuit for the green signal G for phase B remains disconnected even when an input signal from switch Q3 is applied to the cathode gates CG of rectifiers R7 and R8.

Both in the specification and the claims, reference is made to a so-called "ring counter." This terminology is intended to cover ring counters of various types, including those which use vacuum tube flip-flop stages, solid-state bistable state devices, and the like. The term is intended to apply not only to ring counters wherein each stage is directly coupled to the next, but to apply also to ring counters of the type wherein momentarily all of the stages may be restored to their normal state at some point in a complete cycle of operation, with additional circuit means being provided to detect that such a condition exists so as to immediately thereafter operate a selected stage of the ring counter to its active state. Ring counters of this latter type have been devised to ensure that not more than one stage of the counter will at any instant be in its active state, but otherwise the operation is the same as that of the more conventional ring counters in that, in effect, the active state of a stage is continually being advanced sequentially to the successive stages of the ring counter so that cyclical operation of the counter occurs.

Having described a traffic signal controller as a specific embodiment of the present invention, it should be understood that the embodiment illustrated is considered as being merely typical and that various modifications and alterations may be made to the specific form shown without departing from the spirit or scope of this invention.

What we claim is:

1. A traffic signal controller adapted to cyclically energize the lamps of traffic signals at an intersection comprising, a ring counter operable cyclically through a plurality of different step conditions, timing means common to each step condition and selectively set to independently demarcate predetermined time duration for each of said step conditions, driver means controlled by said timing means for impulsing said ring counter into a successive step condition, and control means rendered effective by said ring counter for selectively energizing particular ones of the signal lamps for each of said step conditions.

2. The traffic signal controller according to claim 1 wherein said ring counter includes a plurality of electronic devices, a separate one of said devices being operative on each step of said ring counter for providing an output continuously in the respective step.

3. The traffic signal controller according to claim 1 wherein said control means includes a plurality of separate switching devices responsive to said ring counter, each switching device being coupled to at least one traffic signal lamps at the intersection and operative to energize such lamp therein during the time period in which said ring counter is on a respective one of its said steps.

4. A traffic signal controller adapted to cyclically energize the lamps of a traffic signal at an intersection comprising, ring counter means operable through a plurality of different step conditions, a timing circuit including capacitor means and a plurality of resistors, each of said resistors being individually associated with a separate step condition and coupled to said capacitor means for independently demarcating a predetermined time duration for said step condition, driver means controlled by said timing circuit for operating said ring counter means to a successive step condition, and control means rendered effective in response to the step conditions of said ring counter means for selectively energizing said lamps in accordance with each step condition of said ring counter means.

5. The traffic signal controller of claim 4 wherein said timing circuit further includes switching means responsive to the amplitude of voltage on said capacitor means for discharging said capacitor means when said voltage reaches a predetermined amplitude.

6. In a traffic signal control system, means for cyclically operating a traffic signal through successive indications comprising, ring counter means having a plurality of stages, circuit means for advancing the count of said counter means one stage at a time sequentially at predetermined intervals, said counter means providing a distinctive output from each step as said counter is operated to such step, said circuit means being individually controlled in accordance with each separate stage when said separate stage furnishes the output of said counter means, and means coupling the output of each stage of said counter means to said traffic signal to differently control the signal indications displayed by said signal as said counter advances from stage to stage.

7. In a traffic signal control system, means for cyclically operating a traffic signal through successive indications comprising, ring counter means having a plurality of stages, charge storage means, a plurality of feedback means, each said feedback means coupling a stage of said ring counter to said charge storage means for controlling the charging rate of said charge storage means, means coupling said counter means to said traffic signal, and circuit means responsive to said charge storage means for initiating start of a new indication each time the quantity of charge on said charge storage means reaches a predetermined amount.

8. A control circuit for operating a conventional two-phase traffic signal having at least red and green aspects in response to at least a pair of sources of sequentially-occurring voltages, said circuit having interlocking means to prevent simultaneous display of green signals to both directions of traffic in the event of either open-circuit or short-circuit failure of components in said circuit, said circuit comprising, an overcurrent-responsive device, first and second controlled rectifiers connected in series-aiding with said first-phase green signal and said overcurrent-responsive device, third and fourth controlled rectifiers connected in series-aiding with said second phase green signal and said overcurrent-responsive device, means connecting the junction common to the first and second rectifiers with the junction common to the third and fourth rectifiers, said first and fourth rectifiers thereby being connected in series-aiding and said second and third rectifiers thereby being connected in series-aiding, circuit means coupling one of said sources to the second phase red signal and the control electrodes of said first and second controlled rectifiers, and circuit means coupling the other of said sources to the first phase red signal and the control electrodes of said third and fourth controlled rectifiers.

9. A traffic signal controller for controlling the indications displayed by the lamps of traffic signals at a street intersection comprising, an electronic ring-type counting means having a plurality of steps each being operable from a normal state to an active state, means responsive to discrete input signals for operating all said steps of said ring-counting means to their active state one at a time sequentially, timing circuit means for generating said discrete input signals, said timing circuit means including a plurality of individually adjustable timing elements each selected one at a time by a corresponding step of said ring-counting means when in its active state for controlling the time of occurrence of the next of said discrete input signals relative to the last-occurring of such input signals, means coupling each signal lamp of said traffic signal to a corresponding one of the steps of said ring-counting means for selectively controlling the illumination of said lamps in dependence upon the particular step of said ring-counting means which is at any instant in its active state, said ring-counting means operating through a complete cycle wherein all its steps

are sequentially operated to their active states for each signal cycle of indications displayed by said traffic signals.

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