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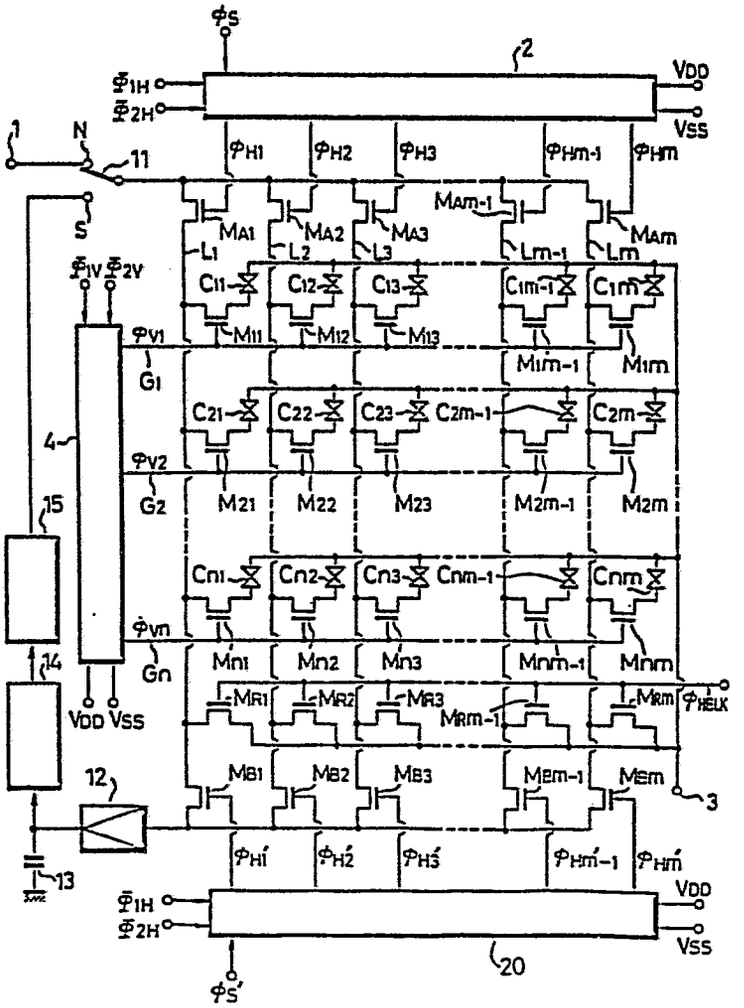
(54) **LIQUID CRYSTAL DISPLAY DEVICE.**

(57) A liquid crystal display device which is capable of displaying a still picture, wherein column lines (L_1) to (L_m) served with image signals are provided with second horizontal switching elements (M_{B1}) to (M_{Bm}) that are driven by phases ($\varnothing H'_1$) to ($\varnothing H'_m$) which are just before the phases of picture switching signals ($\varnothing H_1$) to ($\varnothing H_m$), a switch (11) is connected to a contact point (S) of the still picture display side, image signals stored in the liquid crystal cells C are taken out through the second horizontal switching elements (M_{B1}) to (M_{Bm}) and are fed back to an input terminal (1) through an inverter circuit (14) and a normalizing circuit (15), provision is made of third switching elements (M_{R1}) to (M_{Rm}) that are turned on after every horizontal flyback period, the signals taken out from the liquid crystal cells C are inverted and are returned to the same liquid crystal cells C, and the potentials of the signal lines are reset after every horizontal flyback period. Therefore, the picture quality is not deteriorated by residual electric charge, and a still picture is displayed in favorable condition for extended periods of time.

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Croydon Printing Company Ltd.

FIG. 1


φS
2
VDD
Φ1H
Φ2H
VSS
1
N
11
φH1
φH2
φH3
φHm-1
φHm
S
MA1
MA2
MA3
MAm-1
MAm
L1
L2
L3
Lm-1
Lm
Φ1V
Φ2V
C11
C12
C13
C1m-1
C1m
M11
M12
M13
M1m-1
M1m
φV1
G1
C21
C22
C23
C2m-1
C2m
4
φV2
G2
M21
M22
M23
M2m-1
M2m
15
Cn1
Cn2
Cn3
Cnm-1
Cnm
φVn
Mn1
Mn2
Mn3
Mnm-1
Mnm
14
Gn
MR1
MR2
MR3
MRm-1
MRm
φHELK
VDD
VSS
MB1
MB2
MB3
MBm-1
MBm
12
3
φH1'
φH2'
φH3'
φHm'-1
φHm'
13
Φ1H
Φ2H
VDD
VSS
20
φS'

0192784

DESCRIPTION

TITLE OF THE INVENTION

LIQUID CRYSTAL DISPLAY APPARATUS

TECHNICAL FIELD

The present invention relates to a liquid crystal display apparatus used to carry out the display of a still picture.

BACKGROUND ART

It is proposed to display a television picture by using, for example, a liquid crystal.

In Fig. 6, reference numeral 1 designates an input terminal to which a television video signal is supplied. The signal from this input terminal 1 is supplied through switching elements M_1, M_2, ... M_m, each of which is formed of, for example, an N-channel FET, to lines L_1, L_2, ... L_m in the vertical (Y axis) direction where m is the number corresponding to the number of picture elements in the horizontal (X axis) direction. Further, there is provided a shift register 2 having m stages. This shift register 2 is supplied with clock signals Φ_{1H}, Φ_{2H} each having a frequency m times the horizontal frequency. Picture element switching signals Φ_{H1}, Φ_{H2}, ... Φ_{Hm}, which are derived from the respective output terminals of this shift register 2 and sequentially scanned by the clock signals Φ_{1H}, Φ_{2H} are supplied to the respective control terminals of the switching elements M_1 to M_m. To the shift register 2, there are supplied a low potential (V_{SS}) and a high potential (V_{DD}) and thereby drive pulses of the two potentials are generated.

To the respective lines L_1 to L_m, there are connected

one ends of switching elements M_{11}, M_{21}, ... M_{n1}, M_{12}, M_{22}, ... M_{n2}, ... M_{1m}, M_{2m}, ... M_{nm}, which are each formed of, for example, an N-channel FET, where n is the number corresponding to the number of the horizontal scanning lines. The other ends of these switching elements M_{11} to M_{nm} are respectively connected through liquid crystal cells C_{11}, C_{21}, ... C_{nm} to a target terminal 3.

Further, there is provided a shift register 4 having n stages. This shift register 4 is supplied with clock signals Φ_{1V} and Φ_{2V} each having a horizontal frequency. Scanning line switching signals ϕ_{V1}, ϕ_{V2}, ... ϕ_{Vn}, which are derived from the respective output terminals of this shift register 4 and sequentially scanned by the clock signals Φ_{1V} and Φ_{2V}, are supplied through gate lines G_1, G_2, ... G_n in the horizontal (X axis) direction to control terminals of the switching elements M_{11} to M_{nm} at every rows (M_{11} to M_{1m}), (M_{21} to M_{2m}), ... (M_{n1} to M_{nm}) in the X axis direction, respectively. Also, the shift register 4 is supplied with the potentials V_{SS} and V_{DD} similarly to the shift register 2.

That is, in this circuit, to the shift registers 2 and 4, there are supplied the clock signals Φ_{1H}, Φ_{2H}, Φ_{1V} and Φ_{2V} which are shown in Figs. 7A and 7B. Then, the shift register 2 generates signals ϕ_{H1} to ϕ_{Hm} at every picture element period as shown in Fig. 7C, while the shift register 4 generates signals ϕ_{V1} to ϕ_{Vn} at every one horizontal period as shown in Fig. 7D. Further, to the input terminal 1, there is supplied a signal as shown in Fig. 7E.

When the signals ϕ_{V1} and ϕ_{H1} are generated, the switching elements M_1 and M_{11} to M_{1m} are turned on and

thereby a current path from the input terminal 1 through M_1, L_1, M_{11}, C_{11} to the target terminal 3 is formed, through which a potential difference between the signal supplied to the input terminal 1 and that at the target terminal 3 is supplied to the liquid crystal cell C_{11}. As a result, in the capacitive portion of the cell C_{11}, there is sampled and then held a charge corresponding to a potential difference made by the signal of a first picture element. The optical transmissivity of the liquid crystal is changed in response to this charge amount. The similar operation is sequentially carried out on the following cells C_{12} to C_{nm}. Further, when the signal of the next field is supplied, the charge amounts of the respective cells C_{11} to C_{nm} are re-written.

As described above, the optical transmissivities of the liquid crystal cells C_{11} to C_{nm} are changed in response to the respective picture elements of the video signal, and this operation is sequentially repeated to thereby display a television picture.

By the way, when the display is carried out by the liquid crystal, an AC drive is generally adopted so as to improve its reliability and its service life. In the display of, for example, a television picture, a signal, which results from inverting a video signal at every one field or at every one frame, is supplied to the input terminal 1. In other words, to the input terminal 1, there is supplied a signal which is inverted at every one field or at every one frame as shown in Fig. 7E.

By the way, it is requested to display an arbitrary television picture in the form of a still picture by the

above mentioned apparatus. In that case, it has been proposed in the prior art that there is provided a memory having, for example, one field or one frame storage capacity, a desired picture is stored in this memory, it is repeatedly read out therefrom, the signal read out is phase-inverted at every field and then fed to the above mentioned input terminal 1. However, the memory having the capacity of one field or one frame itself is very large in size and expensive so that it is difficult to apply it to a standard commercially available apparatus.

On the other hand, it is proposed to display the still picture by utilizing the memory function of the liquid crystal cell C. That is, in a liquid crystal video display drive circuit having a first sample and hold circuit for supplying a video signal having a polarity inverted at every picture to a plurality of picture elements in a time series fashion, this apparatus is a liquid crystal video display drive circuit which comprises inverting means for inverting the video signal and supplying it to the first sample and hold circuit, a second sample and hold circuit for reading the video signal of the plurality of picture elements in a time series fashion, and switching means for switching a video signal from an external terminal or the video signal from the second sample and hold circuit and supplying it to the inverting means.

However, in the case of this apparatus, each time the display of one field is carried out, the picture is displaced by one picture element each in the scanning direction. As a result, the processing such as to reverse the scanning direction at every one field and the like is

carried out. In order to switch the scanning direction as set forth above, a circuit of a large scale must be provided and, there remains the state in which the picture is alternately displaced by one picture element at every one field. There is a fear that this will give rise to a flicker and so on.

Since the signal of the liquid crystal cell C is derived, this signal is returned again to the liquid crystal cell C and this operation is repeated to thereby carry out the display of the still picture, if a signal transmission characteristic during such period has a distortion, this distorion is accumulated, deteriorating the quality of the picture considerably in a very short time period. To cope therewith, it may be considered to adjust the gain of the inverting means. However, it is impossible to carry out such adjustment perfectly and it is almost difficult to carry out the normal display of the still picture during a long time period.

Further, when the signal is derived from the liquid crystal cell C, if a residual charge exists in a stray capacity of the signal line and the like, this causes the signal to be deteriorated so that the display of the still picture can not be carried out over a long time period any more.

DISCLOSURE OF INVENTION

This invention is made in view of the above described problems. According to the apparatus, since the signal derived from the liquid crystal cell C is returned to the same liquid crystal cell C, the displacement of the picture and so on can be avoided, any special scanning and the like

become unnecessary and the prior art drive circuit and the like can be used without modification. Further, since the potential of the signal line of the signal is reset, the quality of picture can be prevented from being deteriorated and also, it is possible to carry out the display of the still picture over a long time period.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a constructional diagram of a liquid crystal display apparatus according to the present invention, Figs. 2 to 5 are diagrams useful for the explanation thereof, and Figs. 6 and 7 are diagrams used to explain a prior art apparatus.

BEST MODE FOR CARRYING OUT THE INVENTION

In Fig. 1, the above mentioned switching elements M_1 to M_m are used as first switching elements M_{A1} to M_{Am} and there are provided equivalent second switching elements M_{B1} to M_{Bm}. Further, there is provided a shift register 20 having m stages similar to the above mentioned shift register 2. The clock signals Φ_{1H} and Φ_{2H} are supplied to this shift register 20. Picture element switching signals ϕ_{H1}, ϕ_{H2}, ... ϕ_{Hm} are supplied from the respective output terminals of the shift register 20 to the respective control terminals of the switching elements M_{B1} to M_{Bm}. To the shift register 2, there is supplied a start pulse ϕs which is associating to the horizontal synchronization of the video signal, while to the shift register 20, there is supplied a start pulse ϕ's the phase of which is advanced from that of the pulse ϕs. The input terminal 1 is connected through a normal display side contact N of a normal display/still picture display change-over switch 11

to the switching elements M_{A1} to M_{Am}. The connecting point among the switching elements M_{B1} to M_{Bm} is connected to an amplifier 12 and a capacitor 13 is connected to the output terminal of this amplifier 12. This output terminal is connected through an inverting circuit 14 to a normalizing circuit (normalizer) 15. The output terminal of this normalizing circuit 15 is connected to a still picture display side contact S of the change-over switch 11. To the respective signal lines L_1 to L_m, there are respectively connected switching elements M_{R1}, M_{R2}, ... M_{Rm} and they are connected through these switching elements M_{R1} to M_{Rm} to a predetermined voltage source, for example, a target terminal 3.

In this apparatus, to the gate terminals of the switching elements M_{A1} to M_{Am}, there are supplied picture element switching signals ϕ_{H1} to ϕ_{Hm} shown at D and formed by clock signals Φ_{1H}, Φ_{2H} shown at A and B in Fig. 2 and the start pulse ϕs shown at C. While, to the gate terminals of the switching elements M_{B1} to M_{Bm}, there are supplied picture element switching signals ϕ_{H1}' to ϕ_{Hm}' shown at F and formed by the start pulse ϕ's shown, for example, at E in Fig. 2.

Consequently, at the phase of, for example, the picture element switching signal ϕ_{H1}, by the picture element switching signal ϕ_{H3}' which is the same in phase, the signal of the liquid crystal cell C corresponding to the line L_3 is derived. This signal is accumulated through the amplifier 12 in the capacitor 13 and then written through the inverting circuit 14 and the normalizing circuit 15 in the same liquid crystal cell C at the phase of the picture

element switching signal ϕ_{H3} with a delay of τ time. Here, the potential of the signal from the liquid crystal cell C assumes vs and the capacity of the capacitor 13 assumes Cs. Then, a potential vs' at the hot side of the capacitor 13 becomes as $vs' = \frac{Cp}{Cs}$ vs where Cp is the capacity of the amplifier 12. If the gain of the inverting circuit 14 is taken as - A, a potential vs'' of the output from this inverting circuit 14 becomes as $vs'' = - A \frac{Cp}{Cs}$ vs. Therefore, if the value of - A is determined in such a manner that this potential vs'' satisfies vs = - vs, the signal same as that inverted is re-written in the liquid crystal cell C and thereby the still picture display is carried out by the AC drive.

In this case, however, it is impossible to determine the value of - A perfectly as above mentioned. For this reason, there is provided the normalizing circuit 15. That is, the input and output characteristics of this normalizing circuit 15 is as shown in Fig. 3, in which relative to potentials Vk-2, Vk-1, Vk, Vk+1, Vk+2, the input signals in a range of $\pm \alpha$ are normalized as Vk-2, Vk-1, Vk, Vk+1, Vk+2 and then output. Accordingly, owing to the provision of this circuit 15, even if the value of - A has a slight ($\pm\alpha$) error, it is possible to always make the value of the output signal (the re-written signal) constant.

Further, to the gate terminals of the switching elements M_{R1} to M_{Rm}, there is supplied a horizontal blanking signal ϕ_{HBLK}. As a result, the respective signal lines L_1 to L_m are reset to the target voltage at every horizontal blanking. Thus, the signal remaining in each signal line is reset so that when the signal in the liquid crystal cell C

is derived, a undesired signal can be avoided from being mixed thereto.

In this way, the display of the still picture is carried out. According to the above mentioned apparatus, the arrangement thereof is extremely simplified, and even when the display is carried out over a long time period, the signal can be prevented from the deterioration, and hence the satisfactory still picture display can be always carried out.

While in the above mentioned apparatus, the delay time τ from the readout to the writing is restricted by the periods of the clock signals Φ_{1H} and Φ_{2H}, it is also possible to set a more delicate delay time by arbitrarily determining the phase of the clock signal which is to be supplied to the shift registers 2 and 20.

While in the afore-mentioned apparatus the normalizing circuit 15 must carry out sequentially the normalizing processing at a time less than one picture element clock, when the processing time is insufficient in the cases, such as to improve the resolution of the normalization and the like, it is possible to carry out the parallel processing as shown, for example, in Fig. 4. In the figure, the display section is omitted. Further, Fig. 5 is a flow chart thereof.

That is, in this figure, the signal read out from the liquid crystal cell C connected to the line L_1 at the phase of the horizontal switching signal Φ_{H1}' shown, for example, at A is held in a sample and hold (SH) circuit 31a by a sampling pulse Pa shown at B and then supplied through a switching element Ma to a normalizing circuit 15a during the

period of a switching signal ϕa shown at E. Then, the signal normalized during the two-picture element clock periods is held during the period of a switching signal $\phi a'$ shown at H through a switching element Ma' in a sample and hold circuit 32a by a sampling pulse Pa' shown at K and then written in the liquid crystal cell C connected to the signal line L_1 at the phase of a horizontal switching signal ϕ_{H1} shown at N. The similar operations will hereinafter be carried out at every one picture element clock by circuits suffixed by b and c and the operation will be returned to a circuit suffixed by a and thereby repeated at every three picture element clocks. Therefore, according to this apparatus, it becomes possible to set a processing time twice that of the apparatus in Fig. 1.

In this case, this apparatus can be applied to a liquid crystal display apparatus formed of an active matrix using TFTs, such as an amorphous silicon, a polysilicon, a silicon sapphire, an organic semiconductor and the like.

Further, it is possible to provide the above mentioned shift registers 2, 4 and 20 outside the IC which forms the apparatus.

Furthermore, the display can be applied to both of dot-sequential type display and line-sequential type display.

CLAIMS

1. In a liquid crystal display apparatus in which video signals are sequentially supplied through first horizontal switching elements, which are turned on by first picture element switching signals sequentially formed at a horizontal picture period, to columns of the number corresponding to the number of effective horizontal picture elements, scanning line switching signals, which are sequentially formed at a horizontal scanning period, are sequentially supplied to rows of the number corresponding to the number of effective horizontal scanning lines and said video signals which are respectively supplied to said columns are supplied through picture element switching elements, which are provided at intersections between respective columns and rows and which are turned on by said scanning line switching signals, to liquid crystal cells, each of which forms one picture element, said liquid crystal display apparatus being characterized in that second horizontal switching elements, which are driven by second picture element switching signals having advanced phases relative to said first picture element switching signals, are connected to said columns, said video signals stored in said liquid crystal cells are read out through said picture element switching elements during a period in which said second horizontal switching elements are turned on, said signals read out are inverted, said inverted signals are sequentially supplied through said first horizontal switching elements to said columns to have a phase delayed by a delay amount corresponding to said advanced phase, and a reset voltage is supplied through third switching elements, which are turned on at every horizontal

blanking periods of said video signal, to said columns.

2. A liquid crystal display apparatus according to claim 1, characterized in that said inverting processing contains a signal normalization processing.

3. A liquid crystal display apparatus according to claim 2, characterized in that the signal normalization processing contained in said inverting processing is carried out in a parallel processing manner.

4. A liquid crystal display apparatus according to claim 1, characterized in that said first and second picture element switching signals are generated by a pair of shift registers and are used to on-drive said first and second horizontal switching elements, respectively.

5. A liquid crystal display apparatus according to claim 4, characterized in that said pair of shift registers are respectively supplied with clock pulses and a phase difference between said clock pulses becomes a phase difference between said first and second picture element switching signals.

6. A liquid crystal display apparatus according to claim 5, characterized in that said phase difference is made equal to a time period necessary for said inverting processing.

7. A liquid crystal display apparatus according to claim 6, characterized in that said inverting processing contains a signal normalization processsing.

8. A liquid crystal display apparatus according to claim 7, characterized in that the signal normalization processing contained in said inverting processing is carried out in a parallel processing manner.

(SUBSTITUTED)

CLAIMS

1. (After being amended) In a liquid crystal display apparatus in which video signals are sequentially supplied to columns of the number corresponding to the number of effective horizontal picture elements through first horizontal switching elements which are turned on by first picture element switching signals, which are seuentially formed at a horizontal picture element period, scanning line switching signals, which are sequentially formed at a horizontal scanning period, are sequentially supplied to lines of the number corresponding to the number of effective horizontal scanning lines, and said video signals sequentially supplied to said columns through picture element switching elements, which are provided at intersections between said columns and rows and which are turned on by said scanning line switching signals, are supplied to liquid crystal cells each of which forms one picture element, said liquid crystal display apparatus being characterized in that second horizontal switching elements, which are driven by second picture element switching signals having a phase advanced relative to said first picture element switching signals, are connected to said columns, said video signals stored in said liquid crystal cells are derived during a period in which said second horizontal switching elements are turned on, said signals derived are inverted and said inverted signals with a phase delayed by an amount corresponding to said advanced phase are sequentially supplied through said first horizontal switching elements to said columns to thereby display a still picture.

2. A liquid crystal display apparatus according to claim 1, characterized in that said inverting processing contains a signal normalization processing.

3. A liquid crystal display apparatus according to claim 2, characterized in that the signal normalization processing contained in said inverting processing is carried out in a parallel processing manner.

4. A liquid crystal display apparatus according to claim 1, characterized in that said first and second picture eloement switching signals are generated from a pair of shift registers and are used to turn on said first and second horizontal switching elements, respectively.

5. A liquid crystal display apparatus according to claim 4, characterized in that said pair of shift registers are respectively supplied with clock pulses and a phase difference between said clock pulses becomes a phase difference between said first and second picture element switching signals.

6. A liquid crystal display apparatus according to claim 5, characterized in that said phase difference is made equal to a time period necessary for said inverting processing.

7. A liquid crystal display apparatus according to claim 6, characterized in that said inverting processing contains a signal normalization processing.

8. A liquid crystal display apparatus according to claim 7, characterized in that said signal normalization processing contained in said inverting processing is carried out in a parallel processing manner.

9. (Added) A liquid crystal display apparatus according to

claim 1, characterized in that a reset voltage is supplied to each of said columns through third switching elements which are turned on at every horizontal blanking period of said video signal.

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FIG. 1

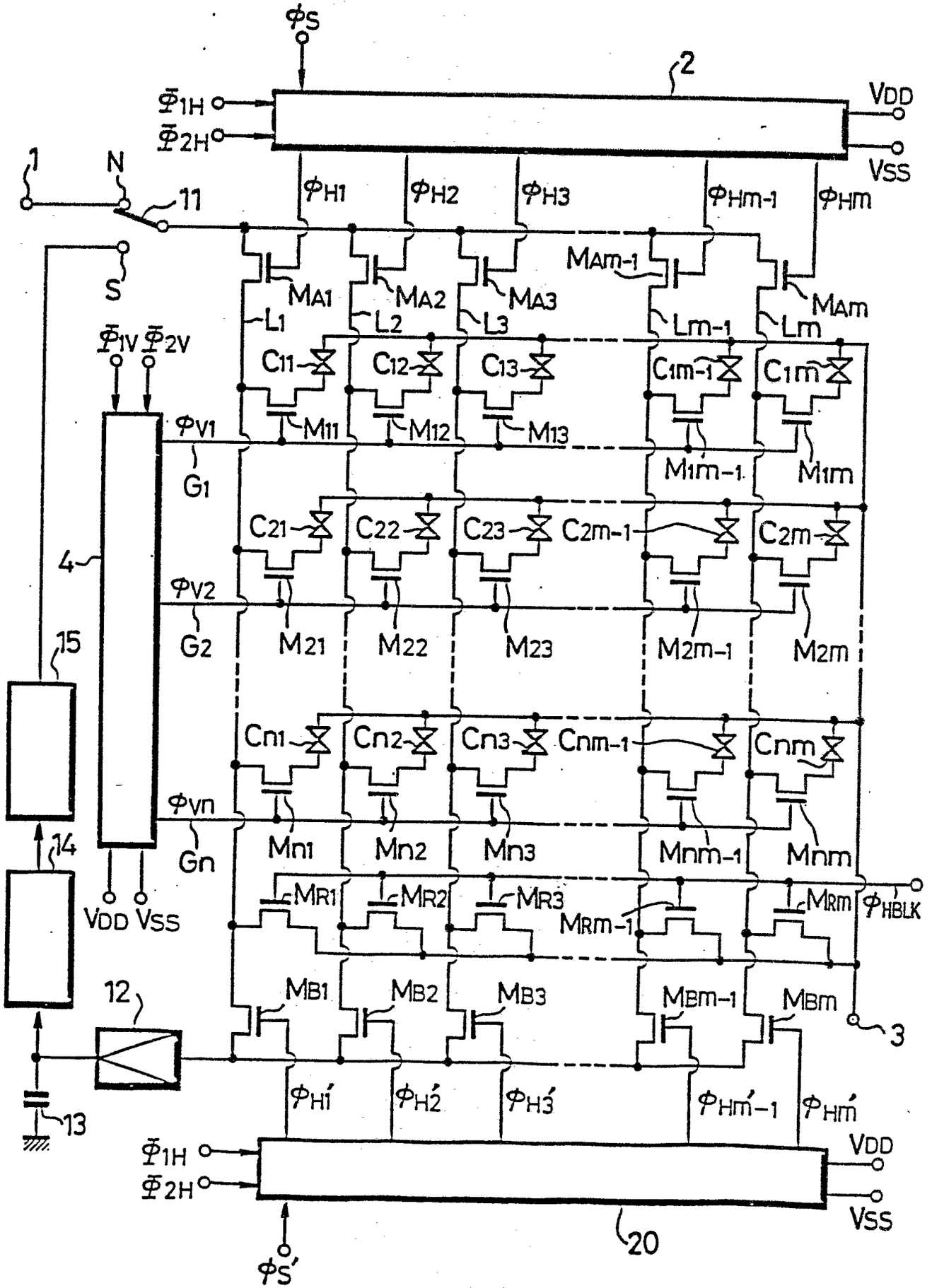


FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

FIG. 2E

FIG. 2F

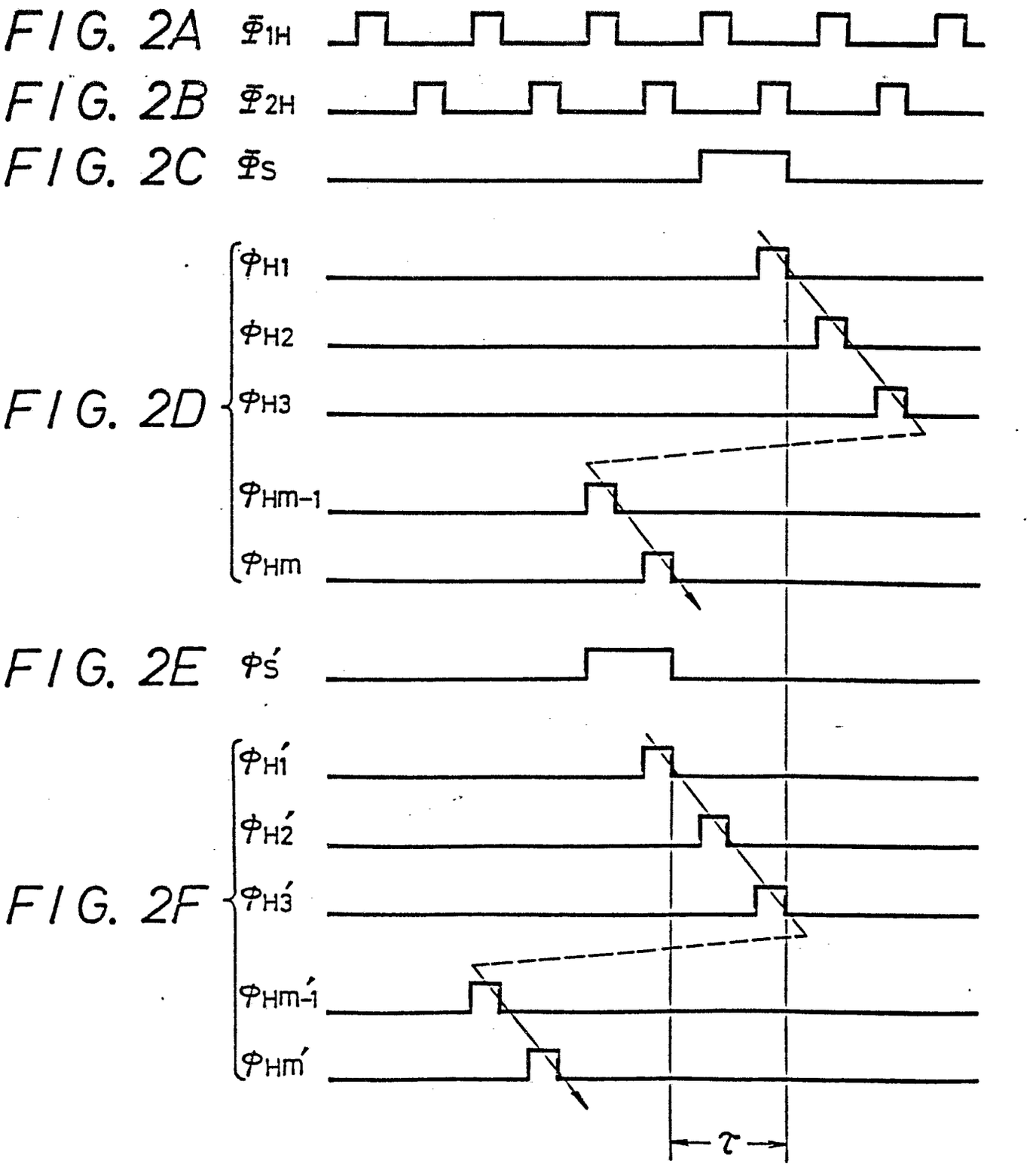


FIG. 3

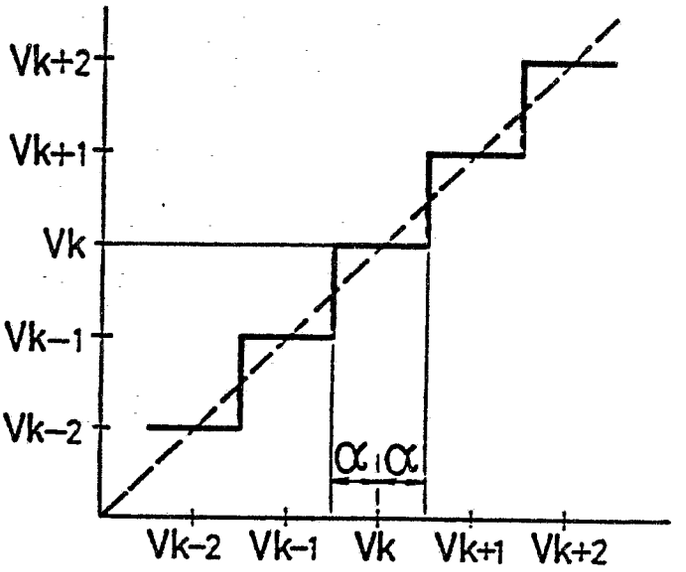

Vk+2
Vk+1
Vk
Vk−1
Vk−2
α
α
Vk−2
Vk−1
Vk
Vk+1
Vk+2

FIG. 4

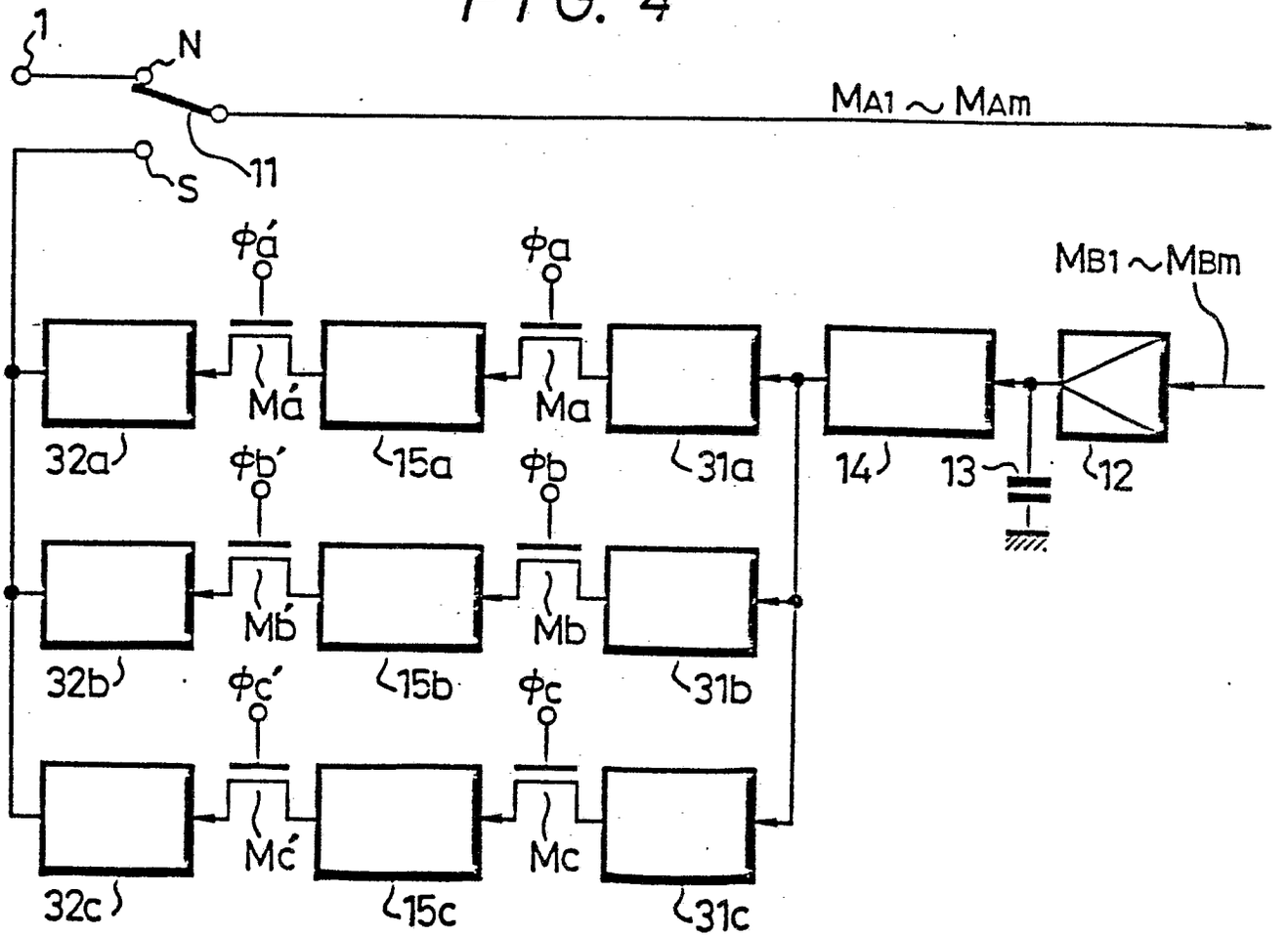

1
N
MA1 ~ MAm
S
11
φá
φa
MB1 ~ MBm
Má
Ma
32a
15a
31a
14
13
12
φb'
φb
Mb́
Mb
32b
15b
31b
φc'
φc
Mć
Mc
32c
15c
31c

FIG. 5A

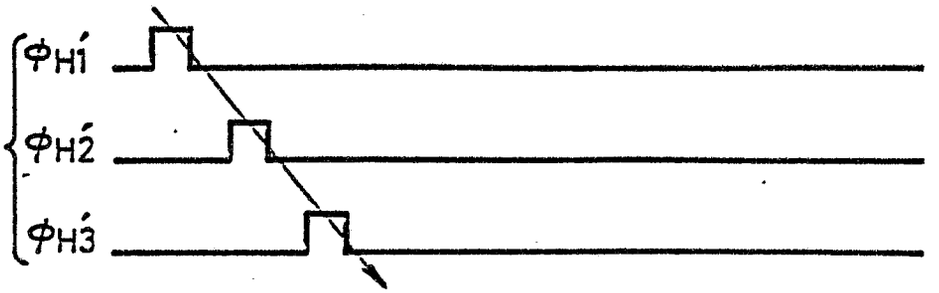


FIG. 5B



FIG. 5C



FIG. 5D



FIG. 5E



FIG. 5F

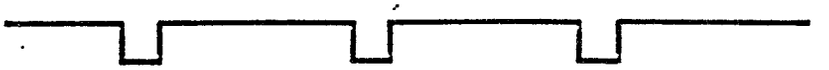


FIG. 5G



FIG. 5H



FIG. 5I



FIG. 5J



FIG. 5K

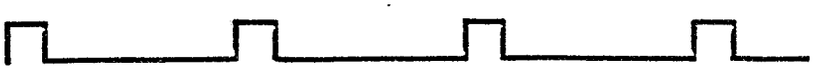


FIG. 5L



FIG. 5M



FIG. 5N

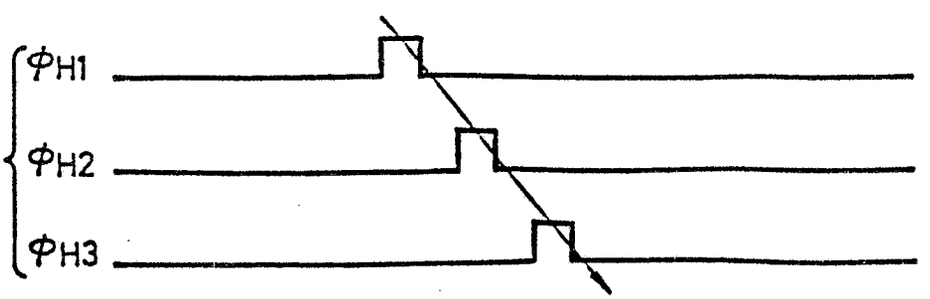


FIG. 6

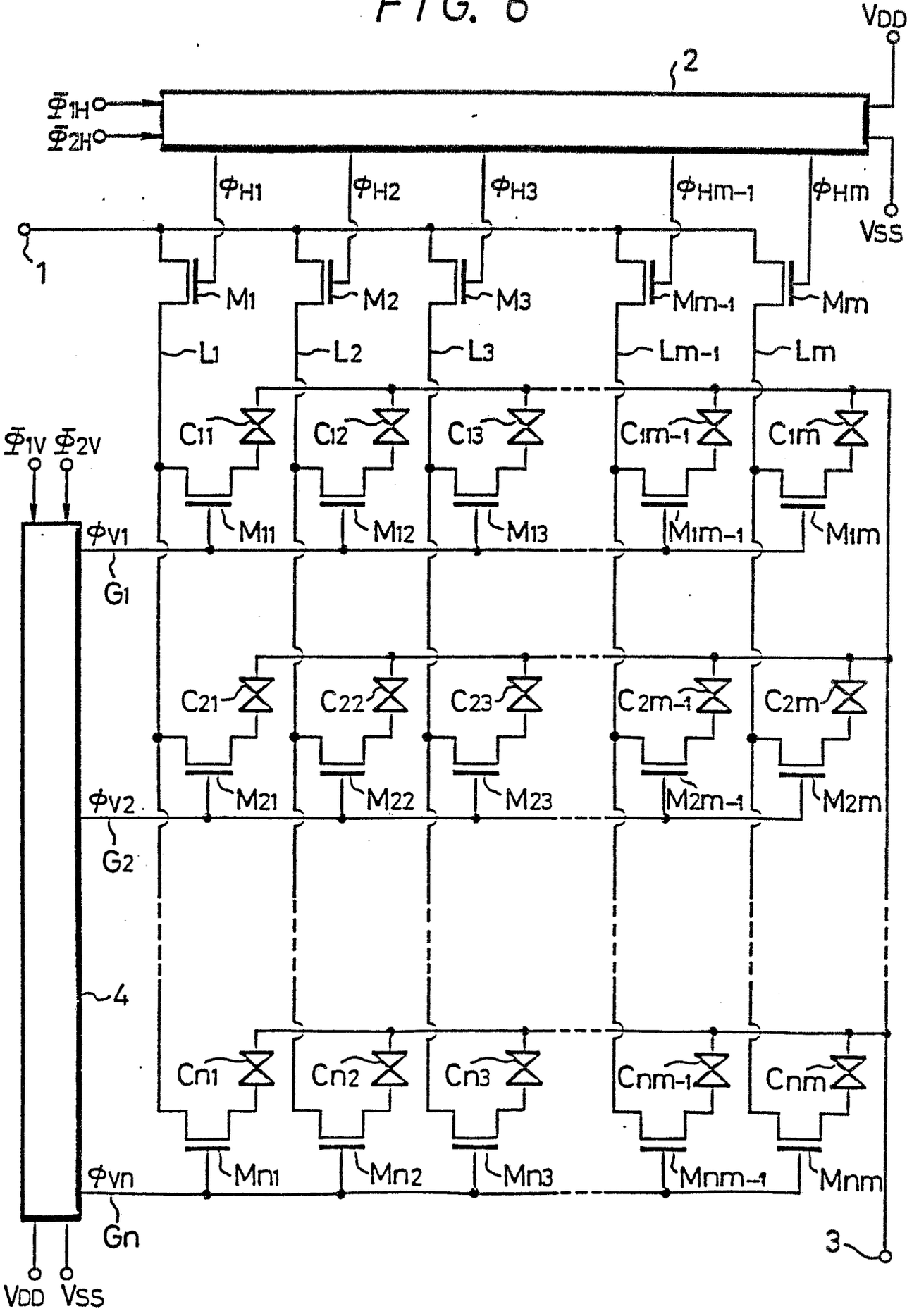

VDD
2
Φ1H
Φ2H
ΦH1
ΦH2
ΦH3
ΦHm-1
ΦHm
VSS
1
M1
M2
M3
Mm-1
Mm
L1
L2
L3
Lm-1
Lm
C11
C12
C13
C1m-1
C1m
Φ1V
Φ2V
M11
M12
M13
M1m-1
M1m
ΦV1
G1
C21
C22
C23
C2m-1
C2m
M21
M22
M23
M2m-1
M2m
ΦV2
G2
4
Cn1
Cn2
Cn3
Cnm-1
Cnm
Mn1
Mn2
Mn3
Mnm-1
Mnm
ΦVn
Gn
3
VDD
VSS

FIG. 7A

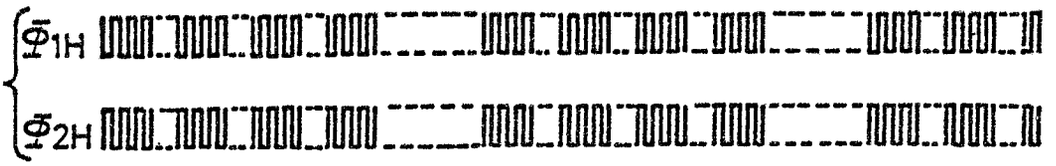


FIG. 7B

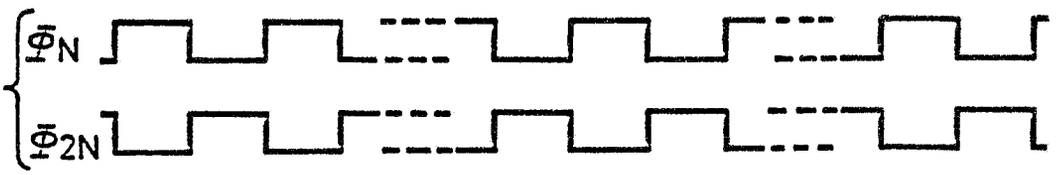


FIG. 7C

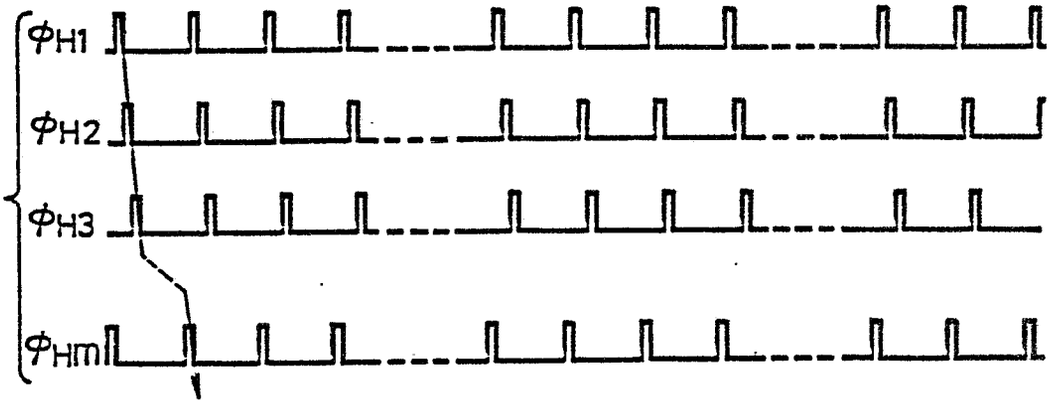


FIG. 7D

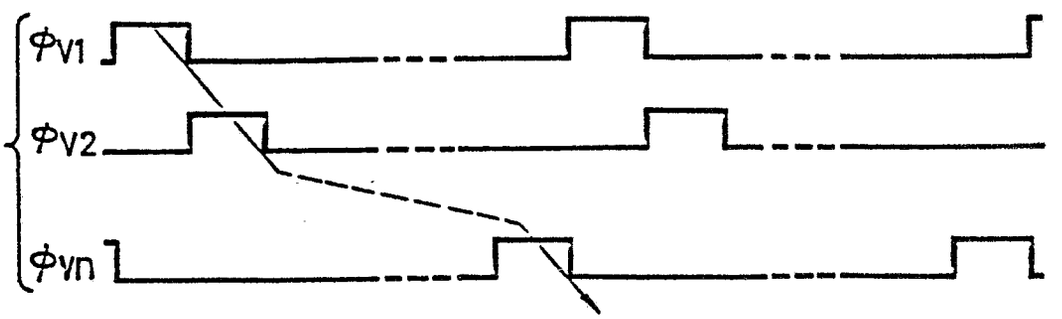


FIG. 7E

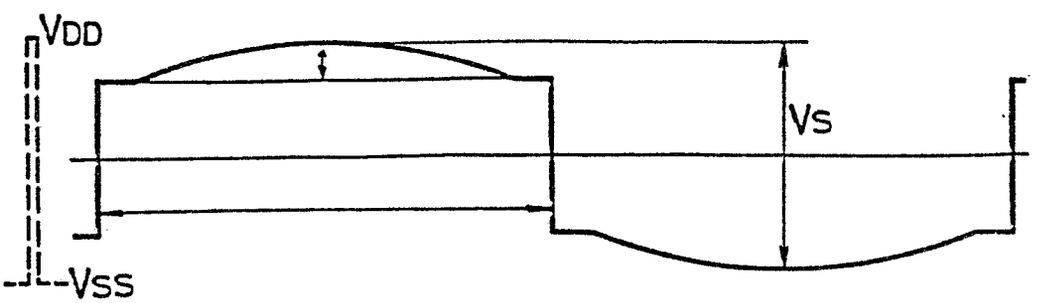


TABLE FOR REFERENCE NUMERALS AND COMPONENTS

reference numerals	components
2, 4 and 20	the shift registers
14	the inverting circuit
L_1 to L_m	the vertical signal line
M_{A1} to M_{Am}	the first switching elements
M_{B1} to M_{Bm}	the second switching elements
M_{R1} to M_{Rm}	the third switching elements
C_n to C_{nm}	the liquid crystal display cells

INTERNATIONAL SEARCH REPORT

0192784

International Application No. PCT/JP85/00508

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl[4] G09G3/36, G02F1/133, H04N5/66

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	G09G3/36, G02F1/133, H04N5/66

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

Jitsuyo Shinan Koho 1926 - 1985
Kokai Jitsuyo Shinan Koho 1971 - 1985

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category*	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	JP, A, 59-24892 (Nippon Telegraph & Telephone Public Corp.), 8 February 1984 (08. 02. 84) (Family: none)	1 - 8

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
December 5, 1985 (05. 12. 85)	December 16, 1985 (16. 12. 85)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
Japanese Patent Office	