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[33] **France**

[31] **PV79,568**

[54] **APPARATUS FOR CONTROLLING THE MEAN
VALUE OF CURRENT SUPPLIED BY AN
ALTERNATING CURRENT SOURCE TO AN
ELECTRIC APPARATUS**
7 Claims, 6 Drawing Figs.

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307/252; 323/22, 323/24

[51] Int. Cl. **H02m 1/08,**
H02p 13/16

[50] Field of Search..... 328/63, 7,
2, 75, 81, 92, 136; 321/5, 16, 47; 323/22SCR, 24;
307/233, 252, 269, 271

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ABSTRACT: Device for regulating the mean value of current supplied by an AC current source to an electrical apparatus, dependent on data supplied by a computer, comprising a cycle counter having N binary flip-flops providing N binary signal combinations of a series of 2^N pulses and a control arrangement responsive to the computer for applying one of 2^N combinations of said N binary signals in control of the current supplied to said electrical apparatus.

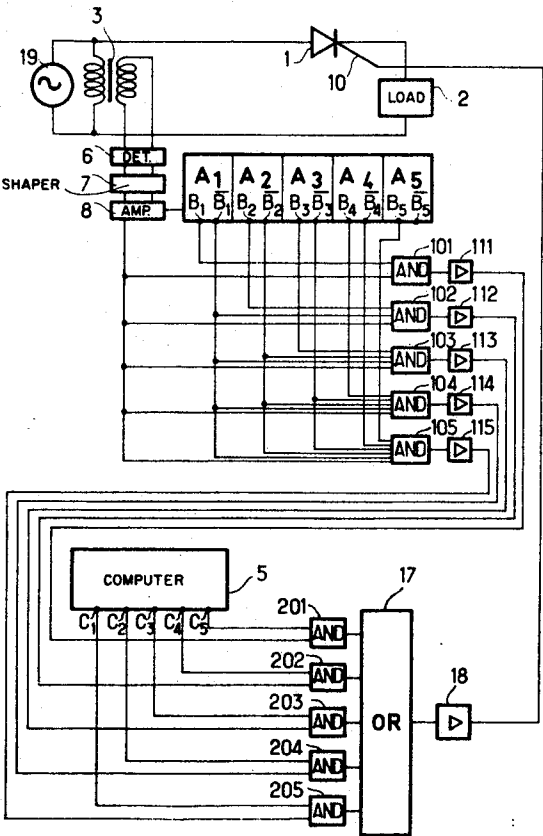


FIG. 1

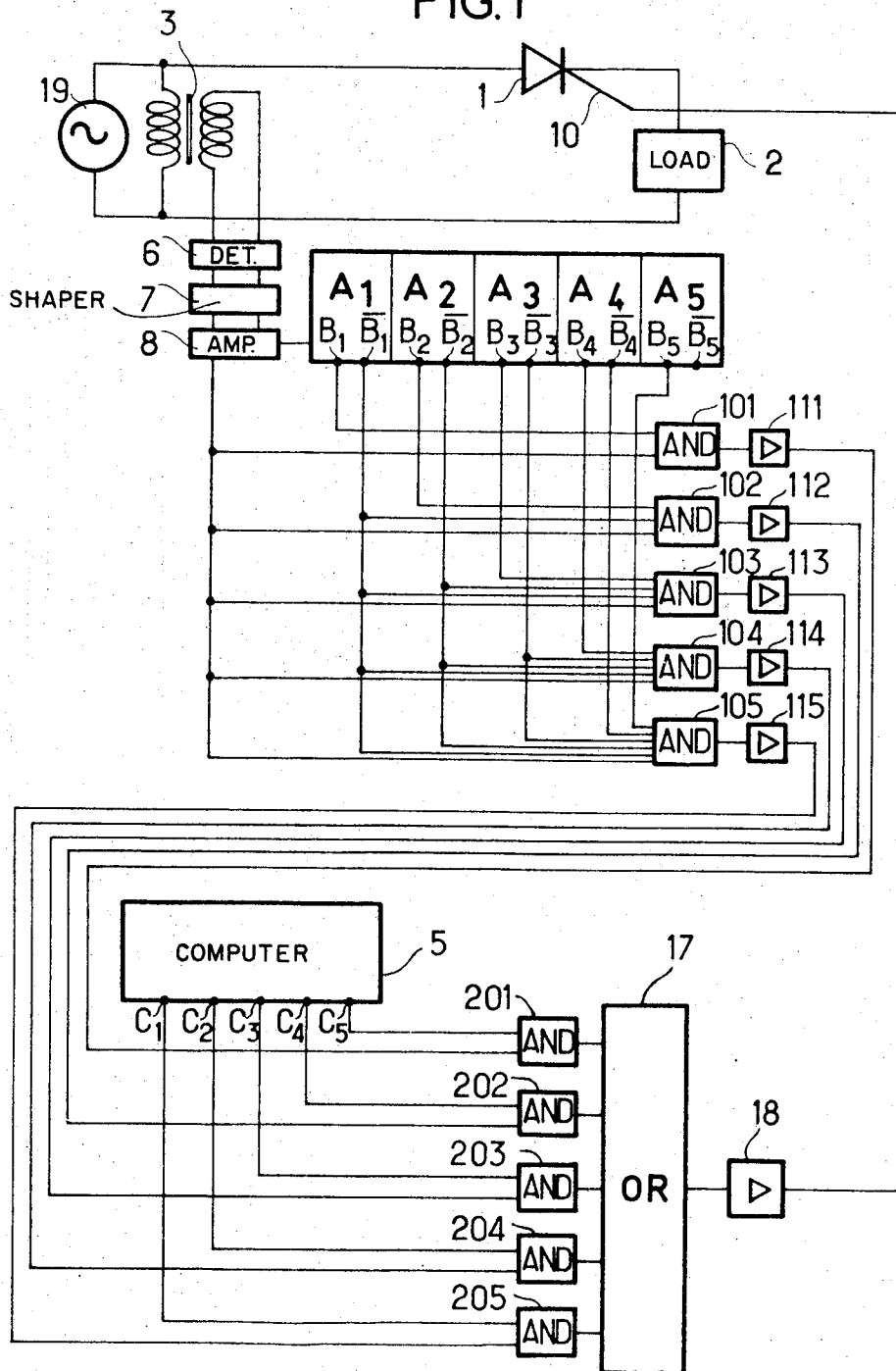


FIG.2

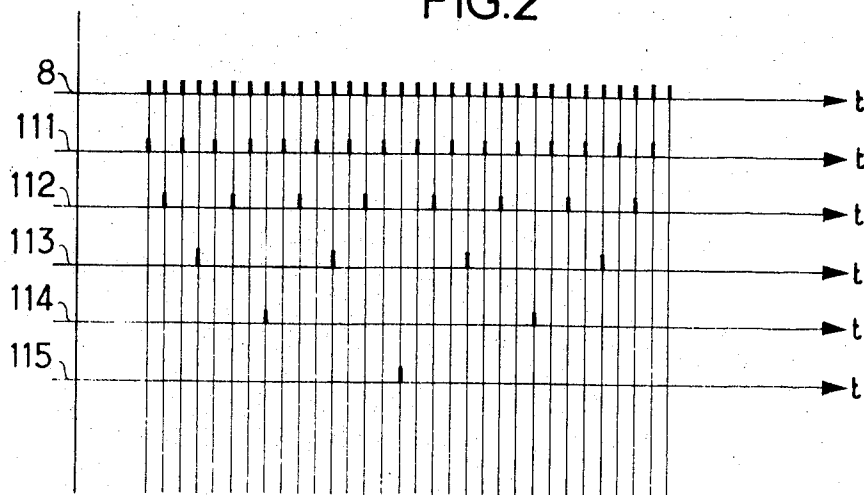
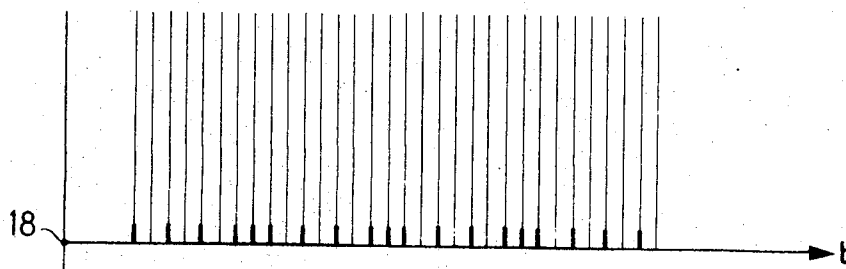
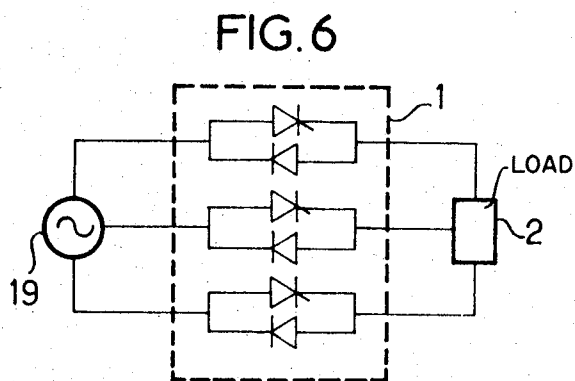
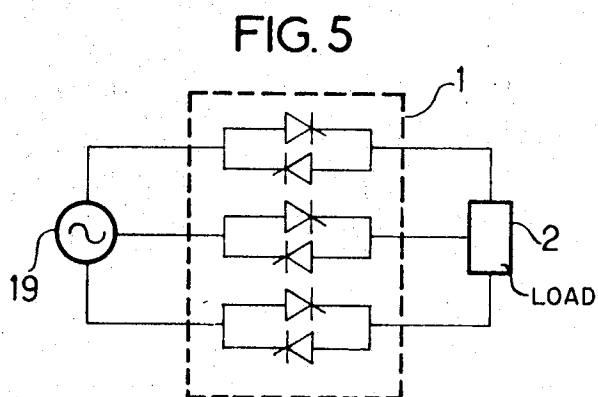
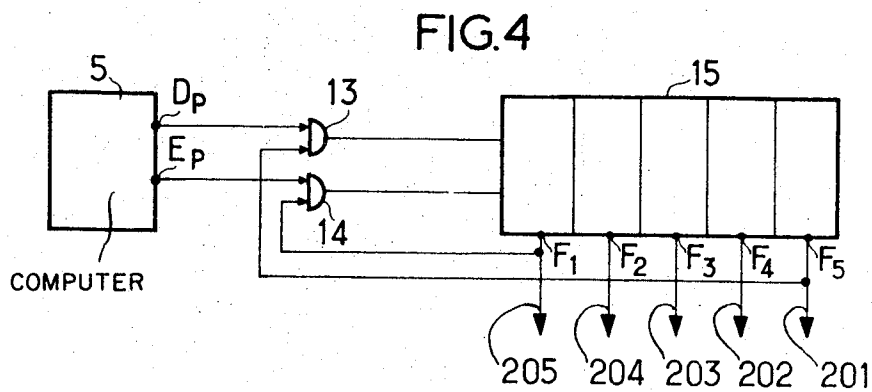


FIG.3





APPARATUS FOR CONTROLLING THE MEAN VALUE OF CURRENT SUPPLIED BY AN ALTERNATING CURRENT SOURCE TO AN ELECTRIC APPARATUS

The invention concerns an apparatus for controlling the firing of a group of thyratrons or other current control devices at a rhythm preset by an electronic computer.

There is known an apparatus for supplying a plurality of electrical apparatus from an alternating current source through a series of semiconductor rectifier groups, in a proportion of one rectifier group per electrical apparatus. The apparatus makes it possible to render the rectifier groups conductive for a certain number of p of consecutive half-cycles, each of a duration of $\frac{T}{2}$, of the current and to render them nonconductive for another number q of consecutive half-cycles. The duration $(p+q)\frac{T}{2}$ is referred to as the "sequence."

To this end, the aforesaid apparatus comprises for each electrical apparatus to be supplied a power stage comprising in series a voltage source, the apparatus itself and a rectifier group. The rectifier group is preferably a thyatron or a number of thyratrons connected in push-pull. The source supplying the power stage, in series with the electrical apparatus and the rectifier group, is single-phase or polyphase. The aforesaid apparatus also comprises a control stage comprising a computer to which a program is fed and an electronic unit which interprets the orders from the computer and transmits them to the power stage.

The control stage of the aforesaid apparatus comprises a means for detecting the change of the amplitude of the voltage of the source to a given value. In addition, the control stage comprises means for converting the numerical indication of the computer into a train of pulses applied to the control electrodes of the rectifier group, in phase with the supply voltage of the latter and synchronously with the passage of the said voltage through the aforesaid given value.

In this stage, the pulses are utilized in such a manner that the rectifier passes the current from the supply source for a series p of consecutive half-cycles of this current, without omitting any of them, and then interrupts the said current for the duration of another series q of consecutive half-cycles. This process is cyclically repeated; it is the computer which, in accordance with the established program, determines the number of pulses in each train.

It is obvious that the notion of the mean energy received by the apparatus can be appreciated only if it is calculated for a period of time corresponding to a number of cycles; for a period of time less than one complete cycle, this notion has no significance.

One object of the present invention is to modify the control stage in such manner that the momentary energy is closer to the mean energy than it is with the aforesaid apparatus.

The invention relates to an apparatus for controlling the mean value of the current supplied to an electrical apparatus comprising, on the one hand, an alternating current source and a rectifier device having a control electrode, which are connected in series with the said apparatus, and on the other hand a device for detecting the passage of the voltage across the terminals of the current source, connected to a device which emits a pulse of calibrated value at each passage of the said voltage through the said value, and comprising in addition an apparatus of the digital computer type having N outputs, which is capable of representing at its outputs any number between 1 and $2N$ the adjustment of the mean value of the current passing through the said apparatus being effected in accordance with a program fed to the computer, by rendering the said rectifier device conductive for a number r of current cycles, each of a duration equal to T , distributed over a duration $2NT$, called the sequence, the value r being displayed in accordance with the program established at the terminals of the computer, characterized by the fact that the output of the said device emitting calibrated pulses of period T is connected to the input of an electronic device having N outputs which is capable of processing at its respective outputs trains of pulses

of periods $2T, 4T, \dots, 2NT$ time-delayed in relation to the first calibrated pulse of the train of pulses of period T , by times $0, T, 2T, 2^{N-1}T$ respectively, the N outputs of the aforesaid electronic device being connected respectively to N first inputs of N AND circuits each having two inputs and one output, the N second inputs being connected respectively to the N outputs of the aforesaid device of the digital computer type, each of the outputs of the aforesaid N AND circuits being connected to each of the N inputs of an OR circuit whose output is connected to the control electrode of the aforesaid rectifier device.

The present invention will be more readily understood with reference to the accompanying drawings, in which:

FIG. 1 is a circuit diagram of an apparatus according to the present invention;

FIGS. 2 and 3 are diagrams serving to explain the operation of the apparatus of FIG. 2;

FIG. 4 illustrates a variant of the apparatus according to the present invention; and

FIGS. 5 and 6 illustrate two forms of construction of three-phase current rectifier groups.

In FIG. 1, the reference 19 denotes a current source intended to supply an electrical apparatus 2, for example an infrared lamp. Connected in series between the said source 19 and the apparatus 2 is a rectifier group symbolically represented by a thyatron 1 provided with its control electrode 10. This rectifier group may be in the case where source 19 is a three-phase supply, a set of thyristors connected in push-pull in a proportion of two push-pull thyristors per phase, as illustrated in FIG. 5, or a mixed set comprising for each phase a thyristor and a diode connected in push-pull, as illustrated in FIG. 6. In the case of continuous supply, the rectifier group may have any of the features well known to the person skilled in the art.

Referring again to FIG. 1, it will be seen that a transformer 3 whose primary winding is connected to the terminals of the source 19 supplies through its secondary winding a device 6 for detecting the passage of the voltage of the source through a given value in a given sense, which device produces a pulse every time the said voltage passes through the said value. Owing to the fact that the transformer 3 is connected in parallel with the source, both the zero value of the voltage and any other value may be detected.

The pulses emanating from the detector 6, which are of irregular form, are calibrated by a so-called "shaping" member 7 and brought into a form suitable for use by a pulse counter. After amplification by an amplifier 8, the pulses are sent to a counter of the binary type comprising N bistable flip-flops. In the example of the figure, N has been assumed to be equal to 5. This counter permits of counting $2^5 = 32$ consecutive pulses. This number of flip-flops is given by way of example. It will be seen that it is desirable to increase the number of flip-flops if it is desired to increase the fineness of the control of the apparatus.

Each counter element may assume two stable states represented by the presence (state 1) or absence (state 0) of a voltage at one of its output terminals. Each flip-flop has two outputs, the second output representing the complementary state of the first. There are denoted by $A_1, A_2, \dots, A_5$ the five flip-flops of the counter, and by B_1 and $\bar{B}_1, B_2$ and $\bar{B}_2, \dots, B_5$ and $\bar{B}_5$, their respective pairs of outputs, B_i being the output which supplies the state of the flip-flop and $\bar{B}_i$ that which gives the complementary state. Due to the design of a binary counter, the flip-flop A_1 changes its state at each pulse received, the flip-flop A_2 at every two pulses received, the flip-flop A_3 at every $2^2 = 4$ pulses, the flip-flop A_4 every $2^3 = 8$ pulses and the flip-flop A_5 every $2^4 = 16$ pulses (in the general case, A_i changes its state every 2^{i-1} pulses).

The control stage also comprises five AND circuits (in the general case, in which there are N bistable flip-flops, it comprises N AND circuits). These AND circuits are denoted by the references 101 to 105. They possess respectively from 2 to 6 inputs (in the general case, from two to $N+1$ inputs). One input of each of them is connected to the output of the ampli-

fier 8 which emits a pulse per cycle of the voltage 19. The other inputs of the AND circuits are connected as follows:

- in the case of the AND circuit 101 to B_1
 - in the case of the AND circuit 102 to B_2 and $\bar{B}_1$
 - in the case of the AND circuit 103 to B_3 , $\bar{B}_1$ and $\bar{B}_2$
 - in the case of the AND circuit 104 to B_4 , $\bar{B}_1$, $\bar{B}_2$ and $\bar{B}_3$
 - in the case of the AND circuit 105 to B_5 , $\bar{B}_1$, $\bar{B}_2$, $\bar{B}_3$ and $\bar{B}_4$.
- (A Nth circuit of the general case would be connected to B_N and $\bar{B}_1, \bar{B}_2, \dots, \bar{B}_{N-1}$)

By virtue of its design, and AND circuit passes a pulse only if all the inputs are connected to a terminal displaying the state 1. Thus, in order that the circuit 101 may pass a pulse, it is necessary for B_1 to be in the state 1, which corresponds, at the counter, to a binary number, the last digit of which is of the value 1. Therefore, AND circuit 101 will pass a pulse at every second pulse emitted at the output of the amplifier 8. In order that 102 may pass a pulse, it is necessary for $\bar{B}_1$ and B_2 to be in the state 1, which corresponds, at the counter, to a binary number whose last two digits are 1 and 0. This situation arises at every four pulses emitted by the amplifier 8. In order that 103 may pass a pulse, it is necessary for $\bar{B}_1$, $\bar{B}_2$ and B_3 to be in the state 1, which corresponds, at the counter, to a binary number whose last three digits are 1, 0 and 0. This situation arises at every eight pulses emitted by 8. (It is easy to generalize in the case of N AND circuits and N flip-flops.) The Nth circuit passes a pulse at every 2^N pulses emitted by the amplifier 8.

When the counter has counted 31 pulses ($2^N - 1$ in the general case), all the flip-flops are in the state 1 and the succeeding pulse resets the counter to zero, and the counter recommences a fresh cycle.

Thus, the five circuits 101 to 105 emit periodic pulse trains having, respectively, the periods $2T$, $4T$, $8T$, $16T$ and $32T$, where T is the period of the pulses emitted at the output of the amplifier 8. In the general case, where there are N AND circuits, the Nth output circuit emits a pulse train of period $2^N T$.

FIG. 2 illustrates as a function of time, from the top downwards, the pulses emitted respectively by the output of the amplifier 8 (these pulses serve as a time base) and by the respective outputs of the amplifiers 111 to 115, connected to the outputs of the AND circuits 101 to 105.

The outputs of the amplifiers 111 to 115 are connected respectively to the first inputs of five other AND circuits denoted by 201 to 205 respectively, each of which has two inputs and one output. These AND circuits 201 to 205 are connected to the computers in the following manner: The computer has a number of output terminals equal to the number of AND circuits (five in the present case). Each of these terminals has two states (state 1 due to the presence of a potential and state 0 due to the absence of potential). In addition, these terminals are each allocated to one of the powers of 2 of 2^0 to 2^4 . These terminals are denoted by C_1 to C_5 respectively. Thus, it is possible for the machine to represent any number between 1 and 31.

The terminal C_1 (allotted to the number 2^0) is connected to the second input of the circuit 205, the terminal C_2 to the second input of the circuit 204, the terminal C_3 to the second input of the circuit 203, ... and the terminal C_5 to the second input of the circuit 201.

The AND circuits 201 to 205 pass the output trains of 101 to 105 respectively only if the terminal of the computer to which they are connected is in the state 1. The outputs of the AND circuits 201 to 205 are connected to an OR circuit 17 whose output is connected through an amplifier 18, to the control electrode 10 of the rectifier group 1.

The operation of the apparatus will be explained by means of an example:

It will be assumed that the program fed to the computer is such that the apparatus must be supplied for $r = 19$ periods each of a duration T , out of a sequence of 32 periods (of duration $2NT$). For this purpose, the computer displays the number 19 at its terminals, by bringing its terminals C_1 , C_2 and C_3 to the state 1 (binary number 1 0 0 1 1). The correspond-

ing inputs of the circuits 205, 204 and 201, are brought to the potential required for the pulse trains to pass through them.

Thus, there will be obtained at the output of the OR circuit a pulse train corresponding to the addition of the trains passing through 105, 104 and 101, i.e. 19 pulses out of 32, distributed in time as illustrated in FIG. 3 in the most harmonious possible manner. If the operating program of the apparatus is such that it is necessary to supply the apparatus for 22 periods per sequence, the computer displays the number 22 by bringing its outputs C_5 , C_3 and C_2 into the state 1, and the pulse trains of the circuits 101, 103 and 104 will be transmitted to the OR circuit 17 connected to its output.

It is obvious that the outputs C_1 to C_5 of the computer are allotted to the control of one of the rectifier groups. It is also obvious that it is possible to supply the apparatus for a chosen number of half-cycles by providing a half-wave rectifier device at the output of the transformer 3.

A number of rectifier groups, for example p , may be controlled with the aid of a computer which processes p program and displays each of them at a series of output terminals, but the same pulse distributor may be employed.

The mode of operation just described, referred to as the "coded mode," is applicable whenever there is available a computer having $p \times 2^N$ outputs, where p is the number of groups of apparatus to be controlled and N the power of 2 determining the magnitude of the cycle chosen. The value of N depends upon the desired fineness of the adjustment of the control.

A variant of the apparatus is necessary when the orders emanating from the computer arrive in an incremental form. The computer may then send two types of order:

- increase by one unit of the number of firing pulses per sequence,
- decrease by one unit.

In the absence of an order, the existing situation must be maintained.

The computer is provided with $2 \times p$ terminals (2 terminals per rectifier group to be fired).

The control stage of the apparatus then comprises the set of pulse train generating circuits which, as has been stated, is common to the various rectifier groups.

In order to translate the orders of the computer for each rectifier group, there is provided at the output terminals D_p and E_p of the computer 5 which are allocated to the p th rectifier group, as illustrated in FIG. 4, a binary counter 15 having five flip-flops whose outputs F_1 to F_5 permit of representing any number between 0 and 31 in binary form. The state 0 and the state of each flip-flop is translated as before by the absence or presence of a voltage at the terminals F . The terminal D_p sends the subtractive-counting pulses and the terminal E_p the additive counting pulses.

The terminals F are connected to the control stage in the same way as the terminals C of the computer of FIG. 1.

In addition, there are provided two gate circuits 13 and 14 disposed, respectively, between the subtractive-counting terminal D_p and the output of the flip-flop F_1 , and between the additive counting terminal E_p and the output of the flip-flop F_5 .

In this way, the "decrease" orders are not transmitted if the counter is empty in order that they may not pass from the zero value to the maximum value. Likewise, the "increase" orders are not transmitted if the counter is full, in order that it may not suddenly pass from the maximum value to the zero value.

Of course, the counter 15 may have more or less than five flip-flops, depending upon the required degree of fineness of the control for the mean value of the supply current of the apparatus.

I have shown and described several embodiments in accordance with the present invention. It is understood that the same is not limited thereto but is susceptible of numerous changes and modifications as known to a person skilled in the art and I, therefore, do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

I claim:

1. An apparatus for controlling the mean value of current supplied to a load device for a source of alternating current comprising:

current control means connected in series with said load device to said alternating current source for selectively connecting said load device to said alternating current source upon actuation thereof;

detector means connected to said alternating current source for producing an output pulse at each passage of the current from said source through a prescribed value to produce a series of clock pulses;

timing means including binary counter means having N stages for providing a plurality of output signals in 2^N combinations in synchronism with said clock pulses, and first gating means connected to said detector means and said binary counter means for passing N of said output signal combinations corresponding to 2^0 through 2^{N-1} connected to said detector means for generating N output signals in synchronism with said clock pulses where N is an integer, said output signals representing the combinations 2^0 through 2^{N-1} of a sequence 2^N consecutive pulses; and

control means selectively connecting at least one of said N output signals to said current control means for effecting periodic actuation thereof during each sequence of 2^N pulses.

2. An apparatus as defined in claim 1 wherein each stage of said counter means provides first or second complementary outputs, and said first gating means includes a first AND gate for each stage of said counter means, connected thereto so as to provide an output only when the first output of the stage corresponding thereto is the only first output provided by the stages of said counter means.

3. An apparatus as defined in claim 1 wherein said control means includes second gating means selectively connecting said N output signals to said current control means in one of 2^N combinations for controlling actuation thereof.

4. An apparatus as defined in claim 3 wherein said control means further includes gating control means selectively providing a control signal on N outputs in one of 2^N combinations for controlling operation of said second gating means.

5. An apparatus as defined in claim 4 wherein said second gating means includes N second AND gates, each connected to one output of said gating control means and one output of said first gating means, and an OR gate connected to each second AND gate and having its output connected to said cur-

rent control means.

6. An apparatus as defined in claim 4 wherein said gating control means includes computer means selectively providing first and second output and additional binary counter means having N stages providing N outputs in one of 2^N combinations as determined by the count registered therein, said first and second outputs of said computer means being connected to said additional binary counter means for increasing and decreasing the count thereof, respectively.

7. Apparatus for controlling the mean value of the current supplied to an electrical apparatus comprising an alternating current source and a rectifier device having a control electrode connected in series with the said apparatus, detector means connected to said current source for detecting the passage of the voltage generated thereby through a predetermined value and for emitting a pulse of calibrated value at each passage of the said value, computer means having N outputs capable of representing any number between 1 and 2^N , the adjustment of the mean value of the current passing through the said apparatus being effected in accordance with a program fed to the computer means by rendering the said rectifier device conductive for a number r of current cycles, each of a duration equal to T , distributed over a duration $2NT$, the value r being determined in accordance with the program established by said computer means, the output of the said detector means emitting calibrated pulses of period T being connected to the input of an electronic device comprising a first counter of the binary type having N bistable flip-flops each of which has a first output and a second output, and N AND circuits having 2, 3, ..., $N+1$ inputs, respectively, the N first inputs of the said AND circuits being connected to the output of said detector means, and the other inputs of each circuit being connected, respectively, to the first output of the flip-flop of like order and to the second outputs of the flip-flops of lower order having N outputs capable of producing at its respective outputs trains of pulses of periods $2T$, $4T$, ..., $2NT$ time-delayed in relation to the first calibrated pulse of the train of pulses of period T by times 0 , T , $2T$, $2^{N-1}T$ respectively, the N outputs of said electronic device being connected respectively to N first inputs of N AND circuits each having two inputs and one output, the N second inputs being connected respectively to the N outputs of said computer means, each of the outputs of the aforesaid N AND circuits being connected to each of the N inputs of an OR circuit whose output is connected to the control electrode of the aforesaid rectifier device.

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