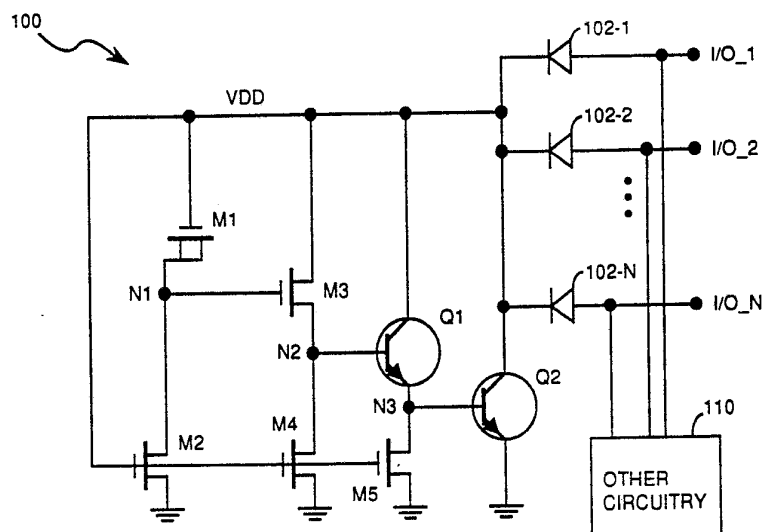




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification <sup>5</sup> : <b>H01L 27/02</b>	<b>A1</b>	(11) International Publication Number: <b>WO 92/16019</b> (43) International Publication Date: 17 September 1992 (17.09.92)
<p>(21) International Application Number: PCT/US92/01832</p> <p>(22) International Filing Date: 4 March 1992 (04.03.92)</p> <p>(30) Priority data: 665,386 5 March 1991 (05.03.91) US</p> <p>(71) Applicant: VLSI TECHNOLOGY, INC. [US/US]; 1109 McKay Drive, San Jose, CA 95131 (US).</p> <p>(72) Inventor: HUANG, Eddy, C. ; 1602 Dorcey Lane, San Jose, CA 95120 (US).</p> <p>(74) Agents: WILLIAMS, Gary, S. et al.; Flehr, Hohbach, Test, Albritton &amp; Herbert, 4 Embarcadero Center, Suite 3400, San Francisco, CA 94111-4187 (US).</p>		<p>(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), MC (European patent), NL (European patent), SE (European patent).</p> <p>Published <i>With international search report.</i></p>

## (54) Title: INPUT PROTECTION CIRCUIT FOR CMOS DEVICES



## (57) Abstract

A shared protection circuit (100) protects an MOS circuit (110), herein called a chip, from the destructive effects of electrostatic discharges conducted by any of the circuits input/output pins. The shared protection circuit is coupled to the high and low voltage source nodes used by the entire chip. In a preferred embodiment which protects against positive voltage electrostatic discharges, each input/output pin of the chip node is coupled by a diode (102) to the high voltage source node (VDD) so that a positive voltage transient on any input/output node will be transmitted to the high voltage source node. A Darlington pair of parasitic bipolar transistors (Q1, Q2) conduct charge from the high voltage source node (VDD) to the low voltage source node when turned on. A bias circuit turns on the Darlington pair of parasitic bipolar transistors when a positive voltage transient having at least a predefined magnitude occurs on the high voltage source node. As a result, the shared protection circuit will drain current from any input/output node, via the high voltage source node (VDD) when a positive voltage transient occurs thereon. The bias circuit also automatically turns off the Darlington pair of parasitic bipolar transistors (Q1, Q2) after it has discharged excess voltage from the high voltage source node (VDD).

*FOR THE PURPOSES OF INFORMATION ONLY*

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FI	Finland	MI	Mali
AU	Australia	FR	France	MN	Mongolia
BB	Barbados	GA	Gabon	MR	Mauritania
BE	Belgium	GB	United Kingdom	MW	Malawi
BF	Burkina Faso	GN	Guinea	NL	Netherlands
BG	Bulgaria	GR	Greece	NO	Norway
BJ	Benin	HU	Hungary	PL	Poland
BR	Brazil	IE	Ireland	RO	Romania
CA	Canada	IT	Italy	RU	Russian Federation
CF	Central African Republic	JP	Japan	SD	Sudan
CG	Congo	KP	Democratic People's Republic of Korea	SE	Sweden
CH	Switzerland	KR	Republic of Korea	SN	Senegal
CI	Côte d'Ivoire	LI	Liechtenstein	SU	Soviet Union
CM	Cameroon	LK	Sri Lanka	TD	Chad
CS	Czechoslovakia	LU	Luxembourg	TG	Togo
DE	Germany	MC	Monaco	US	United States of America
DK	Denmark	MG	Madagascar		
ES	Spain				

## INPUT PROTECTION CIRCUIT FOR CMOS DEVICES

The present invention relates to input protection circuits for protecting CMOS semiconductor devices from large electrostatic discharge voltages as well as input currents that may cause latchup.

5

### BACKGROUND OF THE INVENTION

The purpose of an input protection circuit is to protect input gates, diffusions, metal lines, and other internal components of a chip from the potentially destructive effects of large electrostatic discharge (ESD) voltages applied to an input pad. Input protection circuits are typically formed along the periphery of semiconductor circuits, generally next to the input pads of the circuit. In most prior art devices, a separate input protection circuit is coupled to each input node, and some such schemes require an extra ion implant step for input/output transistors to enhance their performance when subjected to an ESD.

10

15 Furthermore, the transistors in such input protection circuits typically must be large so as to be able to quickly absorb the current from an electrostatic discharge. As a result, such input protection circuits can occupy a sizeable amount of space, which increases the complexity and cost of the circuit.

The present invention provides a input protection circuit for CMOS devices that can be shared by many input/output nodes, thereby substantially reducing the complexity and amount of space occupied by input protection circuitry.

5

## SUMMARY OF THE INVENTION

In summary, the present invention is an input protection circuit for protecting MOS semiconductor circuits from electrostatic discharge voltages and from developing circuit latchup. More particularly, the present invention is a shared protection circuit which protects an MOS circuit, herein called a chip, from the destructive effects of electrostatic discharges conducted by any of the circuits input/output pins. Thus a single shared protection circuit can be used to protect against electrostatic discharges on all of the chip's input/output pins.

15 The shared protection circuit is coupled to the high and low voltage source nodes used by the entire chip. In a preferred embodiment which protects against positive voltage electrostatic discharges, each input/output pin of the chip is coupled by a diode to the high voltage source node so that a positive voltage transient on any input/output node will be transmitted to the high voltage source node. A Darlington pair of parasitic bipolar transistors conduct charge from the high voltage source node to the low voltage source node when turned on. A bias circuit turns on the Darlington pair of parasitic bipolar transistors when a positive voltage transient having at least a predefined magnitude occurs on the high voltage source node. As a result, the shared protection circuit will drain current from any input/output node, via the high voltage source node, when a positive voltage transient occurs. The bias circuit also automatically turns off the Darlington pair of parasitic bipolar transistors after it has discharged excess voltage from the high voltage source node.

## BRIEF DESCRIPTION OF THE DRAWINGS

Additional objects and features of the invention will be more readily apparent from the following detailed description and appended claims when taken in conjunction with the drawings, in which:

- 5
- Figures 1 and 2 schematically depict two preferred embodiments of an input protection device in accordance with the present invention.
- 10 Figure 3 depicts the profile and parasitic bipolar transistor model of the circuit shown in Figure 1.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

- 15 For the purposes of this description, the term VDD refers to the high voltage source used in a circuit (e.g., 5 volts in many circuits) and VSS refers to the low voltage source used in the circuit (e.g., 0 volts, or ground).

Referring to Figure 1, the input protection circuit 100 of the present invention is shown for an N-substrate CMOS circuit. The input protection circuit 100 can be placed anywhere on a CMOS integrated circuit chip so long as connections to both VDD and VSS are available. The purpose of the protection circuit 100 is to prevent high ESD voltages asserted on any I/O pin or node from reaching and destroying the circuits 110 internal to the chip that are coupled to those I/O nodes. More particularly, all the I/O nodes for the entire chip may be coupled to one protection circuit 100, which circuit provides the discharge path for all of the I/O nodes. Since each I/O node needs only to be coupled to the VDD node by a diode in order for it to be protected by the shared protection circuit 100, and VDD must be present in virtually every subcircuit in the chip, it is quite possible to use a single shared protection circuit for an entire chip. Alternately,

20

25

30

- 4 -

if it is difficult to connect all the I/O nodes to a single protection circuit 100 for any reason, a few such protection circuits may be used, each connected to a plurality of nearby I/O nodes.

5 The input protection circuit 100 is designed to protect against positive voltage electrostatic discharges because positive ESD's have been shown to cause the worst damage to the input/output (I/O) transistors in CMOS circuits. Each input/output node I/O\_1 to I/O\_N is coupled to the VDD node by a diode 102 so that a positive voltage static discharge asserted on any I/O pin or pad will  
10 be passed to VDD. Excess voltage on VDD is then discharged through the Darlington bipolar transistors Q1 and Q2. Transistors Q1 and Q2 are CMOS parasitic bipolar transistors.

Each diode 102 may be coupled to its corresponding I/O node by either a  
15 P-channel output transistor or by a connection to a P diffusion region that is connected to the I/O node.

Figure 1 shows a preferred embodiment of the ESD protection circuit for N-substrate CMOS circuits, while Figure 2 shows the preferred embodiment of  
20 the protection circuit of P-substrate CMOS circuits. In both circuits the devices whose labels begin with the letter "Q" are parasitic bipolar devices, and the devices whose labels begin with the letter "M" are MOS transistors that are used to form a bias circuit for the parasitic bipolar devices. That is, the MOS devices control when the parasitic bipolar devices turn on and off.

25 In the circuit of Figure 1, N-channel transistor M1 is used as a capacitor to couple positive going transients, caused by electrostatic discharges on any I/O node, from VDD to node N1. Transistor M3 is then turned on, bringing node N2 high to drive the base of parasitic transistor Q1, which in turn drives the base of Q2  
30 on node N3. The Darlington pair Q1-Q2 is now turned on to discharge the VDD

node to ground. The Darlington pair Q1-Q2 can be designed, using standard circuit design techniques, to strongly turn on when VDD reaches several volts above the normal VDD operating range.

5 Transistors M2, M4 and M5 are all low width-to-length devices which have little impact on the protection circuit's behavior during the discharging of transient voltages. In particular, transistors M2, M4 and M5 are used to discharge nodes N1, N2 and N3, respectively, after an ESD transient has been processed by the protection circuit. This allows the protected MOS circuit to resume normal  
10 operation without having to first power the chip down and then back on.

The ESD protection circuit 150 of Figure 2 works as follows. As in circuit 100 of Figure 1, N-channel transistor M1 is used as a capacitor to couple positive going transients from VDD to node N1. P-channel transistors M6 and M8 are  
15 used to keep bipolar parasitic transistors Q1 and Q2 off during the initial VDD rising transition by tracking nodes N4 and N5, which keeps Q1 from turning on. As in Figure 1, transistors M2 and M5 are used to discharge the internal nodes N1, N2 and N3 of the protection circuit 150 after an ESD transient has been processed.

20

Transistors M3, M4 and M7 are used to set the VDD trip point to turn on bipolar transistors Q1 and Q2. The VDD trip point is preferably set to several volts about the VDD normal operating range.

25 In both embodiments, more bipolar transistors can be cascaded to enable the protection circuit to absorb large ESD currents, if necessary. Furthermore, in both embodiments, the diodes 102 used to connect the I/O nodes to the protection circuit must be made sufficiently large so that these diodes do not become a bottleneck when the protection circuit is absorbing an ESD transient.

30 The output nodes of many CMOS circuits are already connected to large

P-channel transistors, which have large parasitic diodes connecting the output node to VDD. As a result, the required diode connections often already exist, at least for output nodes with large output driver circuits.

5 Under normal operation, VDD is at a nominal supply voltage and node N1 is pulled to ground (VSS) by transistor M2, which turns transistor M3 off. Bases of Q1 and Q2 are pulled low by transistors M4 and M5, respectively, in the protection circuit 100 of Figure 1. Bases of Q1 and Q2 are pulled high by transistors M6 and M8, respectively, in the protection circuit 150 of Figure 2.  
10 In both circuits the Darlington pair Q1-Q2 is turned off during normal operating conditions. Further, there is no danger of accidental turn-on of the Darlington pair during normal operation because a large VDD surge, typically more than 2.5 volts, is required to overcome the bipolar devices' base drive requirements. Thus a positive voltage transient having at least a predefined magnitude must  
15 occur on VDD before the Q1-Q2 will be turned on.

Referring to Figure 3, there is shown a circuit profile of the protection circuit of Figure 1, which is formed on a silicon N-substrate 160. The same labels are used for transistors M1-M5, nodes (I/O\_x, N1-N3, VDD, and VSS) and parasitic  
20 devices Q1-Q2 as in Figure 1. The N-channel transistors M1-M5 are formed in a first P-well 162, and the two parasitic bipolar transistors Q1-Q2 are formed in separate P-wells 164 and 166. It should be understood that the circuit profile shown is not drawn to scale, so that the relevant features can be more clearly  
25 represented. Furthermore, the parasitic bipolar devices Q1-Q2 shown in these profiles represent or model the operation of these circuits in certain circumstances - they do not represent additional components of the circuit. Since such parasitic structures are available on all CMOS chips, no modification of the manufacturing process is required in order to add the protection circuit of the present invention to such CMOS chips.  
30



While the present invention has been described with reference to a few specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

In particular, while the preferred embodiment of the present invention is designed to protect CMOS circuits against positive voltage ESD, anyone skilled in the art could use the teachings of the present invention to generate a "mirror image" version of the above described positive voltage ESD protection circuit, which would protect against negative voltage ESD. In particular, all the I/O nodes could be coupled by diodes to the VSS node, with a Darlington pair of bipolar parasitic transistors being used to supply current to the VSS node in the case of a negative voltage ESD. By putting both the positive voltage ESD and negative voltage ESD circuits on the same CMOS chip, the chip would be protected against both positive and negative voltage electrostatic discharges.

## WHAT IS CLAIMED IS:

1. In an MOS semiconductor circuit, a shared protection circuit coupled to a plurality of input/output pads and to other circuitry in the MOS semiconductor circuit, said shared protection circuit comprising:

5 first and second voltage source nodes, one of said voltage sources node comprising a high voltage source node and the other comprising a low voltage source node;

10 a multiplicity of diodes, each coupling a distinct input/output node to said first voltage source node so that a transient voltage of a predefined polarity on any input/output node is transmitted to said first voltage source node; and

15 a Darlington pair of parasitic bipolar transistors, coupled to said first and second voltage source nodes so as to conduct charge from said first voltage source node to said second voltage source node when a transient voltage of said predefined polarity having at least a predefined magnitude occurs on said first voltage source node;

20 whereby said shared protection circuit will drain current from any of said input/output nodes, via said first voltage source node, when a transient voltage of said predefined polarity occurs thereon.

2. The shared protection circuit of Claim 1, wherein said circuit is formed in a semiconductor substrate of a first type and said Darlington pair of parasitic bipolar transistors comprise vertical bipolar structures formed in a well of semiconductor material of opposite type.

25 3. The shared protection circuit of Claim 1, including a bias circuit for turning on said Darlington pair of parasitic bipolar transistors when a transient voltage of said predefined polarity having at least said predefined magnitude occurs on said first voltage source node; said bias circuit including means for automatically  
30 turning off said Darlington pair of parasitic bipolar transistors after said Darlington

pair of parasitic bipolar transistors has drained current from said first voltage source node.

4. In an MOS semiconductor circuit, a shared protection circuit coupled to  
5 a plurality of input/output pads and to other circuitry in the MOS semiconductor circuit, said shared protection circuit comprising:

a high voltage source node and a low voltage source node;

a multiplicity of diodes, each coupling a distinct input/output node to said  
high voltage source node so that a positive voltage transient on any input/output  
10 node is transmitted to said high voltage source node; and

a Darlington pair of parasitic bipolar transistors, coupled to said high  
voltage source node and a low voltage source node so as to conduct charge  
from said high voltage source node to said low voltage source node when a  
positive voltage transient occurs on said high voltage source node;

15 whereby said shared protection circuit will drain current from any of said  
input/output nodes, via said high voltage source node, when a positive voltage  
transient occurs thereon.

5. The shared protection circuit of Claim 4, wherein said circuit is formed  
20 in a semiconductor substrate of a first type and said Darlington pair of parasitic  
bipolar transistors comprise vertical bipolar structures formed in a well of  
semiconductor material of opposite type.

6. The shared protection circuit of Claim 4, including a bias circuit for turning  
25 on said Darlington pair of parasitic bipolar transistors when a positive voltage  
transient having at least a predefined magnitude occurs on said high voltage  
source node; said bias circuit including means for automatically turning off said  
Darlington pair of parasitic bipolar transistors after said Darlington pair of parasitic  
bipolar transistors has drained current from said high voltage source node.

30

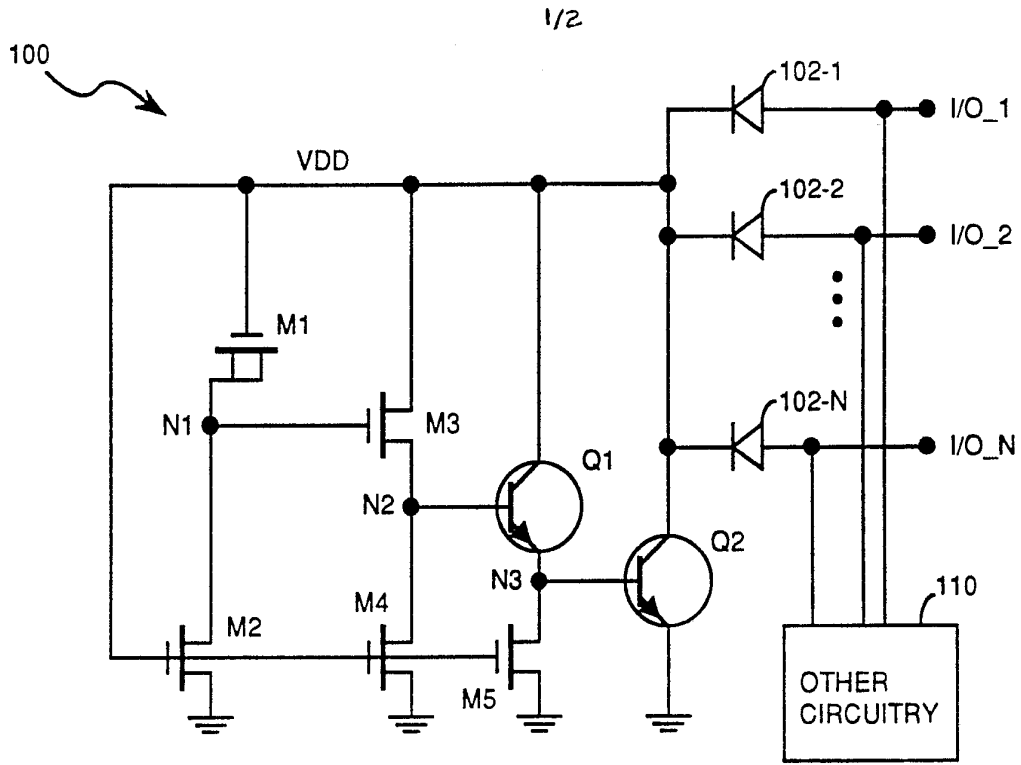


FIGURE 1 ✓

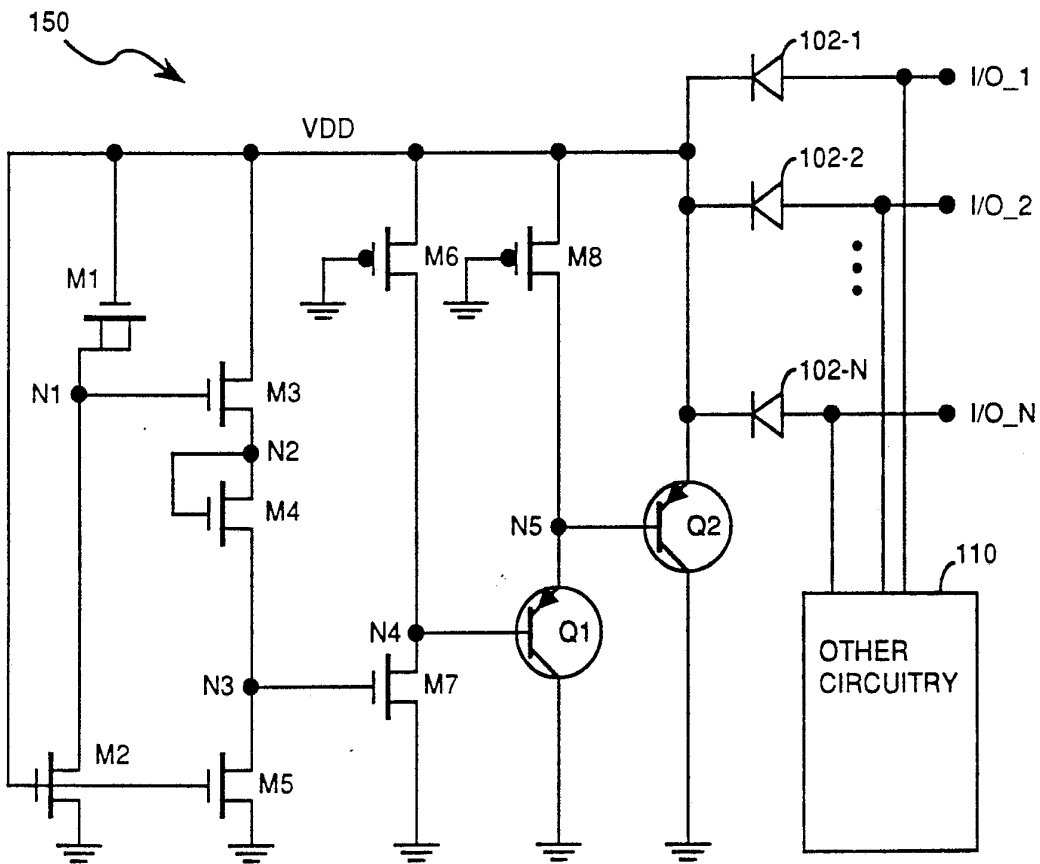


FIGURE 2

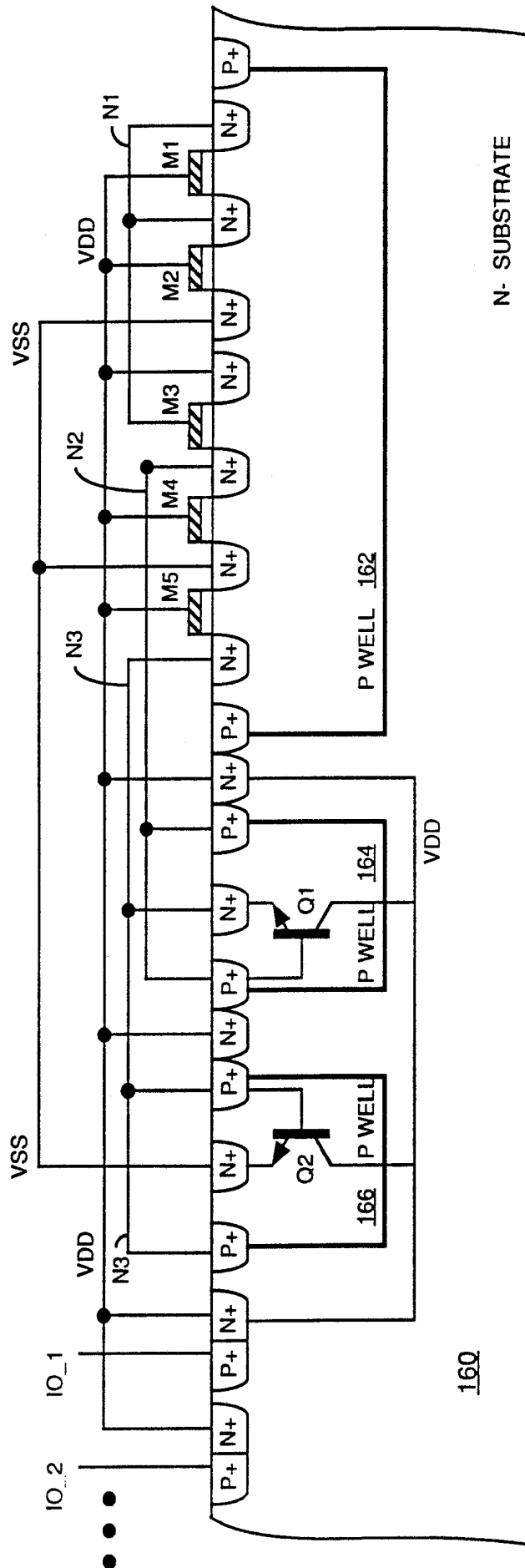


FIGURE 3

# INTERNATIONAL SEARCH REPORT

International Application No. **PCT/US92/01832**

**I. CLASSIFICATION OF SUBJECT MATTER** (if several classification symbols apply, indicate all) \*

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): **H01L 27/02**

U.S. CL.: **357/43**

**II. FIELDS SEARCHED**

Minimum Documentation Searched <sup>7</sup>

Classification System

Classification Symbols

U.S.

357/43

Documentation Searched other than Minimum Documentation  
to the Extent that such Documents are Included in the Fields Searched <sup>8</sup>

**III. DOCUMENTS CONSIDERED TO BE RELEVANT <sup>9</sup>**

Category <sup>10</sup>	Citation of Document, <sup>11</sup> with indication, where appropriate, of the relevant passages <sup>12</sup>	Relevant to Claim No. <sup>13</sup>
A	US, A, 4,888,623 (ENOMOTO ET AL.) 19 December 1989, See the entire document.	1-6
A	US, A, 4,918,563 (KANAI ET AL.) 17 April 1990, See the entire document.	1-6

\* Special categories of cited documents: <sup>16</sup>

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

**IV. CERTIFICATION**

Date of the Actual Completion of the International Search

Date of Mailing of this International Search Report

17 JUNE 1992

02 JUL 1992

International Searching Authority

Signature of Authorized Officer

ISA/US

*Robert E. Wise*  
ROBERT E. WISE