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(54) Title: SYSTEMS AND METHODS FOR IMPROVED DELAMINATION CHARACTERISTICS IN A SEMICONDUCTOR PACKAGE

(57) Abstract: Systems and methods are provided for producing an integrated circuit package, e.g., an SOIC package, having reduced or eliminated lead delamination caused by epoxy outgassing resulting from the die attach process in which an integrated circuit die is attached to a lead frame by an epoxy. The epoxy outgassing may be reduced by heating the epoxy during or otherwise in association with the die attach process, e.g. using a heating device provided at the die attach unit. Heating the epoxy may achieve additional cross-linking in the epoxy reaction, which may thereby reduce outgassing from the epoxy, which may in turn reduce or eliminate subsequent lead delamination. A heating device located at or near the die attach site may be used to heat the epoxy to a temperature of 55 °C ± 5 °C during or otherwise in association with the die attach process.

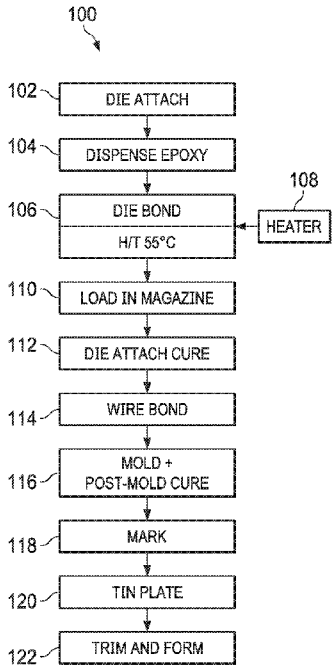

FIG. 1

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[Continued on next page]

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SYSTEMS AND METHODS FOR IMPROVED DELAMINATION CHARACTERISTICS IN A SEMICONDUCTOR PACKAGE

RELATED PATENT APPLICATION

This application claims priority to commonly owned United States Provisional Patent Application No. 62/489,869 filed April 25, 2017, which is hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

The present disclosure relates to semiconductor manufacturing, e.g., to systems and methods for providing improved delamination characteristics in a semiconductor package (e.g., providing reduced or eliminated delamination of a lead frame lead and/or DAP region) by reducing epoxy outgassing during the die attach process.

BACKGROUND

Many conventional integrated circuit ("IC") packages suffer from delamination after exposure to certain environmental conditions for an amount of time. For example, many IC packages experience delamination after the moisture loading requirement of 85°C & 85% humidity for a duration of 168 hours, as specified by JEDEC MSL ("Moisture Sensitivity Level") testing. As used herein, "delamination" may refer to a separation between areas of the lead frame (which may be silver plated, in some devices) and an adjacent structure or material (e.g., mold compound or die/IC chip), which may result from poor adhesion between the lead frame and the adjacent structure or material, for example. Delamination may affect the IC packaging, resulting in package and wire bond weaknesses during reliability testing, such as when stress is applied to the package, e.g., due to moisture, temperature or humidity. Delamination may also result in product field failures such as broken or lifted wire bonds.

Thus, there is a need for reducing or eliminating lead frame delamination in IC packages, e.g., SOIC (Small Outline Integrated Circuit) packages. As an example only, there is a need for reducing or eliminating lead frame delamination, e.g., inner lead delamination, in 8-lead SOIC (SOIC-8) and 28-lead SOIC (SOIC-28) semiconductor device housings. The

JEDEC requirement (JEDEC J-STD-020E) mandates zero delamination on wire bonding areas using palladium coated copper wire at MSL 1, which rating indicates that the devices is not moisture sensitive. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag). One way to reduce or eliminate the leadfinger delamination is to downgrade the devices to MSL3, which rating defines a maximum of one week exposure to ambient conditions before the device is assembled on a PCB. However, this typically adds substantial cost to the parts and requires special handling of the parts by the customer when removing the parts from moisture barrier bags.

SUMMARY

Many IC packages, such as SOIC (Small Outline Integrated Circuit) packages for example, suffer from lead frame delamination, e.g., inner lead delamination, during package qualification testing. The inventors have determined that a significant cause of such lead delamination is epoxy outgassing resulting from the die attach process, in which an epoxy is deposited on the lead frame pad and the IC die is mounted on the epoxy-covered area of the lead frame pad to thereby secure the die to the lead frame.

The present invention provides systems and methods that reduce or eliminate lead delamination caused by epoxy outgassing resulting from the die attach process. In some embodiments, SOIC packages produced using such systems and/or methods may qualify to CuPdAu wire with zero lead delamination. This may provide increased cost savings and produce high quality products using CuPdAu wire.

In some embodiments, the epoxy outgassing is reduced by heating the epoxy during or otherwise in association with the die attach process, e.g. using a heating device provided at the die attach unit. Heating the epoxy may achieve additional cross-linking in the epoxy reaction, which may thereby reduce outgassing from the epoxy, which may in turn reduce or eliminate subsequent lead delamination. In some embodiments, a heating device is used to heat the epoxy to a temperature of 55 °C ± 5 °C during or otherwise in association with the die attach process.

One embodiment provides a method for manufacturing an integrated circuit device including an integrated circuit chip mounted on a die support area of a lead frame, wherein the method includes (a) performing a die attach process to form an integrated circuit structure, the

die attach including depositing epoxy on at least a portion of the die support area of the lead frame, mounting the integrated circuit chip over the epoxy-covered die support area such that a portion of the epoxy extends laterally outside of an outer perimeter of the integrated circuit chip, and using a heating device to apply heat during the mounting step; (b) after the die attach process, performing a die attach cure process on the integrated circuit structure; (c) performing a wire bond process to bond at least one wire to the integrated circuit structure; and (d) applying a molding material to at least partially encapsulate the integrated circuit structure.

In one embodiment, the heating step comprises heating the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy as compared with an integrated circuit device produced according to a similar production processes but without the die attach heating step.

In one embodiment, the heating step is configured reduce a measure of outgassing from the epoxy by a factor of at least three as compared with an integrated circuit device produced according to a similar production processes but without the die attach heating step.

In some embodiments, the heating step comprises using the heating device to heat the epoxy to a temperature of 55 °C ± 15 °C. In some embodiments, the heating step comprises using the heating device to heat the epoxy to a temperature of 55 °C ± 10 °C. In some embodiments, the heating step comprises using the heating device to heat the epoxy to a temperature of 55 °C ± 5 °C. In some embodiments, the heating step comprises using the heating device to heat the epoxy to a temperature of about 55 °C.

In one embodiment, the die attach process includes: using a feeding device to carry the lead frame to an epoxy dispensing station; at the epoxy dispensing station, depositing the epoxy on the die support area of the lead frame; using the feeding device to carry the lead frame with deposited epoxy to a chip mounting station, the chip mounting station having an associated heater; and at the chip mounting station: mounting the integrated circuit chip over the epoxy-covered die support area, and using the heater to apply heat to at least the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy.

Another embodiment provides a system for manufacturing an integrated circuit device, the system including a loading unit configured to position a lead frame on a machine feeder,

the lead frame including a die support area and a plurality of leads; the machine feeder configured to deliver the lead frame to an epoxy dispensing unit and to a die attach unit; wherein the epoxy dispensing unit is configured to deposit epoxy on at least a portion of the die support area of the lead frame; and wherein the die attach unit includes a mounting unit configured to mount the integrated circuit chip over the epoxy-covered die support area, and a die attach heating unit configured to apply heat to at least the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy.

In one embodiment, the die attach heating unit is configured to reduce outgassing from the epoxy as compared with an integrated circuit device produced without heating the epoxy in association with the die attach.

In one embodiment, the die attach heating unit is configured to reduce a measure of outgassing from the epoxy by a factor of at least three as compared with an integrated circuit device produced without heating the epoxy in association with the die attach.

In one embodiment, the die attach heating unit is configured to heat the epoxy to a temperature of about 55 °C.

In one embodiment, the die attach heating unit is configured to heat the epoxy to a temperature of 55 °C ± 10 °C.

In one embodiment, the die attach heating unit is configured to heat the epoxy to a temperature of 55 °C ± 5 °C.

BRIEF DESCRIPTION OF THE FIGURES

Example aspects of the present disclosure are described below in conjunction with the figures, in which:

Figure 1 illustrates an example assembly process for producing an integrated circuit (IC) device/package having improved lead delamination characteristics (e.g., reduced or eliminated lead delamination), according to one example embodiment.

Figure 2 illustrates an example system for facilitating a heated die attach process, e.g., using the example process shown in Figure 1, according to one embodiment.

Figure 3 illustrates an example embodiment of a lead frame advancing through an epoxy dispensing device followed by a pick-and-place device having an associated heater for providing a heated die bonding process, according to one embodiment.

Figure 4 illustrates an example reliability test flow for example lots of IC packages formed using systems and methods disclosed herein (including heating the die attach epoxy before, during and/or after the die attach), according to one embodiment.

Figure 5A and 5B illustrate differences between an example IC package formed according to conventional techniques (Figure 5A) and an example IC package formed using systems and methods disclosed herein (Figure 5B), e.g., including heating the die attach epoxy before, during and/or after the die attach.

DESCRIPTION

Figure 1 illustrates an example assembly process 100 for producing an integrated circuit (IC) device/package having improved lead delamination characteristics (e.g., reduced or eliminated lead delamination), according to one example embodiment. The lead delamination characteristics of the resulting IC package may be improved by adding a heating step to the die attach (D/A) process. At 102, a die attach (D/A) process is performed to attach an integrated circuit die (e.g., chip) to a lead frame. A lead frame may be loaded onto a machine feeder, e.g., a moving belt or track, and delivered to an epoxy dispensing unit. At 104, the epoxy dispensing unit may deposit epoxy on at least a portion of an upper surface of a lead frame, e.g., on a portion of a lead frame pad configured to receive the IC die.

The machine feeder may then deliver the epoxy-covered lead frame to a die bond unit, which may include a die mounting device and a heating device. At 106, the die mounting device mounts the die onto the epoxy-covered area of the lead frame pad, and a heating device 108 heats the region of the epoxy to achieve additional cross-linking in the epoxy reaction, which may thereby reduce outgassing from the epoxy, which may in turn reduce or eliminate lead delamination from the produced IC package. The heating device 108 may operate before,

during, and/or after the mounting of the IC chip to the epoxy-covered lead frame pad. In some embodiments, the heating device 108 may heat the epoxy to a temperature of about 55 °C, or 55 °C ± 10 °C, or 55 °C ± 5 °C during or otherwise in association with the die attach process at 106.

At 110, the lead frame and IC chip structure may then be loaded into a magazine by a loading device, to complete the die attach process. A die attach cure may then be performed on the structure at 112, using any known techniques. A wire bond process may then be performed at 114, e.g., to connect the IC chip to one or more lead frame leads adjacent the lead frame pad. In some embodiments, CuPdAu bond wire may be used. A mold compound may then be applied to the IC structure at 116, e.g., to at least partially encapsulate the structure, and a post mold cure (PMC) process may be performed, using any known techniques. The IC structure, which may include any number of lead frames and IC chips mounted thereon, may then be marked at 118 and cut at 120-112 to provide a plurality of discrete IC packages.

Figure 2 illustrates an example system 100 for facilitating a heated die attach process, e.g., using method 100 discussed above, according to one embodiment. System 100 may include an input/loader 202, a machine feeder 204, and an output/unloader 206. Input/loader 202 may be configured to load a lead frame 230 onto an automated conveyor or track 210, which may carry the lead frame 230 to the machine feeder 204. Lead frame 230 may include a die pad 232 and a plurality of lead fingers 234. In some embodiments, a top surface of each lead finger 234, e.g., a tip region 236 or other region(s) of each lead finger 234, may be silver-coated and/or physically roughened by a roughening process, e.g., to increase a bonding between a subsequently deposited molding compound and the lead frame 230.

Machine feeder 204 may include an epoxy dispensing device 212 and a pick-and-place device 214. Epoxy dispensing device 212 may dispense an epoxy 216 onto the lead frame pad 232. The lead frame 230 may then be advanced to the pick-and-place device 214, which may pick and place an integrated circuit (IC) chip or die 250 onto the epoxy-covered portion of the lead frame pad 232, to thereby bond the IC die 250 the pad 232.

A heater 220 may be provided at or near the location of this die bond process, e.g., embodied integral with or separate from the pick-and-place device 214. Heater 220 may be

configured to heat the epoxy 216 before, during, and/or after the mounting of the IC die 250 to the epoxy-covered lead frame pad 232 by pick-and-place device 214, to improve the epoxy-based die attach bond. For example, the heated die bond may achieve additional cross-linking in the epoxy reaction, which may thereby reduce outgassing from the epoxy, which may in turn reduce or eliminate lead delamination from the produced IC package. Heater 22 may heat the epoxy 216 to any suitable temperature to improve one or more characteristics of the epoxy bond. For example, in some embodiments, heater 22 may heat the epoxy 216 to a temperature of about 55 °C; or 55 °C ± 15 °C; or 55 °C ± 10 °C; or 55 °C ± 5 °C during or otherwise in association with the die attach process.

Heater 220 may include any system or device suitable for directly or indirectly heating the epoxy 216 on the lead frame die pad 232, e.g., a convective heater, a radiant heater, a heating cable, a forced air heater, or a conductive heater physically coupled to the lead frame 230 (e.g., at die pad 232). Heater 220 may be powered by electricity, natural gas, propane, solar energy, or any other energy source.

After the heated die attach process, the lead frame 230 with the attached and epoxy-bonded IC chip 250, indicated as bonded unit 240, may be advanced on track 210 to an output/unloading device 206, which may unload the bonded unit 240 for further processing, e.g., encapsulation by a mold compound.

Figure 3 illustrates an example embodiment of lead frame 230 advancing through epoxy dispensing device 212 followed by pick-and-place device 214 having an associated heater 220 for providing a heated die bonding process, e.g., to heat the epoxy 216 before, during, and/or after the mounting of IC chip 250 to the lead frame pad 232. In the example embodiment shown in Figure 3, heater 220 is located at the die bond site. For example, heater 22 may be arranged at an opening between sections 210A and 210B of track 210 that carries and advances lead frame 230 through the die attach system. Track section 210A may advance lead frame 230 through epoxy dispensing device 212, where a mass of epoxy 216 is deposited onto the lead frame pad 232, and then to a location at which lead frame pad 232 is aligned over heater 220, as shown in Figure 3. At this location, heater 220 may heat the epoxy 216 (e.g., to a temperature of about 55 °C; or 55 °C ± 15 °C; or 55 °C ± 10 °C; or 55 °C ± 5 °C) and pick-and-place device 214 may mount the IC chip 250 onto the epoxy-covered region of the lead frame

pad 232. Heater 220 may be controlled (e.g., automatically or manually) to heat the epoxy 216 before, during, and/or after the IC die 250 is physically mounted to the lead frame pad 232 by pick-and-place device 214.

In other embodiments, heater 220 may be arranged below a continuous section of track 210, and at the die bond site. In other embodiments, heater 220 may be arranged above the lead frame 230. For example, heater 220 may be arranged above and laterally offset from lead frame pad 232, to provide room for pick-and-place device 214 to mount the die 250 to pad 232.

In other embodiments, heater 220 may be arranged upstream of the bond site. For example, heater 220 may be located above, below, or integrated in the track 210 at a location upstream of the bond site. Track 210 may advance lead frame pad 232 to a location directly above or below the heater 220, where heater 220 may be operated to heat the epoxy 216 to a target temperature. Track 210 may then advance the lead frame with heated epoxy 216 to the bond site, wherein pick-and-place device 214 may then mount the die 250 onto the heated epoxy 216 on pad 232.

Figure 4 illustrates an example reliability test flow 400 for example lots of IC packages formed using systems and methods disclosed herein, e.g., including heating the die attach epoxy before, during and/or after the die attach. At 402, scanning acoustic imaging (SAM) of a lot of IC packages is performed. At 404, the lot is baked for 24 hours at 150°C. At 406, a moisture soak is performed on the lot, for 168 hours at 85°C and 85% relative humidity. At 408, the lot is subjected to 3x reflow at 260°C. The lot is then imaged by SAM and inspected for delamination or other defects.

Table 1 shows relevant parameters for example lots of IC packages formed using systems and methods disclosed herein and tested according to process 400 shown in Figure 4.

Table 1. Parameters regarding tested IC packages

Die Information	
Wafer tech.	200K
Die size	60.50 x 89.20 mils
Die thickness	15 mils
BPO	82 µm
Die to DAP (die attach pad) ratio	35.95% (for 95 x 158 mils pad) 43.69 (for 95 x 130 mils pad)
BOM Information	
Lead frame	Ag ring+BOT
Epoxy	8390A
Wire	CuPdAu, 0.8 mils
Compound	G600V

Table 2 shows testing results of six lots of IC packages characterized by the information in Table 1 and tested according to process 400 shown in Figure 4. As shown, all lots showed no delamination after the test flow process.

Table 2. IC package test results

Lot #	Package	LF pad size	Cure type	Wafer tech	Top dap	Top lead	Result
1	8L SOIC	95x130	Oven	200K	0/45	0/45	No delamination
2	8L SOIC	95x158	Oven	200K	0/45	0/45	No delamination
3	8L SOIC	95x158 (low Ag thk)	Oven	200K	0/45	0/45	No delamination
4	8L SOIC	95x130	Snap	200K	0/45	0/45	No delamination
5	8L SOIC	95x158	Snap	200K	0/45	0/45	No delamination
6	8L SOIC	95x158 (low Ag thk)	Snap	200K	0/45	0/45	No delamination

Figures 5A and 5B illustrate differences between an example IC package 500A formed according to conventional techniques (Figure 5A) and an example IC package 500B formed

using systems and methods disclosed herein (Figure 5B), e.g., including heating the die attach epoxy before, during and/or after the die attach. Each example IC package 500A, 500B includes a lead frame 502 including a die pad 504 and lead fingers 506, and an IC die/chip 510 mounted to the lead frame pad 504 by an epoxy 514A, 514B. As shown in Figure 5A, in the conventional IC package 500A, the average distance of epoxy outgassing 512A (beyond the outer edge of the epoxy 514A) may be about or greater than 3x the average distance of epoxy bleed out. In contrast, as shown in Figure 5B, in the example IC package 500B according to the present invention, the average distance of epoxy outgassing 512B (beyond the outer edge of the epoxy 514B) may be less than 1x the average distance of epoxy bleed out.

Although the disclosed embodiments are described in detail in the present disclosure, it should be understood that various changes, substitutions and alterations can be made to the embodiments without departing from their spirit and scope.

CLAIMS

WHAT IS CLAIMED IS:

1. A method for manufacturing an integrated circuit device including an integrated circuit chip mounted on a die support area of a lead frame, the method comprising:

performing a die attach process to form an integrated circuit structure, the die attach including:

depositing epoxy on at least a portion of the die support area of the lead frame;

mounting the integrated circuit chip over the epoxy-covered die support area such that a portion of the epoxy extends laterally outside of an outer perimeter of the integrated circuit chip; and

using a heating device to apply heat during the mounting step;

after the die attach process, performing a die attach cure process on the integrated circuit structure;

performing a wire bond process to bond at least one wire to the integrated circuit structure; and

applying a molding material to at least partially encapsulate the integrated circuit structure.

2. The method of claim 1, wherein the heating step comprises heating the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy as compared with an integrated circuit device produced according to a similar production processes but without the die attach heating step.

3. The method of any of claims 1 or 2, wherein the heating step is configured reduce a measure of outgassing from the epoxy by a factor of at least three as compared with an integrated circuit device produced according to a similar production processes but without the die attach heating step.

4. The method of any of claims 1-3, wherein the heating step comprises using the heating device to heat the epoxy to a temperature of about 55 °C.

5. The method of any of claims 1-3, wherein the heating step comprises using the heating device to heat the epoxy to a temperature of 55 °C ± 10 °C.

6. The method of any of claims 1-3, wherein the heating step comprises using the heating device to heat the epoxy to a temperature of 55 °C ± 5 °C.

7. The method of any of claims 1-6, wherein the die attach process includes:

using a feeding device to carry the lead frame to an epoxy dispensing station;

at the epoxy dispensing station, depositing the epoxy on the die support area of the lead frame;

using the feeding device to carry the lead frame with deposited epoxy to a chip mounting station, the chip mounting station having an associated heater;

at the chip mounting station:

mounting the integrated circuit chip over the epoxy-covered die support area; and

using the heater to apply heat to at least the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy.

8. A system for manufacturing an integrated circuit device, the system comprising:

a loading unit configured to position a lead frame on a machine feeder, the lead frame including a die support area and a plurality of leads;

the machine feeder configured to deliver the lead frame to an epoxy dispensing unit and to a die attach unit;

wherein the epoxy dispensing unit is configured to deposit epoxy on at least a portion of the die support area of the lead frame;

wherein the die attach unit includes:

a mounting unit configured to mount the integrated circuit chip over the epoxy-covered die support area; and

a die attach heating unit configured to apply heat to at least the epoxy to achieve additional cross-linking in the epoxy reaction and reduce outgassing from the epoxy.

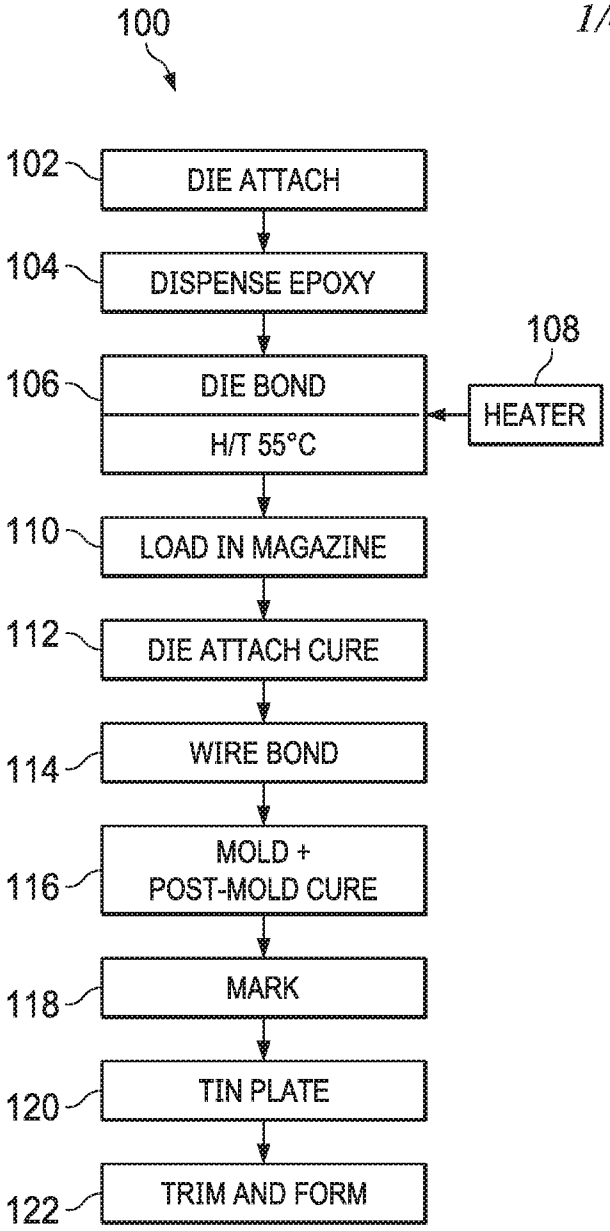
9. The system of claim 8, wherein the die attach heating unit is configured to reduce outgassing from the epoxy as compared with an integrated circuit device produced without heating the epoxy in association with the die attach.

10. The system of any of claims 8-9, wherein the die attach heating unit is configured to reduce a measure of outgassing from the epoxy by a factor of at least three as compared with an integrated circuit device produced without heating the epoxy in association with the die attach.

11. The system of any of claims 8-10, wherein the die attach heating unit is configured to heat the epoxy to a temperature of about 55 °C.

12. The system of any of claims 8-10, wherein the die attach heating unit is configured to heat the epoxy to a temperature of 55 °C ± 10 °C.

13. The system of any of claims 8-10, wherein the die attach heating unit is configured to heat the epoxy to a temperature of 55 °C ± 5 °C.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102
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HEATER
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112
DIE ATTACH CURE
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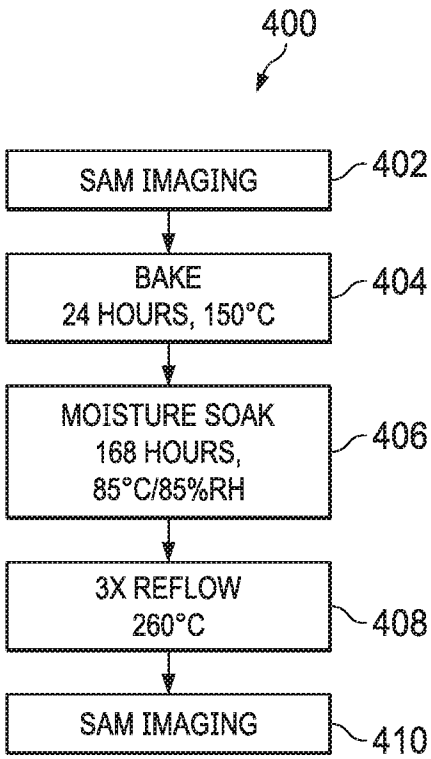
WIRE BOND
116
MOLD +
POST-MOLD CURE
118
MARK
120
TIN PLATE
122
TRIM AND FORM

FIG. 1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402
BAKE
24 HOURS, 150°C
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MOISTURE SOAK
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85°C/85%RH
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3X REFLOW
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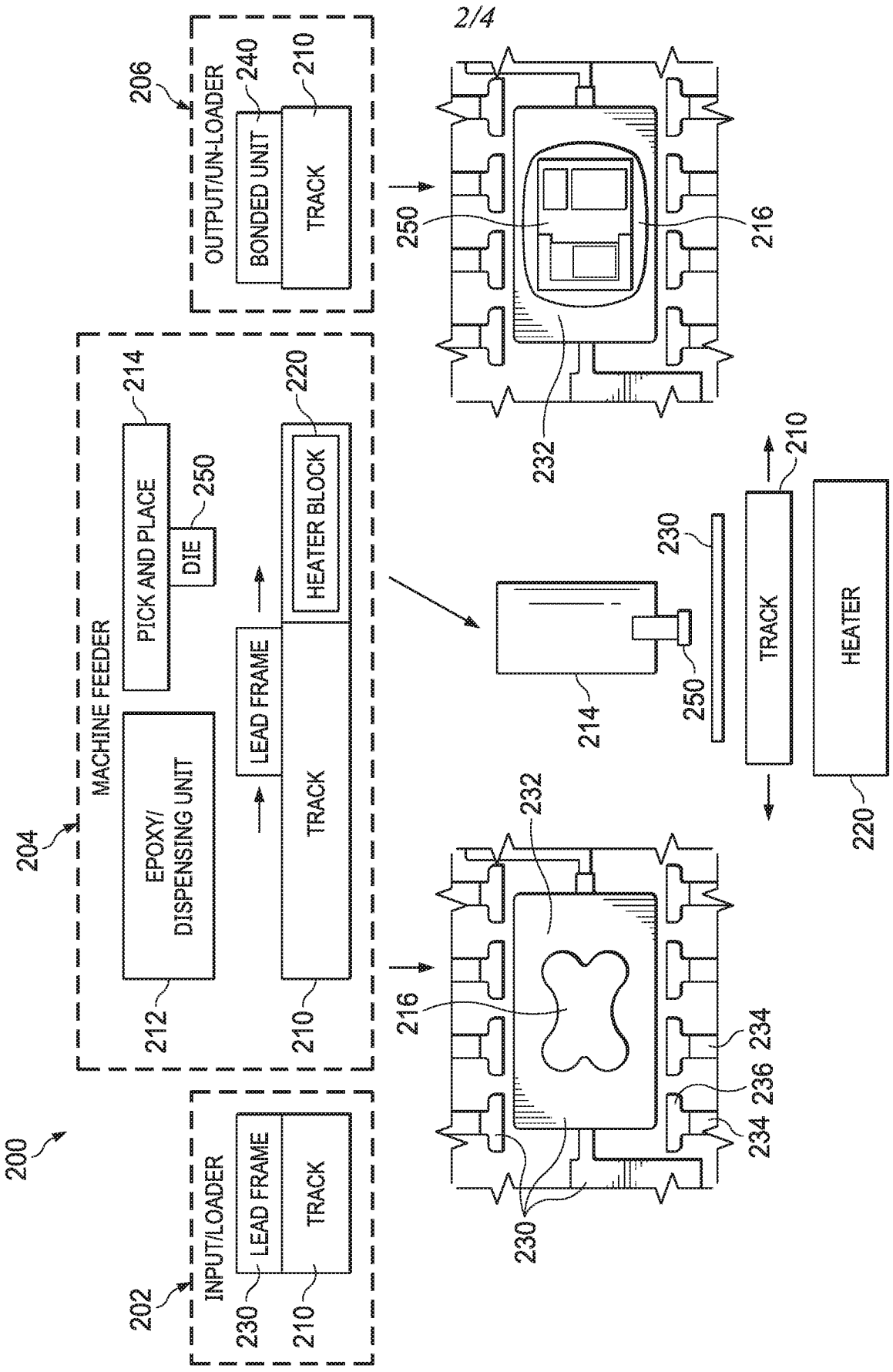
408
SAM IMAGING
410

FIG. 4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202
LEAD FRAME
230
TRACK
210
MACHINE FEEDER
204
EPOXY/
DISPENSING UNIT
212
PICK AND PLACE
214
DIE
250
LEAD FRAME
TRACK
210
HEATER BLOCK
220
OUTPUT/UN-LOADER
206
BONDED UNIT
240
TRACK
210
250
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232
230
214
250
TRACK
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HEATER
220
232
216
234
236
234
230

FIG. 2

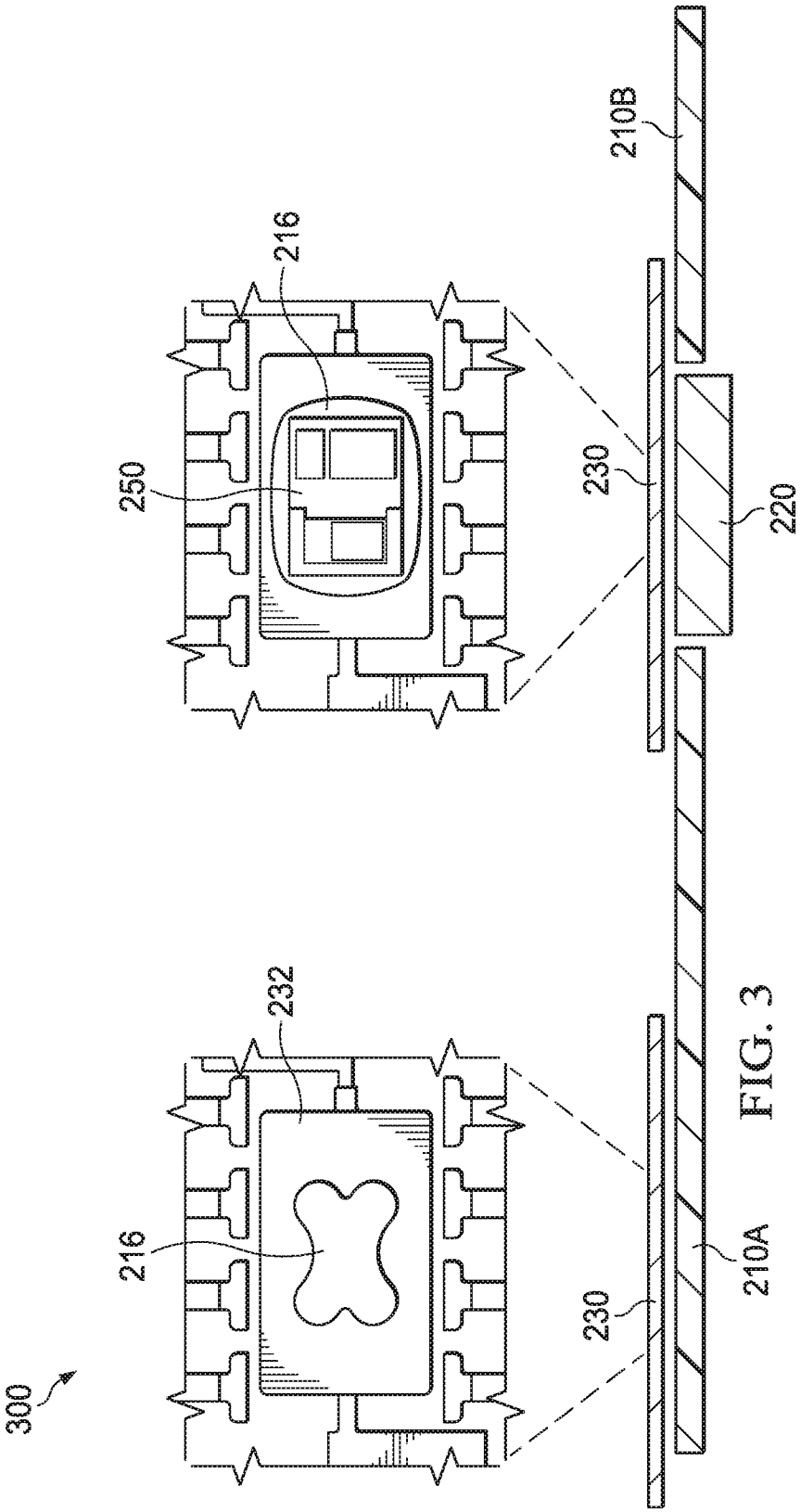

FIG. 3

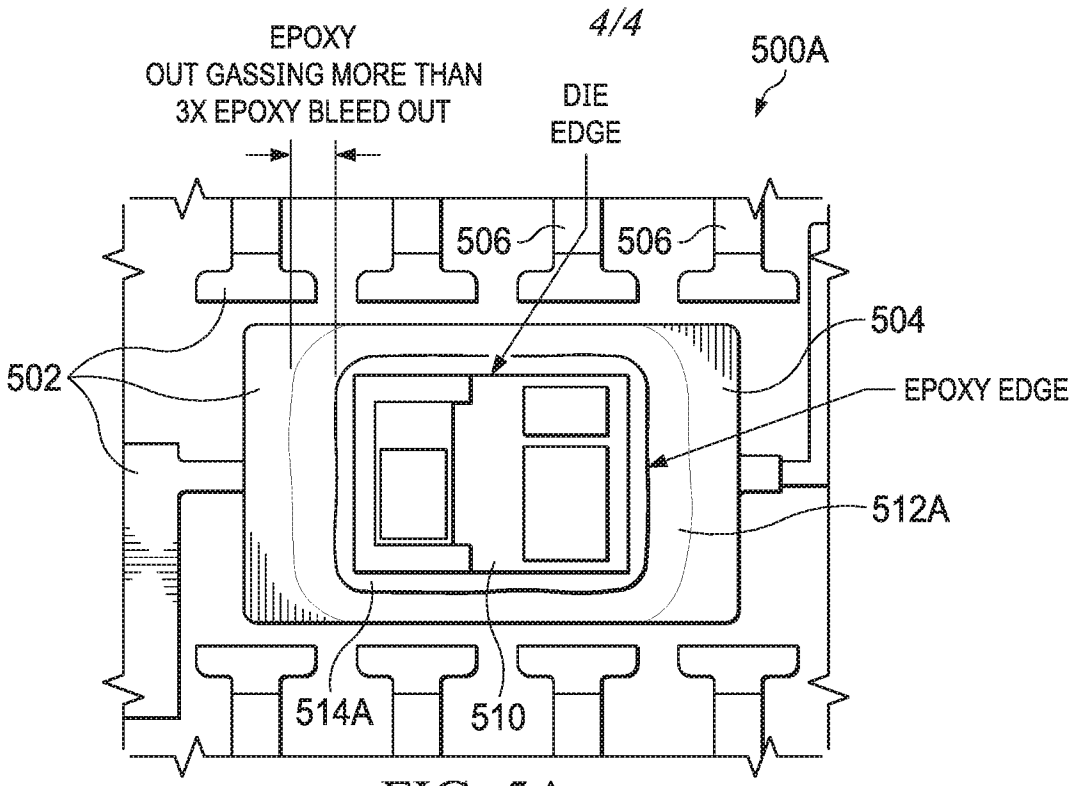

FIG. 5A
(PRIOR ART)

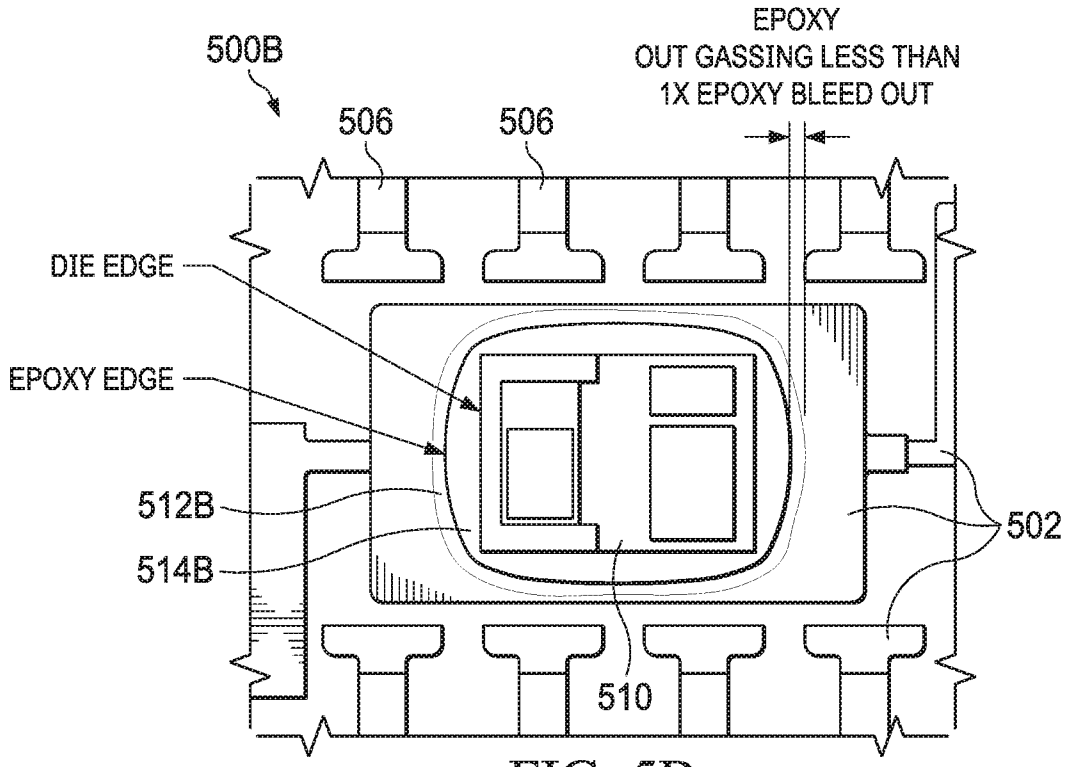

FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/029259

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/58
ADD. H01L21/67

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 223 800 B1 (KIM SEONG-BONG [KR] ET AL) 1 May 2001 (2001-05-01) column 2, line 33 - column 4, line 3 column 4, line 59 - column 5, line 37; figure 3 column 5, line 38 - column 7, line 14; figures 4-8	8-13

X	US 6 110 805 A (SCHROCK ED [US] ET AL) 29 August 2000 (2000-08-29)	1-6
A	column 1, line 11 - column 2, line 31 column 2, line 49 - column 4, line 51; figure 1 column 4, line 52 - column 5, line 38; figure 2	8

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 July 2018	30/07/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Corchia, Alessandra

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 960 491 B2 (CHIPMOS TECHNOLOGIES INC [BM]) 1 November 2005 (2005-11-01) column 1, lines 13-54 column 3, line 8 - column 4, line 56; figures 4A-4F, 5 column 5, lines 4-6	1-7
A	EP 2 387 067 A1 (NAGASE CHEMTEX CORP [JP]) 16 November 2011 (2011-11-16) paragraphs [0002] - [0005], [0008], [0009] paragraphs [0025] - [0038]	1-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/029259

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