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(54) **TRIPLE LAYER HARD MASK FOR GATE PATTERNING TO FABRICATE SCALED CMOS TRANSISTORS**

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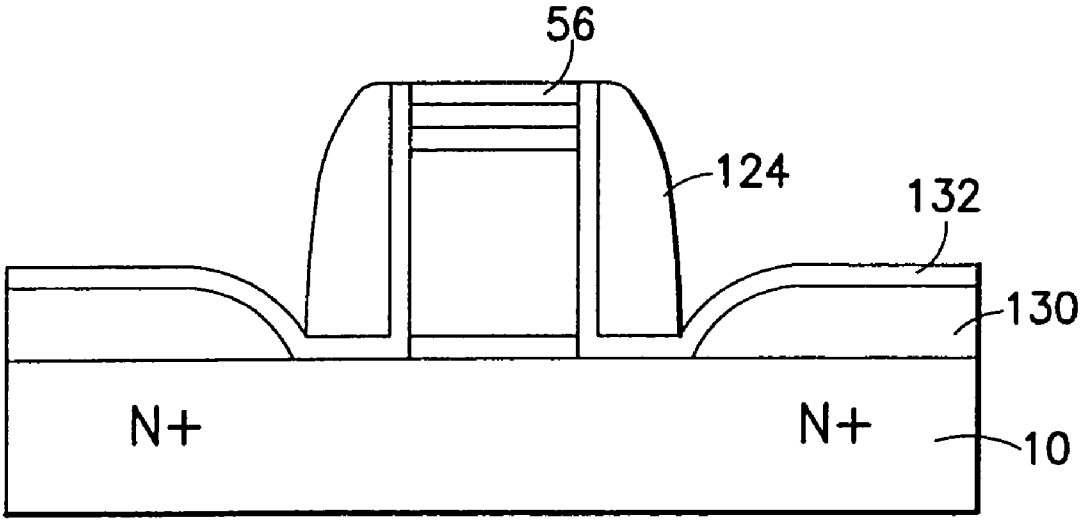
(57) **ABSTRACT**

An integrated circuit employing CMOS technology employs a process integration that combines a source/drain silicide with a replacement gate process using a triple layer hard-mask that is consumed during the course of processing in which a first temporary gate sidewall spacer defines an area for the formation of the raised source and drain and a second temporary spacer defines an area for the implant of the source and drain and for the siliciding of the source and drain while the temporary gate is protected from silicidaiton by the hardmask.



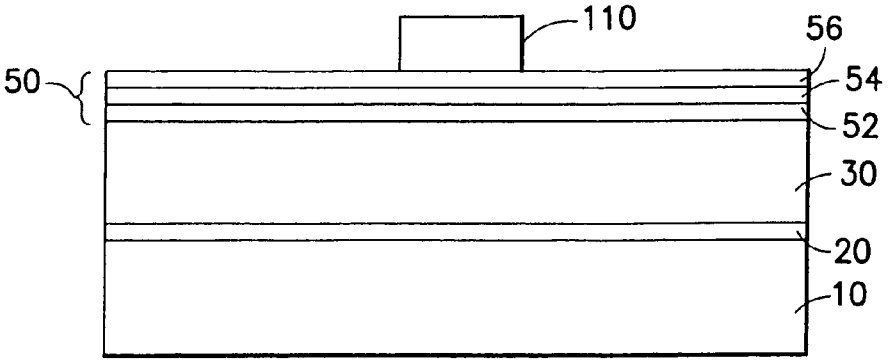


FIG. 1

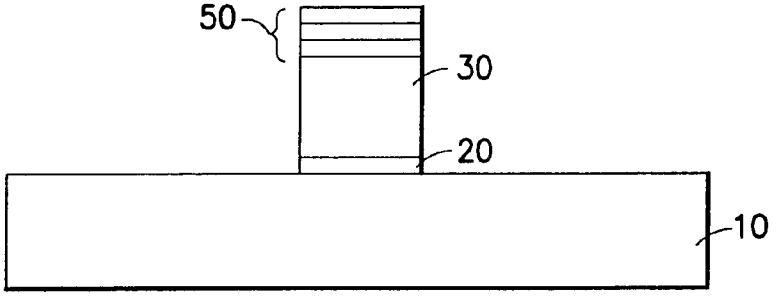


FIG. 2

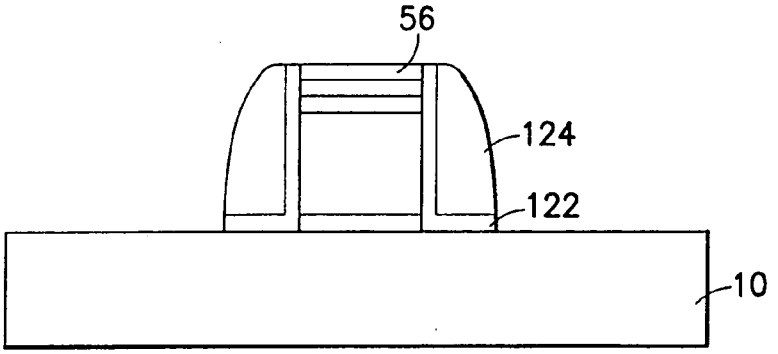


FIG. 3

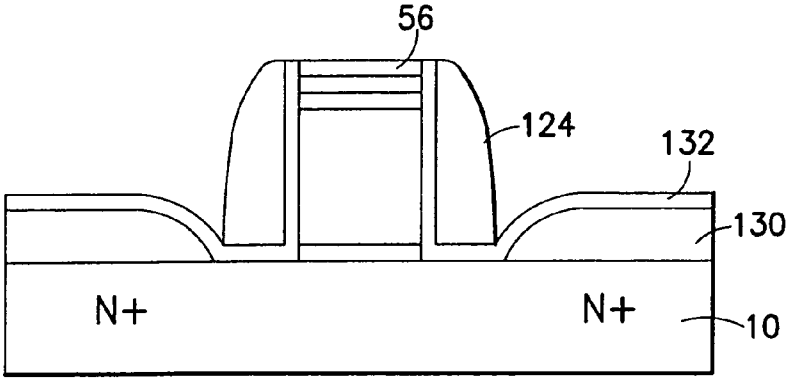


FIG. 4

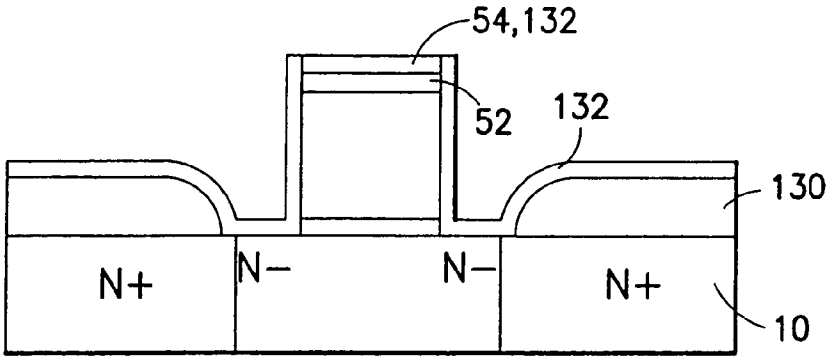


FIG.5

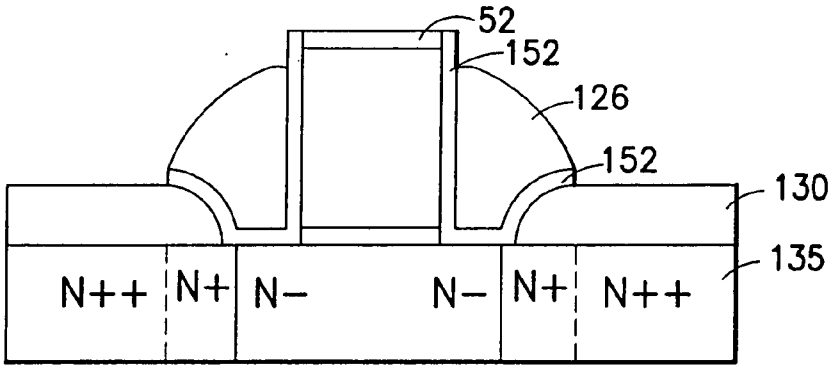


FIG.6

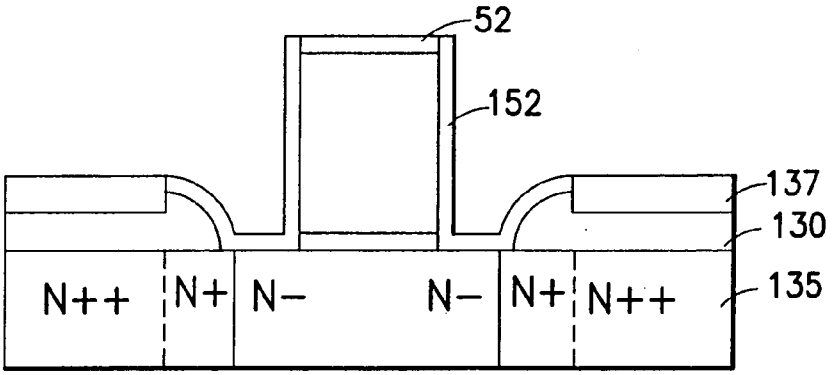


FIG.7

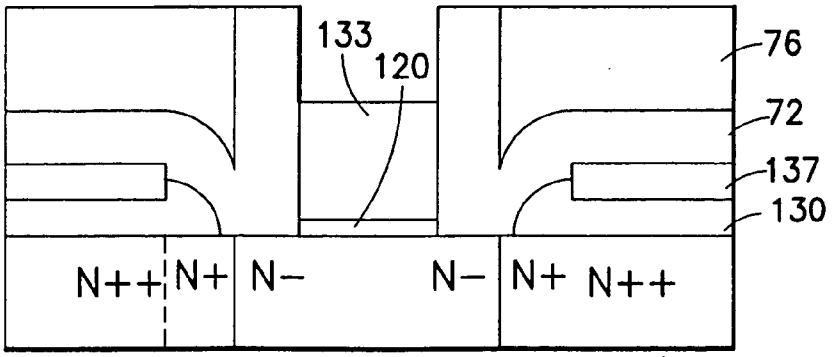


FIG.8

TRIPLE LAYER HARD MASK FOR GATE PATTERNING TO FABRICATE SCALED CMOS TRANSISTORS

TECHNICAL FIELD

[0001] The field of the invention is that of CMOS processing, in particular integration of the process for fabricating integrated circuits.

BACKGROUND OF THE INVENTION

[0002] As dimensions shrink in integrated circuit processing, vertical dimensions shrink as well as transverse ones—i.e. the layers that make up the integrated circuit become thinner.

[0003] The result of this is that various steps that were straightforward in larger-dimension processing become more difficult.

[0004] For example, the dimensions of devices in the near future are expected be less than 100 nm and the gate dielectric in a field effect transistor is expected to be of material having a higher dielectric constant than silicon dioxide (SiO2, oxide). Unfortunately, such materials are less thermally stable than oxide, so that the permissible exposure of the device to high temperatures is even more limited than it is with oxide gate insulators.

[0005] It is nevertheless necessary to expose the wafer, and thus the materials within the transistors, to temperatures in excess of one thousand degrees Centigrade in order to activate the source and drain diffusions of the transistors. Most high-k dielectrics can not withstand exposure to such temperatures for the durations required.

[0006] Further, the use of metal gates (e.g. Tungsten, Tantalum Silicon Nitride (TaSiN), Tantalum Nitride (TaN)) is accepted as being necessary for adequate transistor performance.

[0007] Such gates require a sacrificial gate process, independently of whether the gate dielectric does. In a sacrificial gate process, the transistor is constructed with a dummy, or sacrificial, gate during the steps such as providing alignment of the sources and drains with the gate structure. After activating the source and drain, the sacrificial gate material is removed and the high-k gate dielectric and/or the metal gate material are deposited.

[0008] Those skilled in the art are aware that no removal process is one hundred per cent efficient, and there will inevitably be removal of extra material, so that the final dimensions of the gate will not be exactly as desired.

[0009] In addition, in the case of silicon on insulator wafers, the thickness of the silicon device layer decreases, and there is not enough material in the thickness of the layer to be consumed (e. g. less than about 50 nm of silicon) in the process of forming a silicide for higher conductivity and better performance.

[0010] Those skilled in the art are aware that raised sources and drains provide extra thickness only in the sources and drains, while retaining the desired dimension elsewhere.

[0011] Although various aspects of the foregoing considerations are known to those skilled in the art, there remains a considerable problem of process integration to make all the process steps produce the desired final result.

[0012] It is not enough to combine a step from one solution to a given problem with a step from another solution to another problem if the different steps are mutually exclusive or otherwise conflict.

[0013] In integrated circuit processing at the 70 nm node, it is accepted in the art that a sacrificial gate process is necessary. In such a process, the transistor structure is formed

SUMMARY OF THE INVENTION

[0014] The invention relates to a process for forming a CMOS transistor in a silicon on insulator wafer that combines a sacrificial gate process with a raised source and drain.

[0015] In one embodiment of the invention, a three layer hardmask protects the gate stack during subsequent processing.

[0016] In one embodiment of the invention, two disposable spacers are used to define the area for the raised source/drain and to block an ion implant into the raised source/drain.

[0017] In another embodiment of the invention, the hard mask prevents the formation of silicide on the top of the gate stack.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** illustrates in cross section a CMOS transistor being formed in a SOI wafer, at a preliminary stage in the process.

[0019] **FIG. 2** illustrates the same area after the gate stack has been patterned.

[0020] **FIG. 3** illustrates the same area after forming temporary sidewalls.

[0021] **FIG. 4** illustrates the same area after forming the raised sources and drains.

[0022] **FIG. 5** illustrates the same area after stripping the temporary sidewalls and implanting the lightly doped portions of the sources and drains.

[0023] **FIG. 6** illustrates the same area after encapsulating the gate stack with nitride and depositing the final sidewalls.

[0024] **FIG. 7** illustrates the area after forming a planarizing layer and cmp.

[0025] **FIG. 8** illustrates the area after removal of the sacrificial gate.

DETAILED DESCRIPTION

[0026] **FIG. 1** illustrates in cross section a CMOS transistor being formed in a wafer, which may be either SOI or bulk silicon) at a preliminary stage in the process. At the stage shown, silicon substrate **10** has a gate oxide layer **20** formed on it, with a blanket layer of polycrystalline silicon (poly) **30** on top of that. Oxide **20** will be removed in this area, but is a thermal oxide that may be used as a gate oxide in other portions of the integrated circuit. Poly layer **30** will be used to form the sacrificial gate in this process.

[0027] Above poly layer **30**, there is a hard mask layer **50**, comprising sublayers of silicon nitride (Si3N4—nitride) **52** (30 nm thick), oxide **54** (15 nm thick), and a second or upper layer of nitride (30 nm thick). Block **110** represents a patterned photoresist or other etch mask that defines the width of the gate stack in the following gate etch.

[0028] In this application, the Nitride/Oxide/Nitride stack layer is used as a hard mask for the polysilicon gate. This structure allows raised source/drain formation prior to formation of the LDD extension of the source and drain step and effectively blocks forming silicide during that step of the conventional CMOS process.

[0029] **FIG. 2** shows the gate stack after the directional patterning etch, illustratively a reactive ion etch, which has used appropriate chemistry, changing it as necessary to remove all of the hardmask **50** and then, using the top nitride layer **56** of the hard mask for definition, to pattern the poly layer **30** and the gate oxide **20** by removing those portions of the poly and oxide layers outside the gate stack, stopping on substrate **10**.

[0030] **FIG. 3** shows the result of forming a conformal layer of oxide **122** that encapsulates the gate stack. This layer of oxide protects the gate stack during the formation of disposable nitride spacer **124**, which is used in a subsequent step of forming a raised source and drain. After the deposition of the layer that forms spacers **124** (nominally 30 nm of nitride), a directional etch removes the horizontal portions of the nitride in layer **124** and also the oxide in layer **122**. The structure shown in this figure will be referred to as the expanded stack. The structure of hardmask **50** is unchanged, as the oxide layer **122** on the top of hardmask **50** has been removed during the process of spacer definition.

[0031] **FIG. 4** shows the area after a process of epitaxial deposition of silicon to form raised source and drain layers **130**. Illustratively, silicon **130** is grown in a selective process that increases the thickness only where silicon is exposed; i.e. in which the silicon does not adhere to nitride or oxide. The silicon formation is followed by growth of a thin layer of thermal oxide **132** that protects the new source/drain extension during the subsequent nitride strip.

[0032] Referring now to **FIG. 5**, nitride spacer **124** has been removed, exposing an area adjacent to the expanded gate stack that will be implanted to form the LDD source/drain extension. Advantageously, the vertical portion of oxide layer **122** that was between spacers **124** and the gate stack protects the bottom nitride **52** of hardmask **50** during the nitride stripping step. The remaining portion of oxide **122** that was underneath spacer **124** has been removed in a directional etch that does not substantially attack oxide layer **54** in the hardmask.

[0033] The LDD implant, in this case N^-, is made adjacent to the gate stack.

[0034] **FIG. 6** shows the area after the deposition of a thin layer of nitride **152** on top of the earlier hardmask layer **52** and extending horizontally, and formation of a second spacer **126** of oxide. Nitride **152** is stripped over the source and drain, in a process that preserves enough nitride **52** over the top of the gate stack to block silicide formation there. A silicidation process forms a silicide **137** on the raised source and drain, but not on the top of the gate stack. This protection from silicidation by bottom nitride **52** permits easier removal of the gate stack in the later step of removing the gate.

[0035] In the case where the wafer is a silicon on insulator wafer, whether bonded or implanted, similar considerations to those that drive those skilled in the art to shrink device dimensions also drive a reduction in thickness. In particular, fully depleted devices benefit from a reduction in the the thickness of the silicon device layer in which the bodies of transistors are formed. When the device layer becomes too thin, however, being less than about 50 nm in contemporary technology, the amount of silicon in the area of the wafer that is the source and/or drain is not sufficient to form a silicide film having sufficent thickness to be acceptable. In such a case, the addition of a step of raising the source and drain by depositing additional silicon in that area is beneficial. In the case of a wafer or circuit using SiGe technology, the additional raised source and drain may be SiGe, but does not need to be.

[0036] A second source/drain implant dose implants the raised source/drain and increases the doping of the lower N^+ portion of the source /drain to the conventional concentration of N^{++}. Spacers **126** block this implant over the inner area labeled N^- and the intermediate area that has been implanted N^+, producing an implant gradation from $^-$ adjacent to the gate stack, increasing to N^+ in the next region and then to N^{++} under the silicide. Such a three-step process is preferred, but not necessary and the conventional two-step gradation of the lightly doped LDD region and the heavily doped source and drain may also be used.

[0037] As shown in **FIG. 7**, the oxide spacer **126** (and the intermediate layer **54** of the hardmask) is stripped, leaving nitride **152** over the gate stack. A thermal treatment to activate the implanted dopants may be performed at any convenient time after the N^{++} implant and before the final gate dielectric and gate are put down.

[0038] A blanket deposition of a relatively thick layer of nitride **72** for an etch stop and oxide **76**, for isolation of the conductive members in the local interconnect, forms a thick layer that is reduced by conventional chemical-mechanical polishing (CMP) to the level of the top of the gate stack. The final layer **52** of the hardmask may be polished away during this step, illustratively in a process that uses the exposure of poly **30** in the temporary gate as a signal to stop the polishing. If such a process is not used, the remaining portion of layer **52**/**152** is stripped, exposing the poly **30** in the gate.

[0039] A poly etch removes gate **30**, leaving an aperture lined with layer **152**. Layer **152** may be left in place or stripped. The last removal step is an oxide etch to remove the sacrificial gate oxide **20**. Optionally, if the design calls for a final gate dielectric of oxide, the stripping of the gate oxide may be omitted. A new gate dielectric, which may be a high-k material such as Hafnium Silicon Nitride (HfSiN), Hafnium Oxygen Nitride (HfON) or Hafnium oxide (HfO2) or any other suitable material, is put down and a new gate is deposited. The new gate may be chosen from a number of alternatives, such as Tungsten, Tantalum Silicon Nitride (TaSiN), Tantalum Nitride (TaN). The residue of the two foregoing steps is removed from the top of layer **76**, for example by chemical-mechanical polishing. The new gate may preferably fill the aperture left by the old gate, though

that is not required. It may be preferable in some circumstances to fill the aperture partially and use the remaining space for a contact.

[0040] This process is applied to CMOS transistors of both polarities, NFETs and PFETS. The substrate **10** can be bulk silicon, SiGe and/or SOI, with or without a SiGe top layer.

[0041] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

1. A method of forming a integrated circuit comprising at least one field effect transistor comprising the steps of:

preparing a semiconductor substrate;

forming a first dielectric layer on said substrate;

forming a sacrificial gate layer above said first dielectric layer;

forming a hardmask layer, comprising at least two hardmask sublayers, above said sacrificial gate layer;

forming a gate stack by patterning said hardmask layer, sacrificial gate layer and first dielectric layer;

forming first protective sidewalls about said gate stack;

forming a raised source/drain structure outside said first protective sidewalls;

implanting source/drain extensions within said raised source/drain structure;

forming silicide over said raised source/drain structure while said gate stack is covered by said hardmask;

forming isolation dielectric, planarized to the level of said gate stack, about said gate stack;

removing said sacrificial gate layer within said gate stack, thereby forming a gate aperture;

removing said first dielectric layer in said gate aperture;

depositing a final gate dielectric in said gate aperture; and

depositing a final gate layer in said gate aperture.

2. A method according to claim 1, in which:

said hardmask comprises a top layer of nitride and a layer of oxide below said top layer of nitride;

said first protective sidewalls are composed of nitride;

said first protective sidewalls and said top layer of nitride are removed after said step of forming said raised source/drain structure; and

a step of oxide removal is performed before said step of siliciding that cleans said raised source/drain structure and simultaneously removes said oxide hardmask layer.

3. A method according to claim 1, in which:

a step of removing said first protective sidewalls and said top layer of nitride is performed before said step of implanting said source/drain extensions.

4. A method according to claim 1, in which:

a step of forming second protective gate sidewalls is performed after said step of implanting said source/drain extensions, which second protective gate sidewalls extend out to fill the area over said source/drain extensions, whereby said second protective gate sidewalls define the area for said silicide.

5. A method according to claim 2, in which:

a step of forming second protective gate sidewalls is performed after said step of implanting said source/drain extensions, which second protective gate sidewalls extend out to fill the area over said source/drain extensions, whereby said second protective gate sidewalls define the area for said silicide.

6. A method according to claim 3, in which:

a step of forming second protective gate sidewalls is performed after said step of implanting said source/drain extensions, which second protective gate sidewalls extend out to fill the area over said source/drain extensions, whereby said second protective gate sidewalls define the area for said silicide.

7. A method according to claim 1, in which:

a conformal oxide layer is formed that encapsulates said gate stack before said step of forming said first protective gate sidewalls.

8. A method according to claim 2, in which:

a conformal oxide layer is formed that encapsulates said gate stack before said step of forming said first protective gate sidewalls.

9. A method according to claim 3, in which:

a conformal oxide layer is formed that encapsulates said gate stack before said step of forming said first protective gate sidewalls.

10. A method according to claim 4, in which:

a conformal oxide layer is formed that encapsulates said gate stack before said step of forming said first protective gate sidewalls.

11. A method according to claim 4, in which:

a conformal nitride layer is formed that encapsulates said gate stack before said step of forming said second protective gate sidewalls.

12. A method according to claim 5, in which:

a conformal nitride layer is formed that encapsulates said gate stack before said step of forming said second protective gate sidewalls.

13. A method according to claim 6, in which:

a conformal nitride layer is formed that encapsulates said gate stack before said step of forming said second protective gate sidewalls.

14. A method according to claim 4, in which:

said oxide layer in said hardmask is removed when said second protective gate sidewalls are removed.

15. A method according to claim 5, in which:

said oxide layer in said hardmask is removed when said second protective gate sidewalls are removed.

16. A method according to claim 6, in which:

said oxide layer in said hardmask is removed when said second protective gate sidewalls are removed.

17. An integrated circuit comprising a semiconductor substrate and a set of field effect transistors formed therein, said field effect transistors comprising a raised source and drain covered with a layer of silicide;

a gate dielectric other than thermally grown silicon oxide;

a gate electrode deposited over said gate dielectric after removal of a temporary gate electrode, said gate electrode having a top surface at a height above said substrate that differs from said layer of silicide over said source and drain.

18. An integrated circuit according to claim 17, in which said gate electrode is selected from the group comprising Tungsten, Tantalum Silicon Nitride and Tantalum Nitride.

19. An integrated circuit according to claim 17, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

20. An integrated circuit according to claim 17, in which said semiconductor substrate is a silicon on insulator substrate having a silicon device layer of thickness less than 50 nm disposed over an insulating layer.

21. An integrated circuit according to claim 17, in which said gate dielectric is formed after said silicide.

22. An integrated circuit according to claim 17, in which said gate dielectric is formed from a material having a dielectric constant greater than a dielectric constant of silicon oxide.

23. An integrated circuit according to claim 21, in which said gate dielectric is formed from a material having a dielectric constant greater than a dielectric constant of silicon oxide.

24. An integrated circuit according to claim 21, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

25. An integrated circuit according to claim 22, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

26. An integrated circuit according to claim 23, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

27. An integrated circuit according to claim 21, in which said gate electrode is selected from the group comprising Tungsten, Tantalum Silicon Nitride and Tantalum Nitride.

28. An integrated circuit according to claim 22, in which said gate electrode is selected from the group comprising Tungsten, Tantalum Silicon Nitride and Tantalum Nitride.

29. An integrated circuit according to claim 20, in which said gate dielectric is formed after said silicide.

30. An integrated circuit according to claim 20, in which said gate dielectric is formed from a material having a dielectric constant greater than a dielectric constant of silicon oxide.

31. An integrated circuit according to claim 29, in which said gate dielectric is formed from a material having a dielectric constant greater than a dielectric constant of silicon oxide.

32. An integrated circuit according to claim 29, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

33. An integrated circuit according to claim 30, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

34. An integrated circuit according to claim 31, in which said gate dielectric is selected from the group comprising Hafnium Silicon Nitride, Hafnium Oxygen Nitride, or Hafnium oxide.

35. An integrated circuit according to claim 32, in which said gate electrode is selected from the group comprising Tungsten, Tantalum Silicon Nitride and Tantalum Nitride.

36. An integrated circuit according to claim 30, in which said gate electrode is selected from the group comprising Tungsten, Tantalum Silicon Nitride and Tantalum Nitride.

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