A frequency multiplier (100) comprising cascaded first (105) and second (110) stages. The first stage (105) generates an output signal comprising harmonics of an AC input signal. The second stage (110) comprises N bipolar/FET transistors (115, 120, 125), arranged to receive the output signal from the first stage at their base/gate and to be biased by a base/gate bias voltage \(V_{gs1}, V_{gs2}, V_{gs3}\). Each of said N transistors delivers at its collector/drain a signal with a frequency at a unique multiple of the frequency of the input signal, the base/gate bias voltages being chosen to generate said multiple. Each transistor in the second stage is connected to a frequency filter (130, 135, 140) adapted to optimize the frequency of the output signal for that transistor.

Fig 1
A NOVEL FREQUENCY MULTIPLIER

TECHNICAL FIELD
The present invention discloses a novel frequency multiplier.

BACKGROUND
Frequency multipliers are components which are often used in such applications as, for example, telecommunications systems, radar systems and other systems which utilize electromagnetic signals.

Often, frequency multipliers are desired which can generate a number of multiples of the input frequency, where the lowest multiple is sometimes referred to as the fundamental or the first harmonic, and subsequent multiples are referred to as the second, third...etc harmonic.

Known kinds of frequency multipliers include frequency multipliers which utilize transistors or optoelectronic oscillators, the latter sometimes with tunable multiplication factors. However, optoelectronic oscillators with tunable multiplication factors are not suitable for implementations in, for example, microwave monolithic integrated circuits, MMICs. Frequency multipliers which utilize transistors often exhibit different phase noise performance for signals at different frequencies.

SUMMARY
It is an object to obtain a frequency multiplier which obviates the disadvantages of the frequency multipliers described above, and to also obtain a frequency multiplier which simultaneously can generate more than one signal at a multiple of an input signal's frequency, i.e. several output signals each at differing frequency multiples of the input signal's frequency.
This object is obtained by means of a frequency multiplier which comprises a first and a second stage connected in series with each other, where the first stage is arranged to receive an input AC signal and to generate an output signal comprising harmonics of said input AC signal and to deliver said output signal to the second stage.

In the frequency multiplier, the second stage comprises integer \( N \) bipolar/FET transistors, each of which is arranged to receive the output signal from the first stage at its base/gate and to be biased by means of a base/gate bias voltage, each of which transistors has its emitter/source grounded. In the frequency multiplier's second stage, the base/gate bias voltage of each of the \( N \) transistors is different from that of every other of said \( N \) transistors, and each of the \( N \) transistors is arranged to deliver at its collector/drain a signal at a frequency which is a multiple of the frequency of the input signal, said multiple being unique for each transistor by virtue of the differing base/gate bias voltages being chosen so as to generate an output signal from the transistor in which said multiple is at a maximum value.

Each of the \( N \) transistors in the second stage has its collector/drain connected to one of \( N \) frequency filters, with the frequency filter for each transistor being specific for that transistor in that the frequency filter of each transistor is adapted to let the multiple which is generated by that transistor be the dominant frequency in the output signal from the filter. Each of the frequency filters has an output port which is arranged to be one of \( N \) output ports of the frequency multiplier.

In embodiments of the frequency multiplier, the size of each of said \( N \) transistors differs from the size of each of the other of \( N \) transistors. The size of the transistors is for bipolar transistors determined by the number of
emitter fingers and the length of each finger, and for FET transistors by the number of gate fingers and the width of the gate fingers.

In embodiments of the frequency multiplier, the base/gate bias voltage of the N transistors increases for increasing frequency multiples.

In embodiments of the frequency multiplier, the size of each of said N transistors is kept constant or decreases for increasing frequency multiples.

In embodiments of the frequency multiplier, in which the base/gate bias voltage and size of each of the N transistors is obtained by means of sweeping all combinations of bias voltages in a range of $V_1$-$V_2$ and all transistor sizes in a range of $L_1$-$L_2$, and for each of the N transistors, the combination of bias voltage and transistor's size is chosen which gives the maximum conversion gain for the desired frequency multiple.

BRIEF DESCRIPTION OF THE DRAWINGS
The invention will be described in more detail in the following, with reference to the appended drawings, in which

Fig 1 shows an embodiment of a frequency multiplier, and
Fig 2 shows the frequency spectrum at a point between the two stages of the embodiment of fig 1, and
Figs 3 and 4 show the influence of base biases on amplitude harmonics for a transistor with one emitter finger and a length of 24$\mu$m and 11$\mu$m respectively, and
Figs 5 and 6 show the influence of emitter lengths on amplitude harmonics for base biases of 0.55V and 0.71 V, respectively, and
Figs 7-9 show the output spectrum of the embodiment of fig 1 for differing multiplication factors.
DETAILED DESCRIPTION

Embodiments of the present invention will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. The invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Like numbers in the drawings refer to like elements throughout.

The terminology used herein is for the purpose of describing particular embodiments only, and is not intended to limit the invention.

Fig 1 shows an embodiment 100 of a frequency multiplier. As is shown in fig 1, the frequency multiplier 100 comprises a first stage 105 which is arranged to receive an AC input signal at an input port 102. Since the input signal is an AC signal, it will have a certain frequency, f₀. The first stage 105 is arranged to generate an output signal which comprises harmonics, i.e. signals at frequencies which are multiples of the frequency f₀ of the input signal. The first stage 105 is arranged to deliver its output signal at an output port 107.

The first stage 105 is, in this embodiment, designed as a bipolar junction transistor 145 with its base used as the input port 102 via a DC decoupling capacitor C. The base of the transistor 145 is biased by means of a bias voltage Vₜ via a resistor Rₜ. Suitably, the transistor 145 is biased at so called "class B operation", in order to generate a multitude of strong harmonics.

The emitter of the transistor 145 is grounded, and the collector is used as the output port of the first stage 105 and is biased by means of a bias voltage Vₖ via an inductor Lₖ. The collector of the transistor 145 is thus indicated as "meeting" an input port of the second stage 110 of the frequency multiplier.
100 at the point shown as 107, which thus serves as both the output port of the first stage 105 and the input port of the second stage 110 of the frequency multiplier 100.

As is implied by the name, a function of the frequency multiplier 100 is to generate output signals which are amplified "frequency-multiples" of the input AC signal, i.e. if the input AC signal has a frequency \( f_0 \), the frequency multiplier 100 should generate amplified output signals at frequencies \( N f_0 \), where \( N \) is 1, 2, 3, ..., with the frequency multiplier 100 preferably being able to generate more than one such output signal, i.e. to generate output signals \( N f_0 \), \((N+1)f_0\), \((N+2)f_0\), etc.

The particular embodiment of a frequency multiplier 100 shown in fig 1 is arranged to generate three such multiples of \( f_0 \), and for that reason, the second stage 110 of the frequency multiplier 100 is equipped with three bipolar junction transistors 115, 120, 125, one for each multiple which is to be generated by the frequency multiplier 100. In the description below, by way of example, the multiples which are described as being generated are \( N=3 \), 4 and 6, although, using the description below, the principles utilized by the frequency multiplier 100 will be realized, so that the generation of signals at frequencies which are more or less arbitrary (integer) multiples of the input frequency \( f_0 \) can be performed using those principles. In addition, only the details regarding one of the transistors in the second stage 110, in this case the transistor 115, will be described, since the transistors 120 and 125 are utilized in a manner similar to that of the transistor 115.

As shown in fig 1, the transistor 115 is arranged to receive the input signal to the second stage 110 via the port 107, which is connected to the base of the transistor 115 via a decoupling capacitor \( C_1 \). The base of the transistor 115 is biased by means of a base bias voltage \( V_{bi} \), in this case via a resistor \( R_{bi} \).
The emitter of the transistor 115 is connected to ground, and the collector of the transistor 115 is used as an output port for the signal from the transistor 115. In addition, the collector of the transistor 115 is also subjected to a DC supply voltage $V_{c1}$ via an inductor $L_{c1}$. The output signal from the transistor 115, i.e. the signal from the collector, is, suitably via a capacitor $C_{s1}$, passed through a filter, in this case a frequency filter 130, e.g. a high-pass or band-pass filter, which is optimized for the output signal which is expected from the transistor 145, a notion which will be explained in more detail later in this text.

Thus, as can be seen from fig 1, the second stage 110 of the frequency multiplier 100 can be said to comprise three branches, one of which has been described above, where each branch has "at its heart" a bipolar junction transistor 115, 120, 125, each of which is coupled to "its own" frequency filter 130, 135, 140. Each branch also comprises capacitors, resistors and inductors which correspond to $C_1$, $C_{s1}$, $R_{b1}$, $L_{c1}$ and the base bias voltage $V_{b1}$ and supply voltage $V_{a1}$ described above, which are numbered correspondingly, e.g. $C_NN$ for the decoupling capacitor of branch number $N$ and $V_{bN}$ for the base bias voltage of transistor number $N$.

Since the frequency multiplier 100 in its general form comprises $N$ branches, one for each frequency multiple which it is intended to generate, it also comprises $N$ output ports, each output port being the output port of the frequency filter of that particular branch. In the example shown in fig 1, there are three branches, and thus three output ports 107, 108, 109.

Returning now to the branch of the second stage 110 which comprises the transistor 115, this branch is intended to generate an output signal at a frequency of $3f_0$. This can be accomplished in different manners, as will be explained below. However, regarding the frequency filter 130 to which the
transistor's collector, i.e. output terminal, is connected, the frequency filter is
designed so as to let the multiple which is generated by that transistor, i.e. in
this case 3*f₀, be the dominant frequency in the output signal from the filter.
The frequency filter 130 is thus designed to only admit signals at that
frequency, and to suppress the other frequencies, and can be designed as a
high pass filter which ideally only admits frequencies equal to or larger than
3*f₀, or as a band-pass filter, the pass-band of which is centered around 3*f₀.

Turning now to how the transistor 115 is made to generate a signal at a
frequency of 3*f₀, various principles can be used, one of which is to use
differing base bias voltages Vₜₙ for each transistor, with the base bias
voltage being chosen so as to generate an output signal in which the desired
frequency multiple is at a maximum value, i.e. as large as possible (in
amplitude) as can be obtained by varying the base bias voltage. In this case,
the transistor 115 should then have Vₜ₁ chosen so that 3*f₀ is at a maximum
value from the collector of the transistor. The output signal from the collector
is then connected to the filter 130, which is, as mentioned, designed so as to
let the signal 3*f₀ be the dominant frequency in the output signal from that
filter, or, to put it differently, to "cleanse" the output signal as far as possible
from other harmonics and other signal components than 3*f₀, and to let 3*f₀
become the "dominant" frequency in the output signal from the filter.

Regardless the choice of differing base bias voltages for the different
transistors in the different branches depending on which frequency multiple it
is intended to generate in each branch, one principle which can used is as
follows: the higher the frequency multiple that it is desired to generate in a
branch, the higher the bias voltage used for the base of the transistor in that
branch. In other words, if branch K is intended to generate multiple K and
branch L is intended to generate multiple L, and K>L, then Vₜₖ>Vₜₙ. Since, in
the example 100 of fig 1, branch 1 is intended to generate 3*f₀, branch 2 is
intended to generate $4f_0$ and branch 3 is intended to generate $6f_0$, then $V_{b3} > V_{b2} > V_{b1}$. This also means that the frequency which the frequency filter in branch $K$ is designed to optimize will always be greater than that of the frequency filter branch $L$.

It should be pointed out that the choice of different base bias voltages for the different transistors will not generate "pure" output signals at the desired frequencies from the transistors, but it will serve to generate output signals in which the desired multiple is as large as possible, i.e., at a maximum value.

Another factor which influences the amplitude of the desired multiple frequency in each branch is the size of the transistors in each branch. The size of a transistor is here defined as the number of emitter "fingers" and the length of each finger for bipolar transistors, and, for the case of FET transistors, by the number of gate "fingers" and the width of the gate "fingers". This mechanism can suitably be used together with the variation of the base bias voltages described above. One way of using this mechanism is simply to let the size of each of the N transistors decrease for increasing frequency multiples, so that if branch $K$ is intended to generate multiple $K$ and branch $L$ is intended to generate multiple $L$, and $K > L$, then the size of transistor $L$ is at least equal to or suitably greater than that of transistor $K$. Since, in the example 100 of fig 1, branch 1 is intended to generate $3f_0$, branch 2 is intended to generate $4f_0$ and branch 3 is intended to generate $6f_0$, then transistor 115 is at least equal to or suitably larger than transistor 120, which in turn is larger than transistor 125.

Another way of varying the base bias voltages and sizes of the transistors in the different branches in order to obtain the desired frequency multiples is to perform simulations while designing the frequency multiplier 100. In other words, the base bias voltage and size of each of the N transistors would then
be obtained by means of "sweeping" all combinations of bias voltages in a range of \( V_1 - V_2 \) and all transistor sizes in a range of \( L_i-L_2 \), and for each of the \( N \) transistors, the combination of bias voltage and transistor's size is chosen which gives the maximum gain for the desired frequency multiple. The word "sweeping" is here used in the sense that as many values as possible within the bias voltage range is tested with as many values as possible within the size range. Suitably, this testing is performed by way of computerized simulation in order to arrive at optimal combinations of base bias voltage and transistor size for each desired output multiple, i.e. for each branch of the second stage of the frequency multiplier 100.

As mentioned, each branch in the second stage is used to generate a specific amplified harmonic of the input signal, primarily by means of the transistor and the frequency filter of each branch. The output signal from the first stage, which is used as input signal to each branch of the second stage 120, comprises the 1\(^{\text{st}}\), 2\(^{\text{nd}}\), 3\(^{\text{rd}}\) ....etc harmonics of the input signal, but it is desired to separate them from each other, as well as to amplify them. This is the reason that one branch is used for each harmonic that it is desired to generate in the frequency multiplier: each branch serves as an amplifier and "separator" for a specific harmonic in the signal from the first stage.

Regarding the amplification function of each branch, we can take the branch with the transistor 125 as an example. By means of this branch, it is intended to generate an amplified 6\(^{\text{th}}\) harmonic of the frequency of the input signal \( f_0 \): the transistor 125 of this branch (as well as those of the other branches) has the combined functions of an amplifier, a mixer and a multiplier: the 6\(^{\text{th}}\) harmonic obtained at the output of the transistor 125 is the sum of:

- the amplified 6\(^{\text{th}}\) harmonic, as amplified by the transistor 125,
• the mixing component of the 1\textsuperscript{st} and the 5\textsuperscript{th} harmonics and mixing component of 2\textsuperscript{nd} and 4\textsuperscript{th} harmonics as mixed by the transistor 125, and

• the multiplied component of the 3\textsuperscript{rd} harmonic (frequency doubled), and multiplied component of the 2\textsuperscript{nd} harmonic (frequency tripled) as multiplied by the transistor 125.

Consequently, each branch will amplify the desired harmonic \(N'f_0\) in a highly efficient manner, due to the three mechanisms which have been listed in the "bullet points" above.

Returning now to the issue of how different combinations of transistor size and base bias voltage will affect the harmonics generated in each of the \(N\) branches, in this case in each of the three branches of the embodiment shown in fig 1, this effect will now be illustrated with the help of some examples.

Fig 2 shows the spectrum of the output signal from the first stage 105 to the second stage 110 at the port 107 when the input signal to the first stage at its input port 102 has a frequency of 20 GHz and a power level of 3 dBm. As can be seen, the output signal from the first stage is rich in harmonics. As this output signal is applied at the base of each of the transistors 115, 120 and 125, the desired harmonics can be obtained, for example, the 3\textsuperscript{rd}, 4\textsuperscript{th} and 6\textsuperscript{th} harmonics.

Fig 3 shows the 3\textsuperscript{rd}, 4\textsuperscript{th} and 6\textsuperscript{th} harmonics at the collector of a single transistor which has a single emitter finger with a length of 24 \(\mu\text{m}\), as a function of the base bias voltage. Thus, fig 3 shows the output from a single transistor without any subsequent filtering.
As is underscored by fig 3, the amplitude of the harmonics depends on the base bias voltage. At a large base bias voltage (>0.55V), the 4th harmonic is larger than the 3rd and the 6th harmonics, while at lower base bias voltage, the 4th harmonic is less than the 3rd and the 6th harmonics. The 3rd harmonic is always larger than the 6th harmonic. Thus, the results of fig 3 indicate what has been described above regarding the base bias voltages of the transistors, i.e. that that the transistors of the second stage should be biased by different voltage in order to enhance the desired harmonic from each transistor. Regarding the issue of differing transistor size, the size of the transistors from which the graph of fig 3 was obtained was that it had one emitter finger with a length of 24\( \mu \)m, in other words the transistor used was a bipolar junction transistor.

Fig 4 shows the same as fig 3, i.e. the amplitude of the 3rd, 4th and 6th harmonics generated by a single transistor using the input signal shown in fig 2, as a function of base bias voltage but now with a transistor size of that has one emitter finger with a length of 11\( \mu \)m. We can see, by comparing figs 3 and 4, that the behaviour of the harmonic amplitude as a function of the base bias voltage varies with the transistor size. In fig 4, the harmonic amplitudes increases with increasing base bias voltage, and the 4th harmonic is always larger than the 3rd and 6th harmonic.

Fig 5 shows the amplitudes of the 3rd, 4th and 6th harmonics versus the length of the emitter from a single transistor with one emitter finger for a base bias voltage of 0.55 V. As can be seen, the 4th harmonic drops with the increasing of the emitter length, while the 3rd and the 6th harmonic have a minimum at the emitter length of 16 \( \mu \)m.

Fig 6 shows the same as fig 5, but with a base bias voltage of 0.71 V. It can be seen that the basic features of the curves of the harmonics are similar to
those of fig 5, and thus do not change as the base bias varies, although the specific values of the amplitudes do change.

With reference to Figs 3-6, we can conclude that one efficient way of optimizing transistor size and base bias voltage is to "sweep" all combinations of transistor size and base bias voltages, although the term "all combinations" can be limited by what is practically possible, so that the range of transistor sizes and base bias voltages within the combinations that are swept is kept down. The verb "to sweep" is here used in the sense that all combinations of transistor sizes and base bias voltages are tried, in the same manner that has been shown in figs 5 and 6. However, it should be emphasized that the other principle described herein, i.e. increasing base bias voltage and decreasing transistor size as the desired harmonic increases will also give good results.

As seen above, the base bias voltage of the transistor in each branch can be varied depending on the harmonic which it is desired to generated in that particular branch. As an alternative, the base bias voltages can be used as "switches" or "multiplication factor selectors": if only the harmonic (multiple) which is generated in one of the branches of the second stage 110 is desired, the base bias voltages of the transistors in the other branches can be set to zero, or set as "floating" (i.e. no base bias voltage used), by means of which the transistors in the other branches are shut down, and thereby not generating any output signals. Examples of such operation of the frequency multiplier 100 will now be shown for each of the three branches of the second stage 110, with reference to figs 7-9. However, it should be emphasized that it is also possible for the frequency multiplier 100 to be made to deliver signals at harmonics of the frequency $f_0$ of input signal, i.e. in the example shown above, output signals at frequencies $3f_0$, $4f_0$ and $6f_0$. 
simultaneously, if all transistors in the second stage are in the "on" state, and are base biased as described above.

Fig 7 shows the output spectrum from the frequency multiplier 100 with the transistors 120 and 125 "shut down", so that only the branch with the transistor 115 is in operation. It should be pointed out that fig 7 shows the output after the frequency filter 130 of the branch, which is the same for figs 8 and 9, i.e. the output signals are shown after the respective frequency filters 135 and 140. In figs 7-9, an input signal at a frequency of 20GHz and a power level of 3 dBm is used to the frequency multiplier 100 at port 102.

In fig 7, the base bias voltage is set to 0.42 V for transistor 115, and the base bias voltages for transistors 120 and 125 are set to zero. These values of base bias voltages give a frequency multiplier which operates as a x3 frequency tripler. As can be seen in fig 7, the spectrum of the output signal from the frequency filter 130 is dominated by the 3rd harmonic at about 60GHz. The conversion gain of the multiplier, i.e. the ratio between the input power and the power of the desired harmonic, in this case the 3rd harmonic, is 5.7 dB. The input signal to the frequency multiplier 100 at port 102 had a frequency of 20 GHz and a power level of 3 dBm. The transistor 115 has a single emitter finger with a length of 24 μm.

In fig 8, the base bias voltage is set to 0.57 V for transistor 120 and the base bias voltages for transistors 115 and 125 are set to zero. These values of base bias voltages give a frequency multiplier which operates as a x4 frequency quadrupler. As can be seen in fig 8, the spectrum of the output signal from the frequency filter 135 is dominated by the 4th harmonic at about 80GHz. The conversion gain of the multiplier is 0 dB. The input signal to the frequency multiplier 100 at port 102 had a frequency of 20GHz and a
power level of 3 dBm. The transistor 120 has a single emitter finger with a length of 24 \( \mu \text{m} \).

In fig 9, the base bias voltage is set to 0.71 V for transistor 125 and the base bias voltages for transistors 115 and 120 are set to zero. These values of base bias voltages give a frequency multiplier which operates as a 6th frequency sixtupler. As can be seen in fig 9, the spectrum of the output signal from the frequency filter 140 is dominated by the 6th harmonic at about 150GHz. The conversion gain of the multiplier is -4 dB. The input signal to the frequency multiplier 100 at port 102 had a frequency of 25 GHz and a power level of 3 dBm. The transistor 125 has a single emitter finger with a length of 11 \( \mu \text{m} \).

In summation, some advantageous features of the frequency multiplier 100 of fig 1 are:

1) The second stage 110 comprises multiple outputs, each of which is connected to a different transistor via a frequency filter.

2) Bias voltages \( V_{b1}, V_{b2} \) and \( V_{b3} \) at the base of the transistors 115, 120, 125, in the branches of the second stage 110 determine the output of the branch in question, corresponding to a certain frequency multiplication factor, and can also be used in order to turn each output either "on" or "off". Thus, the transistors 115, 120 and 125 of the different branches in the second stage 110 have dual functions, both as a part of multiplier and as an on/off switch.

3) All transistors in the branches of the second stage can be set to "on" simultaneously, so that the frequency multiplier delivers different frequency multiples simultaneously.
4) The size and bias voltages of the transistor 115, 120 and 125 in the second stage 110, as well as the characteristics of the frequency filters 130, 135 and 140 determine the dominant harmonic which is output from each frequency filter.

5) The multiplying factor selection is electrical, i.e. it comprises changing the base bias voltage of the transistors in the second stage 110 of the frequency multiplier 100.

6) The two-stage design of the multiplier 100 obviates the need for inter-stage amplifiers, thereby saving DC-power consumption and chip area.

Finally, it should be pointed out that the frequency multiplier 100 is not limited to the number of outputs and branches which have been described above and shown in the drawings. The number of branches and thereby the number of outputs can be more (or less) than 3, so that more (or less) transistors and high pass filters are used in branches of the second stage. The multiplication factor can also be changed, by means of changing the base bias voltages of the transistors and the characteristics of the frequency filters to which each transistor is connected.

Throughout in the text above as well as in the drawings, the transistors in the power detectors have been shown and described as bipolar junction transistors. As those skilled in the art will realize, other kinds of transistors can also be used, for example Field Effect Transistors, FETs. If such a substitution is made, the transistor terminals in the description above, as well as in the drawings, should be substituted as follows:

Bipolar junction transistor  FET
In the drawings and specification, there have been disclosed exemplary embodiments of the invention. However, many variations and modifications can be made to these embodiments without substantially departing from the principles of the present invention. Accordingly, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation.
CLAIMS

1. A frequency multiplier (100) comprising a first (105) and a second (110) stage connected in series with each other, the first stage (105) being arranged to receive (102) an input AC signal and to generate an output signal comprising harmonics of said input AC signal and to deliver said output signal to the second stage (110), in which frequency multiplier (100) the second stage (110) comprises integer N bipolar/FET transistors (115, 120, 125), each of which is arranged to receive the output signal from the first stage at its base/gate and to be biased by means of a base/gate bias voltage ($V_{b1}$, $V_{b2}$, $V_{b3}$), each of which transistors has its emitter/source grounded, the frequency multiplier (100) being characterized in that in said second stage (110) the base/gate bias voltage ($V_{b1}$, $V_{b2}$, $V_{b3}$), of each of said N transistors is different from that of every other of said N transistors, with each of said N transistors being arranged to deliver at its collector/drain a signal at frequency which is a multiple of the frequency of the input signal, said multiple being unique for each transistor by virtue of the differing base/gate bias voltages being chosen so as to generate an output signal from the transistor in which said chosen multiple is at a maximum value, with each of the N transistors in the second stage having its collector/drain connected to one of N frequency filters (130, 135, 140), the frequency filter for each transistor being specific for that transistor in that the frequency filter of each transistor is adapted to let said multiple which is generated by that transistor be the dominant frequency in the output signal from the filter, with each of said frequency filters (130, 135, 140) having an output port (107, 108, 109) which is arranged to be one of N output ports of the frequency multiplier (100).

2. The frequency multiplier (100) of claim 1, in which the size of each of said N transistors (115, 120, 125) differs from that of each of the other of N
transistors (115, 120, 125), said size being determined by the number of
emitter fingers and the length of each finger for bipolar transistors and by the
number of gate fingers and the width of the gate fingers for FET transistors.

3. The frequency multiplier (100) of claim 1 or 2, in which the base/gate bias
voltage of the N transistors (115, 120, 125) increases for increasing
frequency multiples.

4. The frequency multiplier (100) of claim 1 or 2, in which the size of each of
said N transistors (115, 120, 125) is kept constant or decreases for
increasing frequency multiples.

5. The frequency multiplier (100) of claim 1 or 2, in which the base/gate bias
voltage and size of each of the N transistors (115, 120, 125) is obtained by
means of sweeping all combinations of bias voltages in a range of \( V_1 - V_2 \) and
all transistor sizes in a range of \( L_1 - L_2 \), and for each of the N transistors, the
combination of bias voltage and transistor's size is chosen which gives the
maximum conversion gain for the desired frequency multiple.
Fig 3
Fig 4
Fig 5
Fig 6
Fig 7
INTERNATIONAL SEARCH REPORT

PCT/EP2013/077727

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03B19/14

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
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<th>Relevant to claim No.</th>
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<td>JP 2000 349557 A (MURATA MANUFACTURING CO) 15 December 2000 (2000-12-15) figure 7</td>
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<td>A</td>
<td>US 4 401 952 A (BASAWAPATNA GANESH R [US]) 30 August 1983 (1983-08-30) figure 1</td>
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<td>CN 102 522 95 A (INST OF MICROELECTRONICS CAS) 27 June 2012 (2012-06-27) figure 1</td>
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See patent family annex.

Further documents are listed in the continuation of Box C.

* Special categories of cited documents:
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Date of the actual completion of the international search: 7 August 2014

Date of mailing of the international search report: 18/08/2014

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Schnabel, Florian
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<td>US 3 202 840 A (AMES J R MILARD E) 24 August 1965 (1965-08-24) figure 7</td>
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<td>A</td>
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